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SEPTEMBER 30, 1981

Introducing Systems & Software: Integrating local networks



MEMORY TECHNOLOGY

Special Reports:

Magnetic, Semiconductor, and Optical Media

Track-following floppy expands storage capacity

RAM controller chip builds large FIFOs

Static MOS RAM beats bipolars in speed-power

Meet the first 128-k EPROM

IC sets memory system errors aright

Design memory systems the byte-wide way

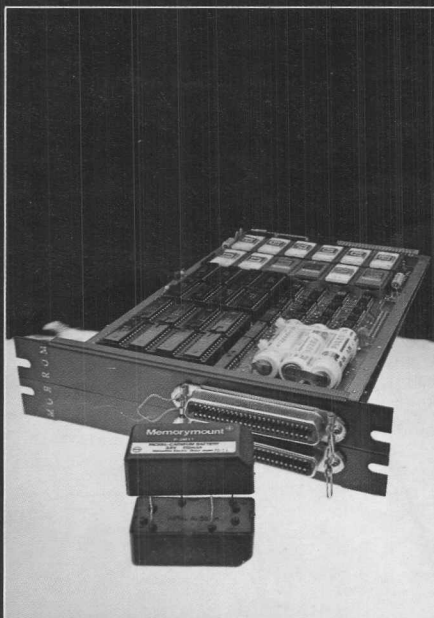
Intelligent streaming tape drive backs up Winchesters

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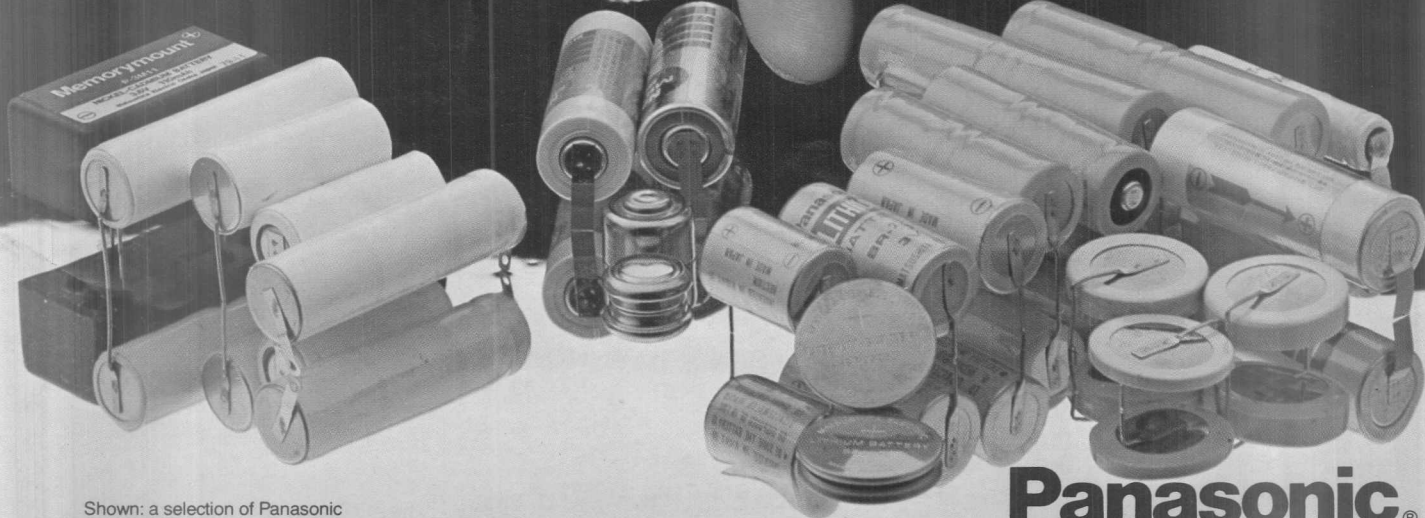
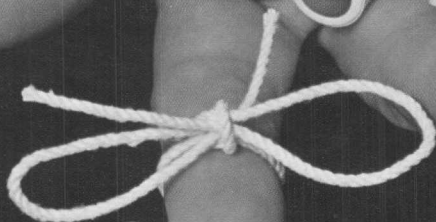


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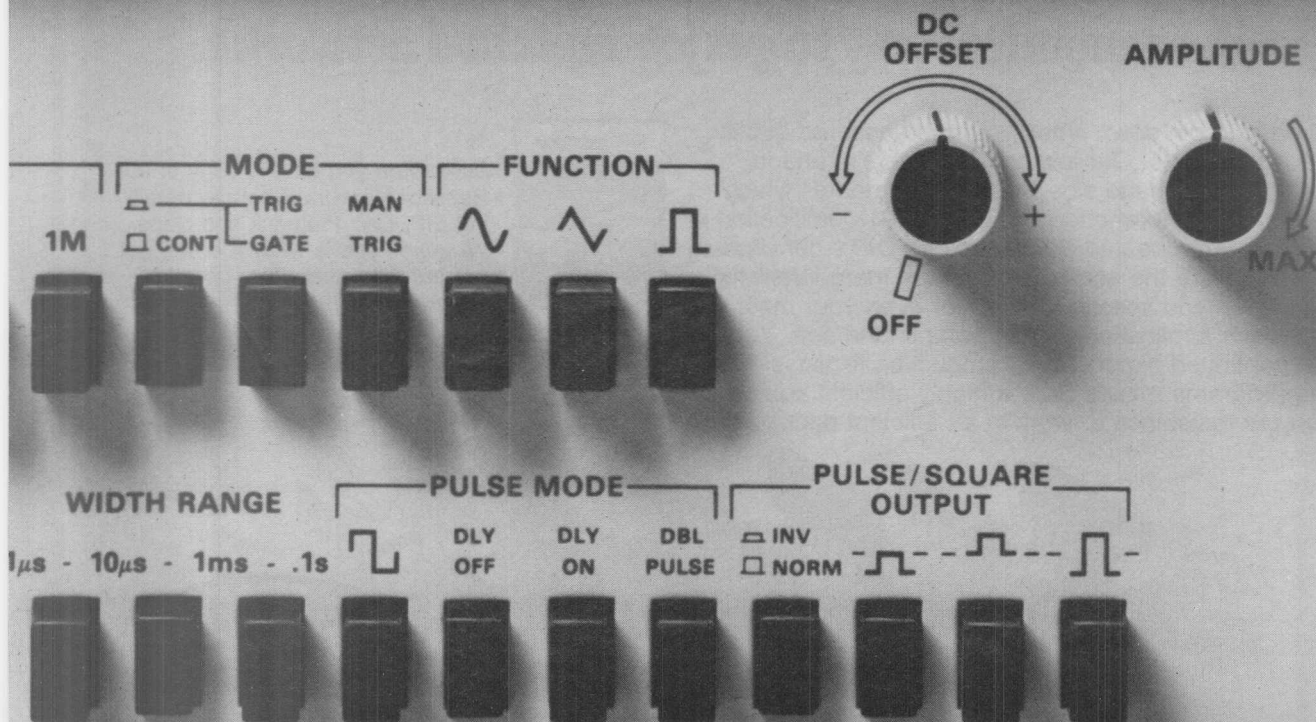
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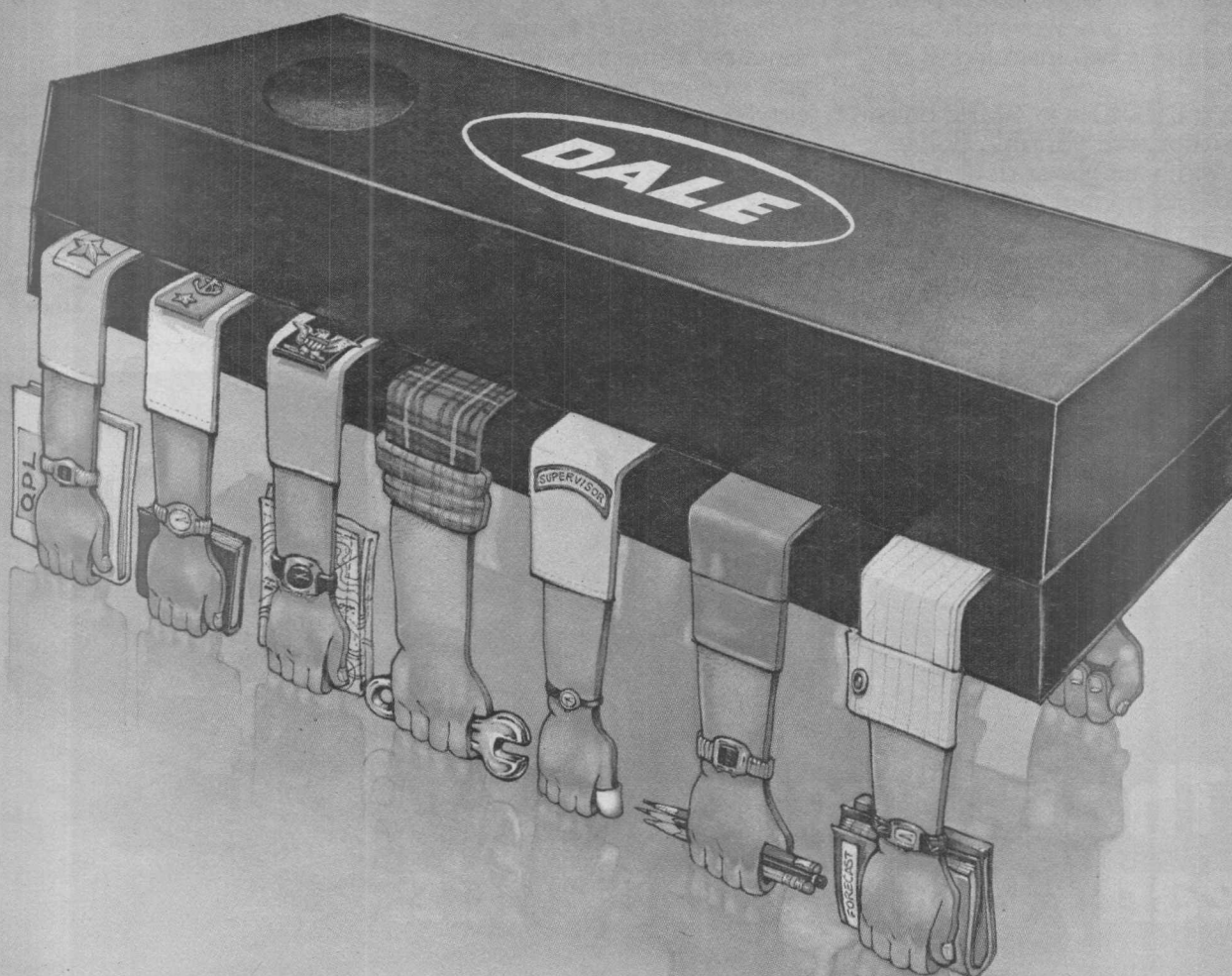
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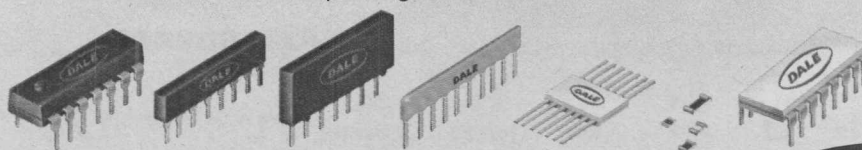
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This Memory Technology issue won't readily be forgotten. It boasts three staff-written special reports, as well as eight design articles, each of which introduces an important new piece of memory-related hardware. What's more, the issue kicks off a new series for systems integrators—Systems & Software.

The memory-technology special reports begin with Computers Editor Len Yencharis's assessment of magnetic-recording technology, which he finds is centering not on developing new media and techniques, but on refining those that already exist. "With the possible exception of thin-film magnetics, the field is starting to follow in the tracks of semiconductor processing to minimize the cost/performance ratio," Yencharis reports.

In the semiconductor-memory field, Senior Editor Dave Bursky finds that performance limits are a will-o'-the-wisp—just as they are about to be reached, they move further away. Redundancy and error-correcting circuitry are enabling designers to live comfortably with the less-than-perfect devices that typify high-density solid-state devices.

Optical-disk storage for archival applications appears almost certain to become widespread within the next five years, according to Field Editor Jonah McLeod. However, critical problems still hinder the development of erasable optical disks; McLeod's report identifies the problems and examines the state of current research aimed at finding solutions.

Integrating the various subsystems that make up a complete computer system is growing more difficult. As subsystems become more complex, problems are increasing, not going away. The Systems & Software series, which stresses the total systems viewpoint, leads off with a four-part report on integrating local networks.

Driven by the need for greater productivity in non-manufacturing activities, business organizations are gearing up to install networks of computers and peripheral devices that will allow users to share such resources as data bases, printers, and telecommunications facilities. However, systems integrators with plans to penetrate such application areas will not only have to select the proper architecture, software, and hardware but also have to keep abreast of the ongoing efforts to establish standards for network communications. Our four-part report will point them in the right directions.

The next installment of Systems & Software, which will appear in the November 12 issue, will cover the growing impact of software automation.

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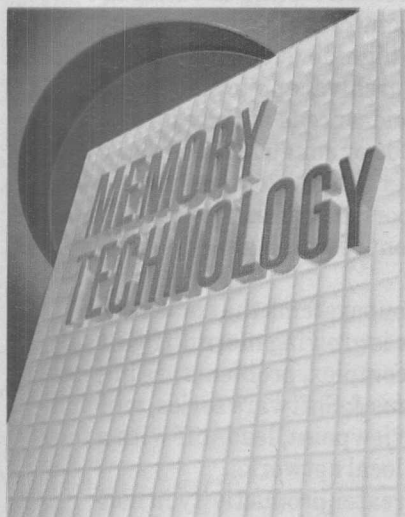
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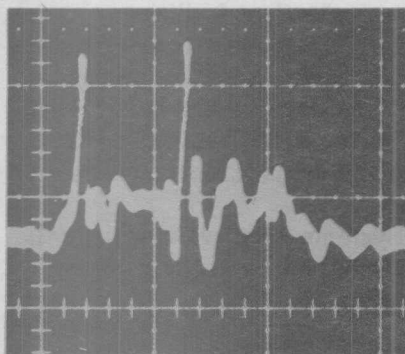
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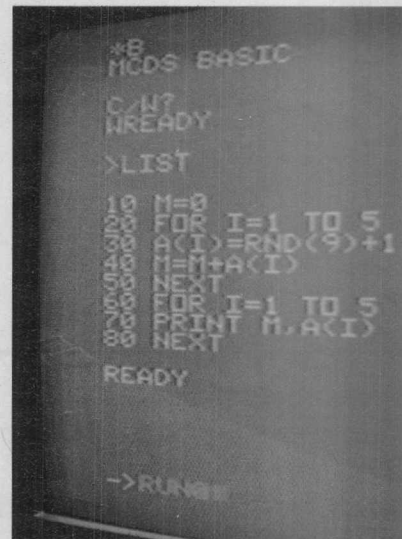
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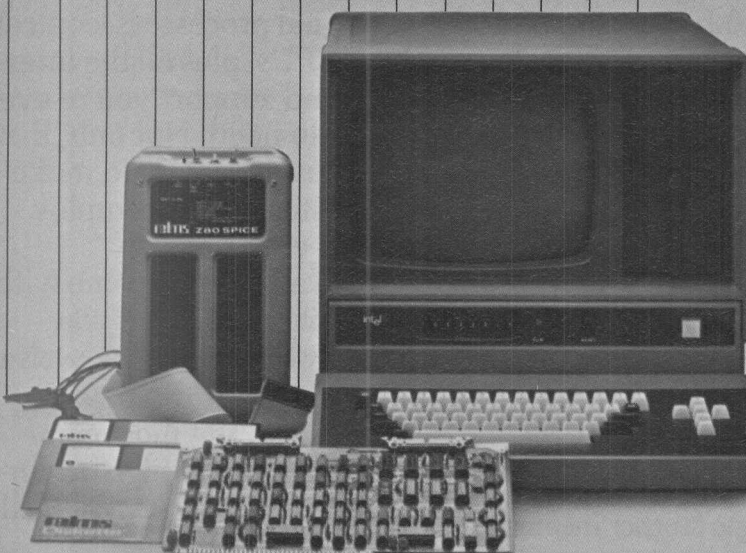
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Editorial

Should the IEEE give its president a paycheck?

The IEEE president a hired hand? That's what might happen if a resolution approved at the Professional Activities Committee conference in July gets the green light. In fact, the PAC conference felt that the IEEE vice president for professional activities and possibly several other executive offices should also be paid positions.

The reasoning behind the idea is simple enough. PAC members would like to see working engineers (as opposed to corporate executives and academics on sabbatical) get some of the top Institute jobs. They figured that the present setup makes this possibility extremely remote, since anyone depending on a regular salary can't very easily get a year off with pay to do "volunteer" work for the IEEE. And it's a fair assessment that the jobs of IEEE president and vice president for professional activities can't very well be done on a part-time basis.

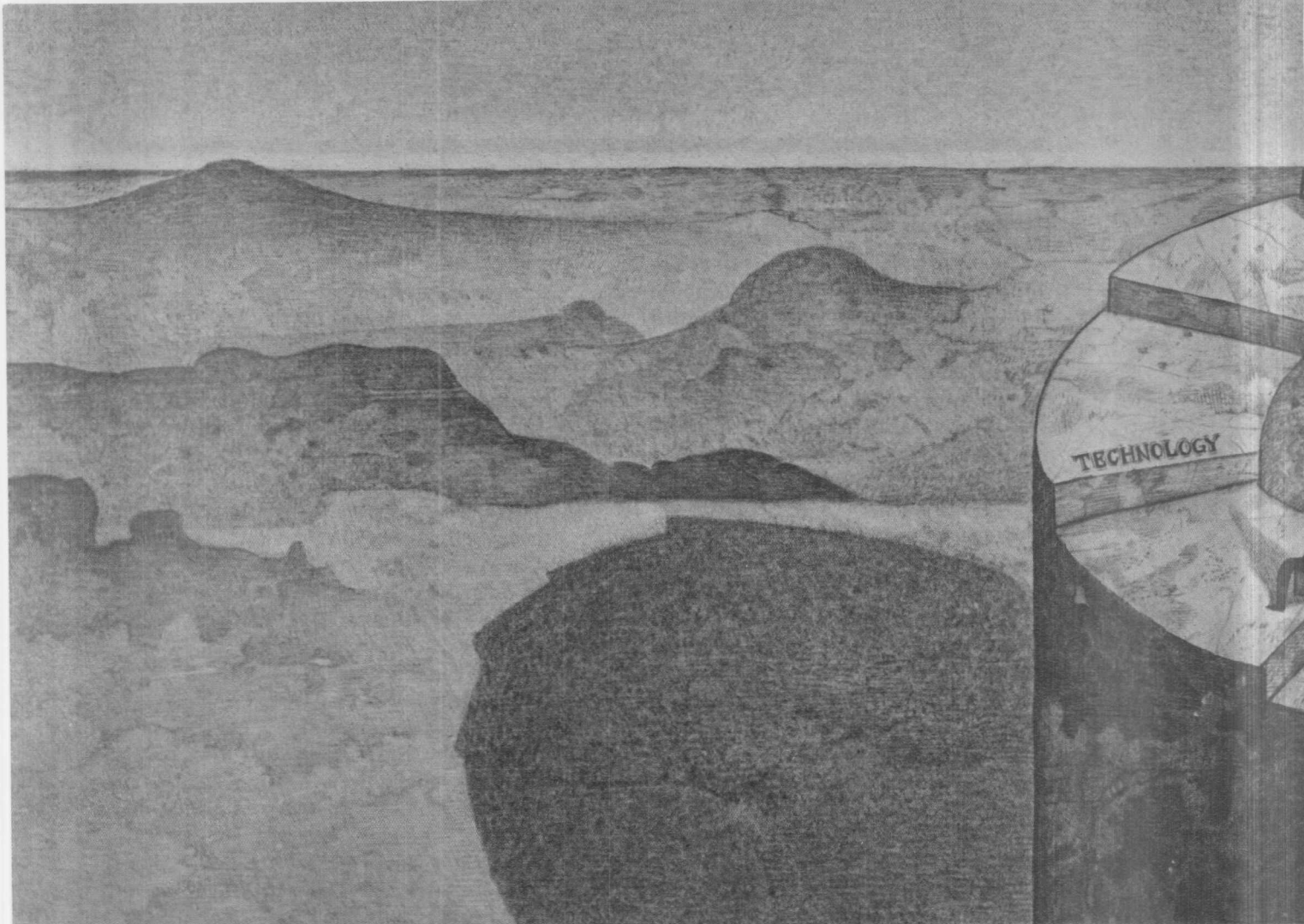
The only problem is that few (if any) working engineers are waiting eagerly in the wings, ready to champion the professional health of their fellows if only they could feed their families at the same time. This year, every national office on the IEEE annual election ballot is being sought by one hand-picked candidate nominated by the Board of Directors. There are no constitutional amendments of any kind and no petition candidates. The flap that erupted last year

over the president-elect amendment has been effectively quashed. The Board of Directors enjoys more influence than ever before over the election process, and outsiders now face an enormous obstacle just getting noticed—let alone elected. Apathy is at an all-time high.

In other words, unless the Institute membership starts signing petitions, voting in elections, and taking a more active interest in the IEEE, there is little reason to subsidize the present crop of high-ranking "volunteers" with a paycheck derived from members' dues. If the time ever comes that a cross section of IEEE officers and candidates is a true reflection of the larger engineering community, there will be ample opportunity to consider the sacrifices made by those with interrupted employment.

Right now the IEEE would be best advised to save its money. As IEEE president Richard W. Damon says in *The Institute*, September 1981: "By the time an engineer has put in the number of years of service to IEEE required to be elected president, his employers have come to appreciate and support his participation in a professional society."

That, of course is exactly the problem the PACs should be dealing with. The IEEE will never be effective on behalf of its members' best interests so long as top Institute positions are simply high-status plums for rewarding service and recognizing seniority.



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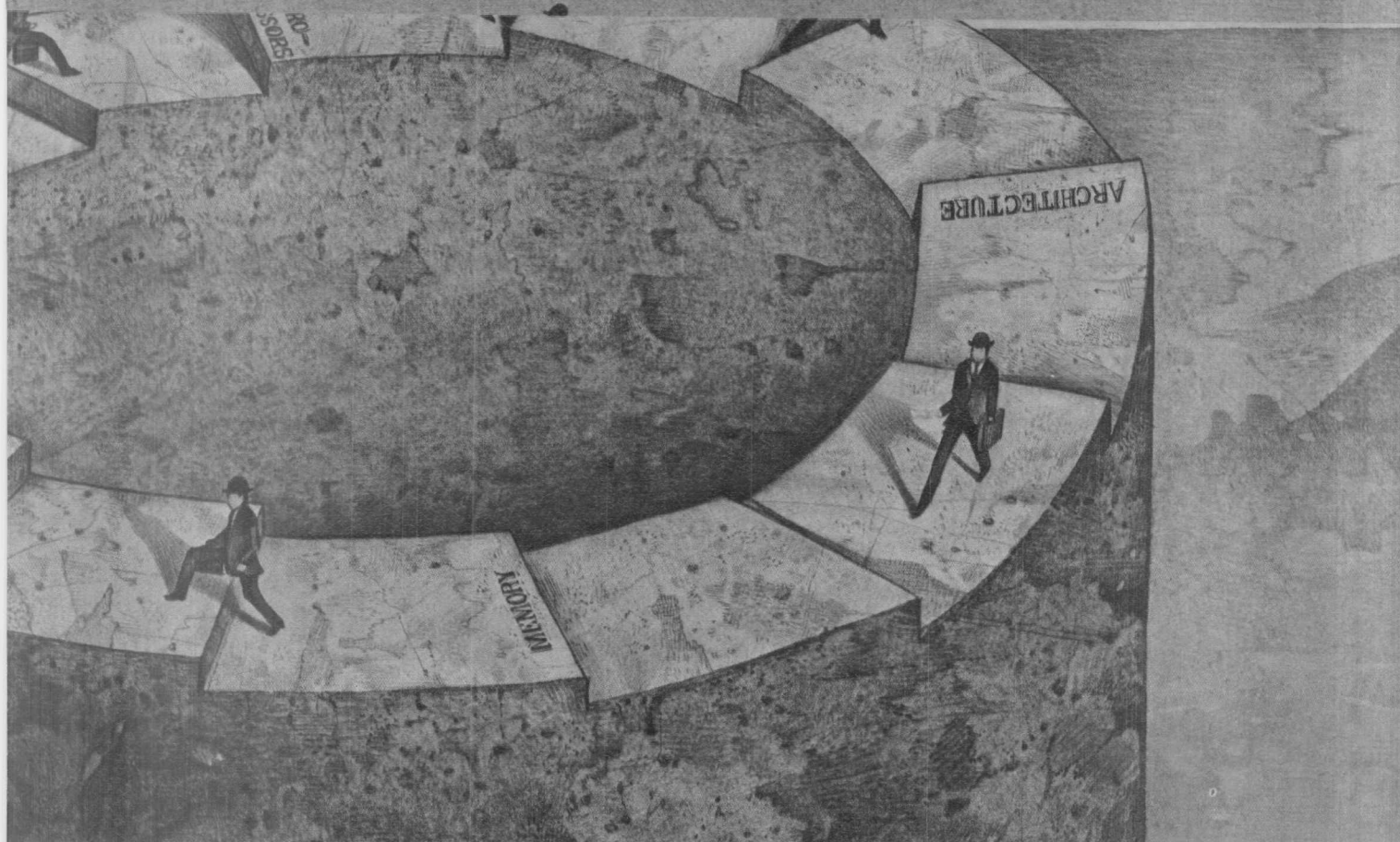
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Letters

Trespassing signals make great gift

Regarding unauthorized reception of subscription TV or any other signal: It is obvious that I cannot intercept such a signal unless it impinges on my property. Either the signal belongs to the originator or it does not. If it does not, then the originator has no complaint coming if I do intercept it, and no complaint if I do anything at all further with it.

If the originator does complain, he evidently believes that the signal belongs to him. But then, his signal has impinged on my property without my permission. The signal then must be considered either a trespass or an unsolicited gift.

If a trespass, then the signal originator will be responsible for removing his signal from my property, something that he would be most unwilling to do: As a trespasser, he presumably is responsible for any damage that his signal might cause. At present, interaction is apparent between the brain and low-level rf signals, but just what this interaction is, has not been determined. The originator would have to prove that his signals do no harm.

This leaves the only possible interpretation: The signal is an unsolicited gift, in which case I have a perfect right to intercept and use the signal. If I have a right to intercept and use the signal, then by logical extension I have the right to purchase equipment to do this. In addition, a supplier has a right to sell me this equipment, since it is not harmful in

itself (and is, in fact, the same equipment that the signal originator wants me to pay to use). And some manufacturer has the right, so long as he does not violate patent and trade-secret laws, to make such equipment for the supplier.

Which leaves the irate signal originator with both feet firmly planted in the ether.

Yale Jay Lubkin
Director of Engineering
Ben Franklin Industries, Ltd.
Casey Creek, KY 42723

Pascal standard getting closer

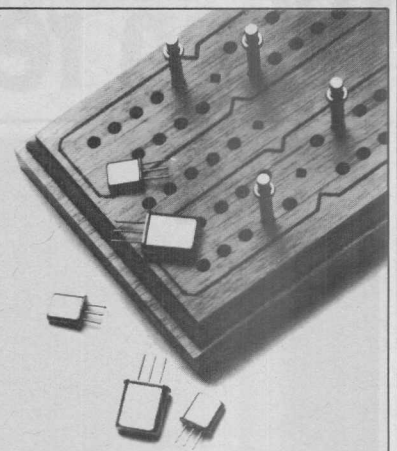
I was saddened to see Max Schindler's report (ELECTRONIC DESIGN, May 28, 1981, p. 38) on our Pascal session at NCC. It seems to me that the report was biased by Mr. Schindler's views about Ada, and was not close to objective about Pascal. The statement by J.A.N. Lee about the time frame for ANSI standards was general, and will not apply to the Pascal effort. Telling the public that the Pascal standard is "years away" was apparently motivated by your belief that Ada should simply replace Pascal.

You neglect the fact that no standard for Ada exists, and that it will take years to obtain one. You discount completely the economic reality of hundreds of millions of dollars' worth of existing Pascal code—a reality that more than justifies the efforts to standardize Pascal, and some reasonable extensions to it.

I believe that the Pascal stan-

(continued on page 16)

Electronic Design welcomes the opinions of its readers on the issues raised in the magazine's editorial columns. Address letters to Editor, Electronic Design, 50 Essex St., Rochelle Park, NJ 07662. Try to keep letters under 200 words. Letters must be signed. Names will be withheld upon request.



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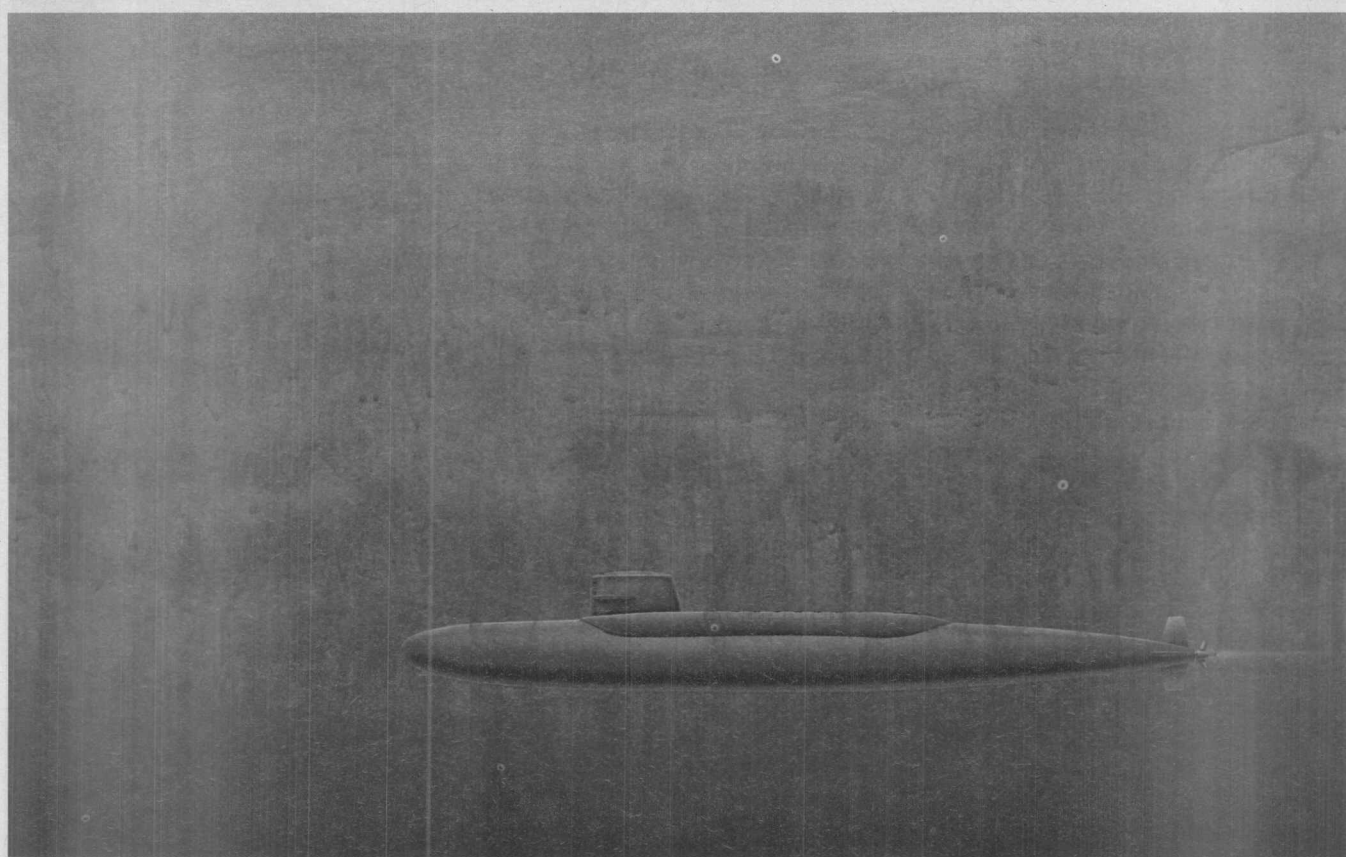
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Antenna Measurement Techniques Symposium, Oct. 13-15. King's Grant Inn, Danvers, MA. Sam Davis, Scientific-Atlanta, 3845 Pleasantdale Rd., Atlanta, GA 30340.

International Telemetry Conference, Oct. 13-15. Bahia Motor Hotel, San Diego, CA. ITC/USA/'81, 21031 Ventura Blvd. Suite 1001, Woodland Hills, CA 91364.

Ultrasonics Symposium, Oct. 14-16. McCormick Inn, Chicago, IL. IEEE.

Northeast Computer Show & Office Equipment Exposition, Oct. 15-18. Hynes Auditorium, Boston, MA. National Computer Shows, 824 Boylston St., Chestnut Hill, MA 02167.

International Symposium for Testing and Failure Analysis, Oct. 19-20. Marriott Hotel, Los Angeles, CA. ISTFA, P.O. Box 742, Lawndale, CA 90260.

Autotestcon, Oct. 19-21. Orlando Hyatt House, Orlando, FL. IEEE.

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Coil Winding '81, Oct. 19-22. Hyatt Regency Hotel, Chicago, IL. ICWA, Inc., Box 159, Libertyville, IL 60048.

Wintek Microprocessor Workshop, Oct. 19-23. Sheraton Inn, Lafayette, IN. Wintek Corp., 1801 South St., Lafayette, IN 47904.

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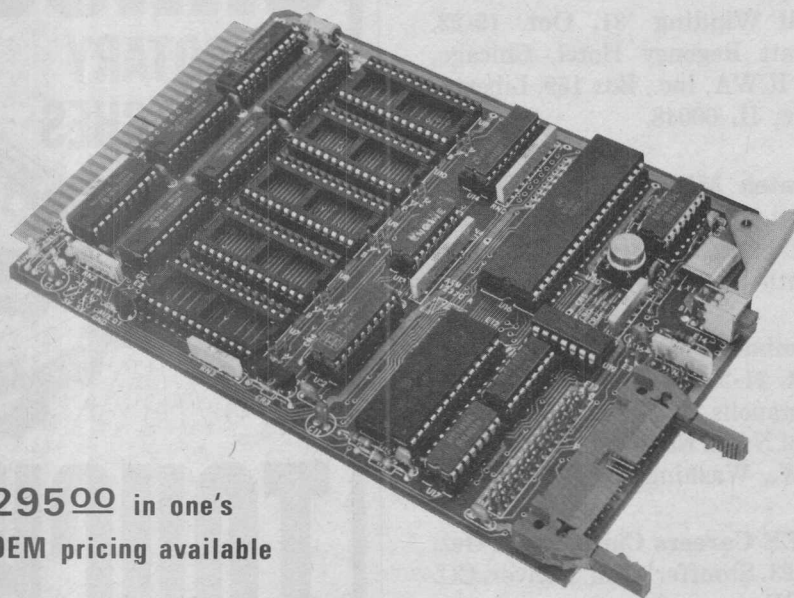
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CIRCLE 12

Letters

(continued from page 13)

standardization effort deserves better, more objective coverage. This standard has broken all records for timeliness, and is an unprecedented, parallel worldwide effort.

Bruce W. Ravenel
Co-Chairman
Joint ANSI/X3J9-IEEE
Standards Committee
Language Resources, Inc.
4885 Riverbend Rd.
Boulder, CO 80301

Mr. Schindler replies

ELECTRONIC DESIGN has repeatedly supported language standards; for a small company like Language Resources to expend a substantial fraction of its efforts on a standards committee deserves the highest praise. Nevertheless, the report's quotes were accurate. Mr. Ravenel's statement that the standard will be complete "within two years" does include the possibility of completion even this year, which would put the headline in error. So much the better.

But the fact remains that both Pascal's originator, Niklaus Wirth, and its apostle in the U.S., Ken Bowles, are no longer advocating Pascal for system design, precisely because of the enumerated limitations of the Pascal draft standard. Ada is far from perfect, and **ELECTRONIC DESIGN** has urged DOD in an editorial to define a kernel quickly (**ELECTRONIC DESIGN**, July 23, 1981, p. 9). However, as long as DOD stands behind Ada, standardization is the language's least problem.

Whether an extended-Pascal standard remains elusive or Ada proves unteachable, the loser is the potential user—**ELECTRONIC DESIGN**'s reader. He will also be the judge of which language serves the industry better.

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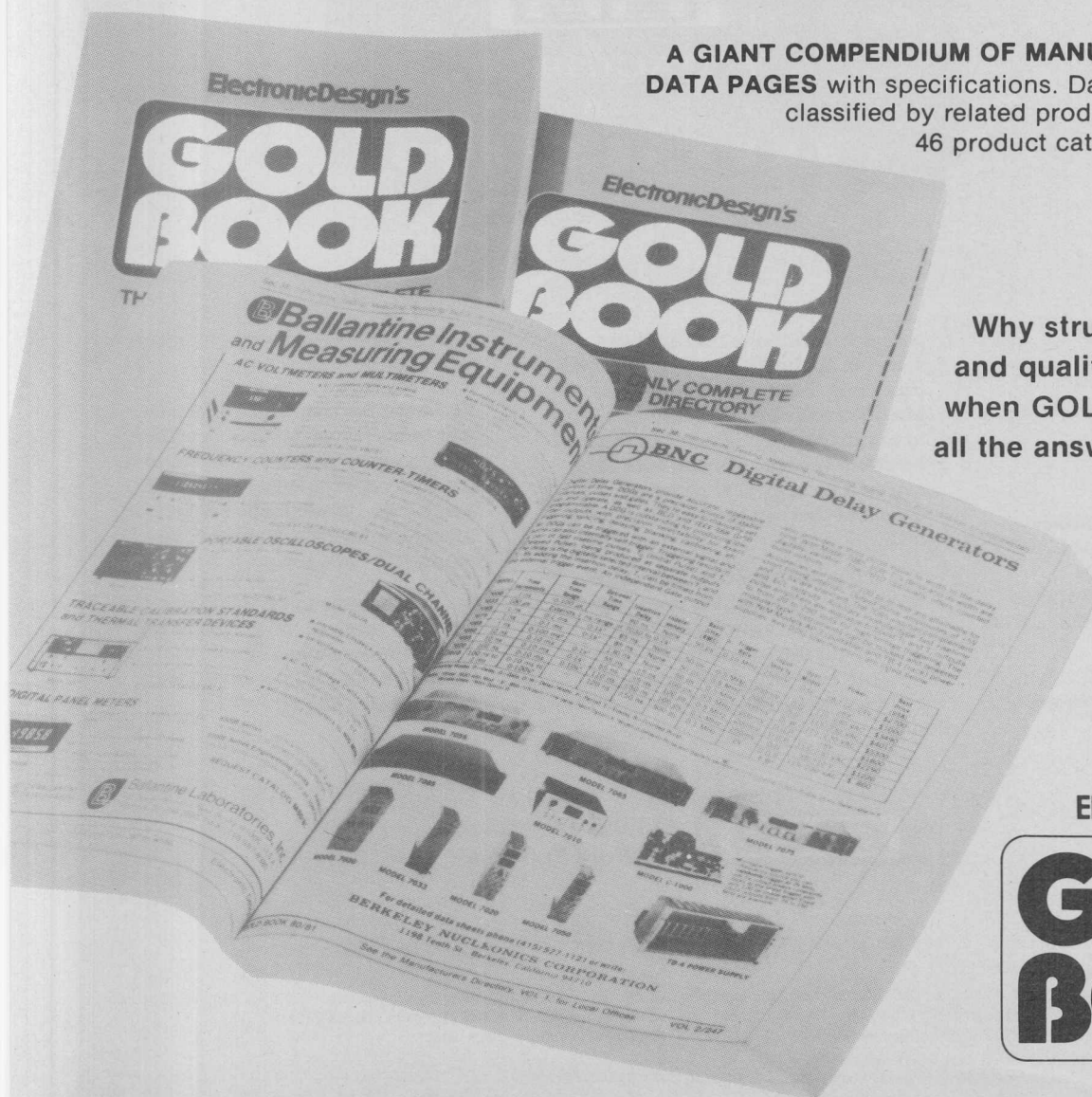
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LateNews

Uncommitted logic arrays use CMOS

A set of CMOS uncommitted logic arrays with up to 2014 cells (each cell containing two p-type and two n-type transistors), allowing users to define logic functions by customizing the interconnections, has been developed by General Instrument Corp. (Hicksville, NY). The CMOS arrays typically dissipate $1 \mu\text{W}/\text{MHz}/\text{gate}$; typical gate delays are 5 ns. GI will offer four ULA chips, with capacities of 560, 960, 1440, and 2014 cells, and 40, 52, 64, and 76 I/O lines, maximum.

Intel codec/filter chip know-how goes to TI

Texas Instruments expects to receive from Intel the masks and other pertinent data for the new 2913/14 single-chip NMOS codec/filter with built-in reference (ELECTRONIC DESIGN, Sept. 17, 1981, p. 228). This agreement gives TI more information than an earlier pact involving the 2910 codec: then, TI received some basic design information, which made it difficult to bring the part to market. The 2913 is a 20-pin synchronously clocked version; the 2914 an asynchronous version in a 24-pin DIP. In addition, the combo chips are pin-selectable to conform to both the μ -law and A-law specifications.

Multiprocessor challenges PDP-11/45 on multiuser turf . . .

A multiprocessor system with performance specifications that rival those of the PDP-11/45 for large multiuser environments and is based on the Unix operating system has been developed by Plexus Computers, Inc. (Santa Clara, CA). The P40, which is the company's first product, uses the Z8000 processor and has a main-memory capacity range of 256 kbytes to 4 Mbytes and C language capability. The company plans to add Basic and Cobol languages at a later date to its lineup of software features.

. . . while another system competes with PDP-11/34 and /44

A 68000-based computer system with a Unix-like operating system and advanced file management and performance specification that compare with those of the PDP-11/34 and /44 is intended for generalized data processing. The Universe 80, from Charles River Data Systems, Inc., (Natick, MA), features the Unos operating system, a 68000-based architecture, and a direct memory addressing capability of up to 16 Mbytes. The company will sell the software to OEM accounts and license the hardware to interested parties.

Intel, Motorola add to CMOS and HMOS 8-bit microcomputers

In an apparent effort to attract designers to their single-chip microcomputers, Intel and Motorola are expanding their 8-bit families in both CMOS and HMOS. The Chandler, AZ, division of Intel and the Austin, TX, operation of Motorola are targeting very-low-end NMOS units to compete with the high-end 4-bit chips, as well as higher-performance versions. Coming from Intel in 1982 is the i8020H, a 20-pin microcomputer with 1 kbyte of ROM, 64 bytes of RAM, 13 I/O lines, and a price tag of less than \$2. Also on the way is an HMOS upgrade of the 8021, the 8021H, which can use an external crystal as well as the passive resistor or inductor of the older version, and has a lower supply current of just 30 mA typically. At the high end, Intel has unveiled specifications for its CHMOS 80C49 version of the 8049 microcomputer. Expected to consume just 15 mA when run at 11 MHz, the 80C49 has an idle mode that draws just $500 \mu\text{A}$, and a $10\text{-}\mu\text{A}$ power-down mode. Additional microcomputers from Intel include an upgrade of the EPROM-based 8049/8747 family in HMOS II, which

LateNews

will provide 11-MHz versions, as well as reduced chip size and thus lower final cost.

Coming from Motorola on the low end will be a highly cost-effective microcomputer, the MC6804, which is derived from the existing 6805 family. In addition, Motorola has unveiled several new versions of the 6805. For communications and control applications, there is the 6805T2, a microcomputer with built-in phase-locked loop logic as well as 2.5 kbytes of ROM and 64 bytes of RAM. The MC68705U3, an EPROM-based chip, has 3776 bytes of EPROM, 112 bytes of RAM, a counter-timer and 24 I/O lines.

RAMs, micros, FETs, and CPU boards improve at Motorola

Improved 64-kbit dynamic RAMs, 16-bit microprocessors, power FETs, and CPU boards are on the way from Motorola (Austin, TX, and Phoenix, AZ). For starters, second-generation 64-k dynamic RAMs, the MCM6664A and MCM6665A, offer a guaranteed soft-error performance of 0.1% per 1000 hours, reduced row-access time, lower input capacitance, wider operating margins, and higher tolerance to V_{CC} slewing than their predecessors. They come in versions with access time ranging from 120 to 200 ns. In addition, there is a 12-MHz version of the MC68000 16-bit microprocessor.

Meanwhile, several 1000-V, n-channel power FETs, including one that can handle up to 15 A of continuous current, are coming right on the heels of a first of its kind—a FET-based asymmetrical SCR. The MCR-1000-8 offers submicrosecond switching times and a current capability of up to 15 A rms at a 600-V blocking capability. Also unveiled: TMOS p-channel power FETs that can handle up to 500 V at 2 A.

Over in microsystem products, another 16-bit CPU board is on the way: The VM-02 offers a local-bus extension that permits the user to add off-board resources such as a-d converters, I/O, real-time clocks, and other support functions. Local memory is available with up to 128 kbytes of dynamic RAM and 64 kbytes of EPROM/ROM.

High-density Winchester is SMD-transparent

An 83-Mbyte, 8-in. Winchester-disk drive using a high-resolution recording head and GCR recording techniques has a recording density of 11,500 bits/in. and a track density of 600 tracks/in. Now available from SLI industries (Woodland Hills, CA), the latest extension of the company's Cheyenne lineup of Winchester drives combines high bit density with a dedicated track-following surface to be transparent to an SMD interface.

iAPX-86 gathers military strength

The licensing by the U.S. Air Force of the instruction set and architecture of its iAPX-86 microprocessor has taken Intel Corp. (Santa Clara, CA) a step closer to military standardization of its 16-bit microprocessor. Also, Intel expects JAN certification of the processor shortly, for companies designing it into equipment for the military. For high-density requirements, users will most likely see the iAPX-86 in a leadless chip carrier in 1982. For programming, an Ada compiler will be available next year for both the iAPX-86 and the iAPX-432.

TI sees first silicon for 99000 processor

The first TMS99000 series 16-bit microprocessor has come out of Texas Instruments' ovens and is undergoing characterization at the company's Houston, TX facility. Containing about 45,000 devices, the chip is fabricated using 3- μ m lithography and is considerably smaller than the mature TMS9900 16-bit processor. Samples are expected to be available in early 1982.

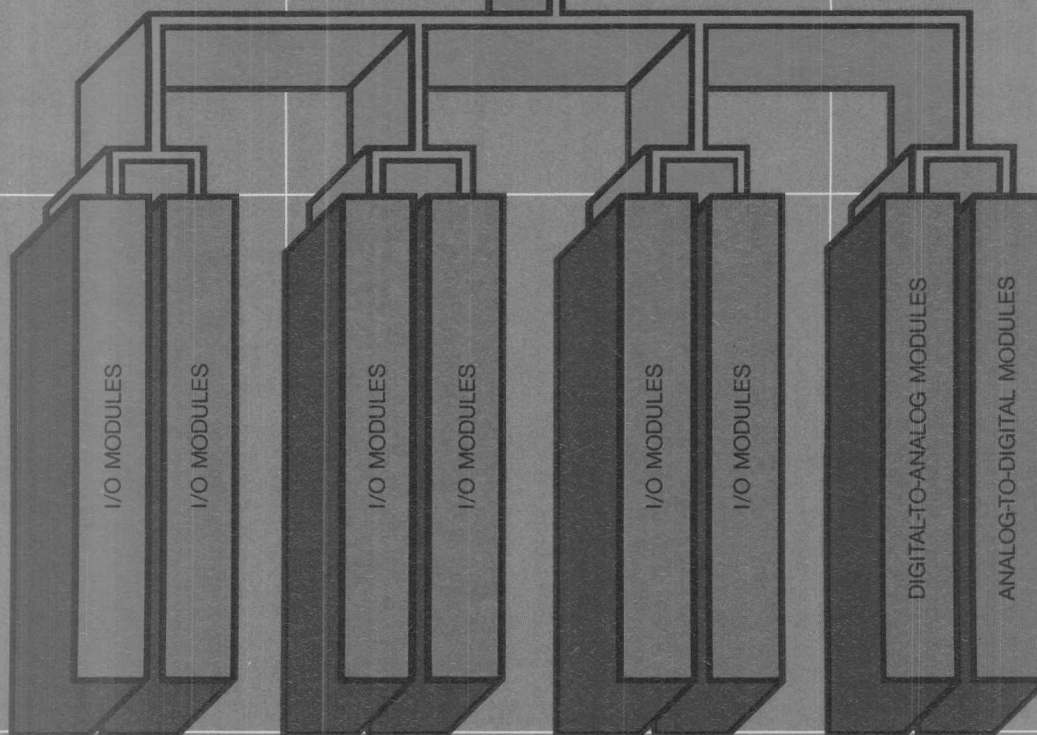
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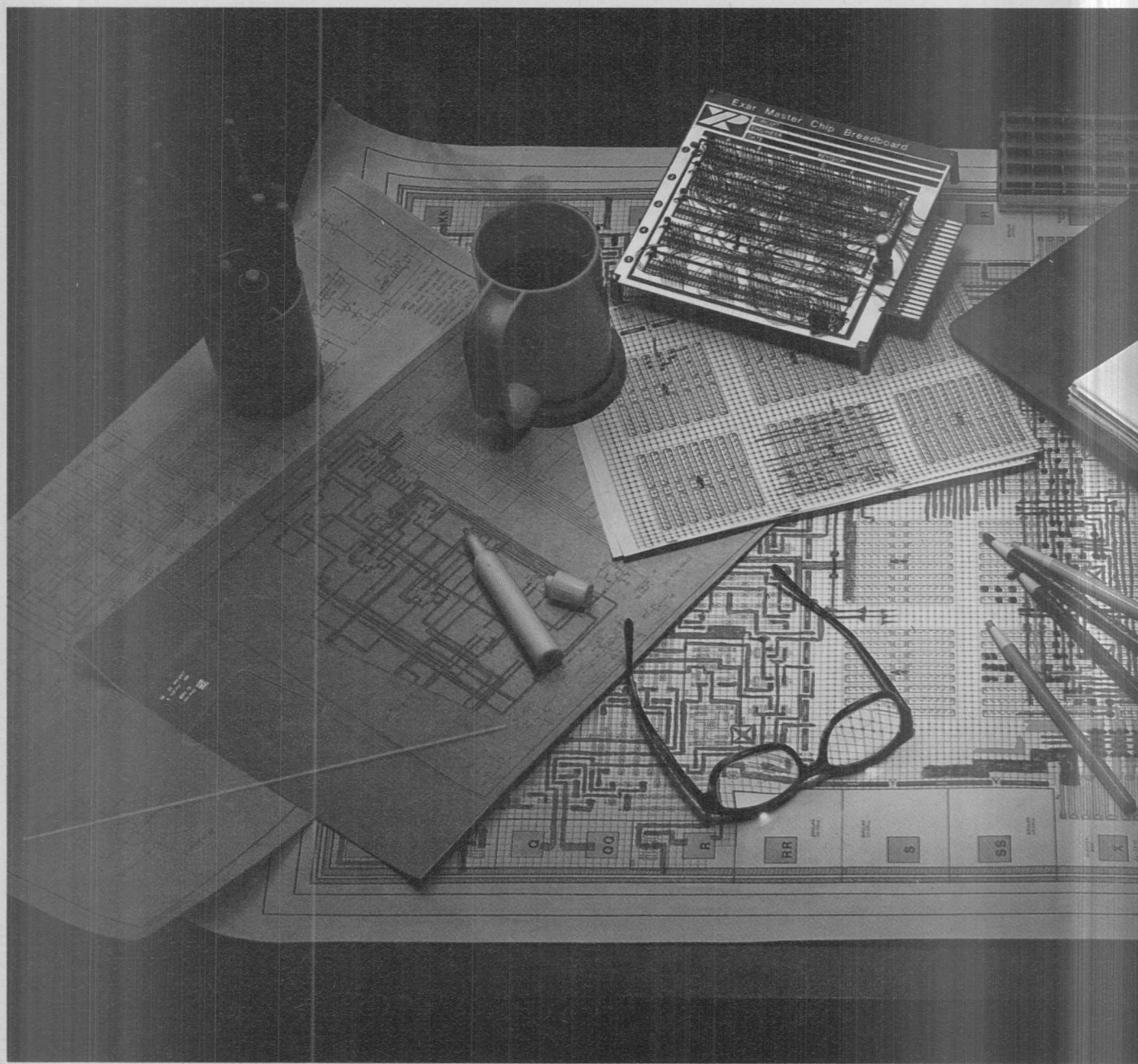
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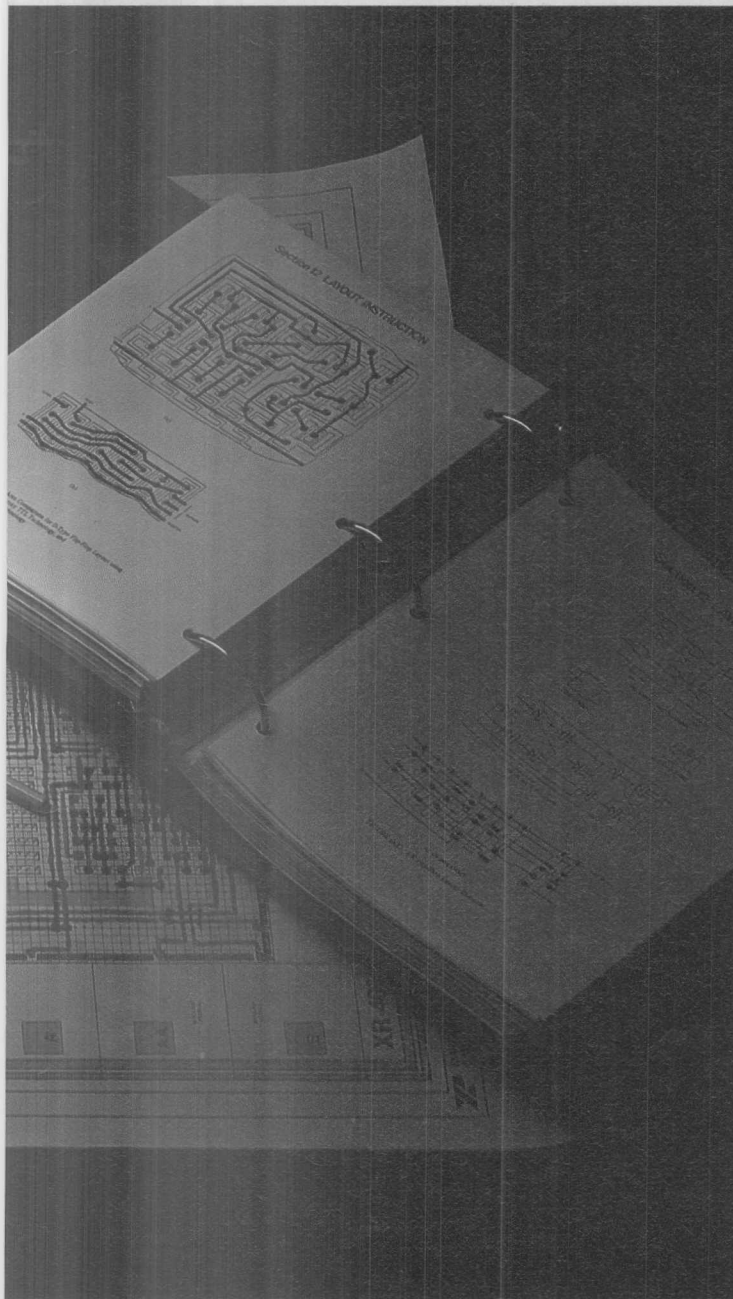


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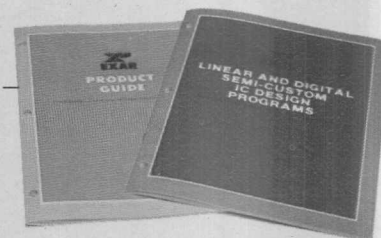
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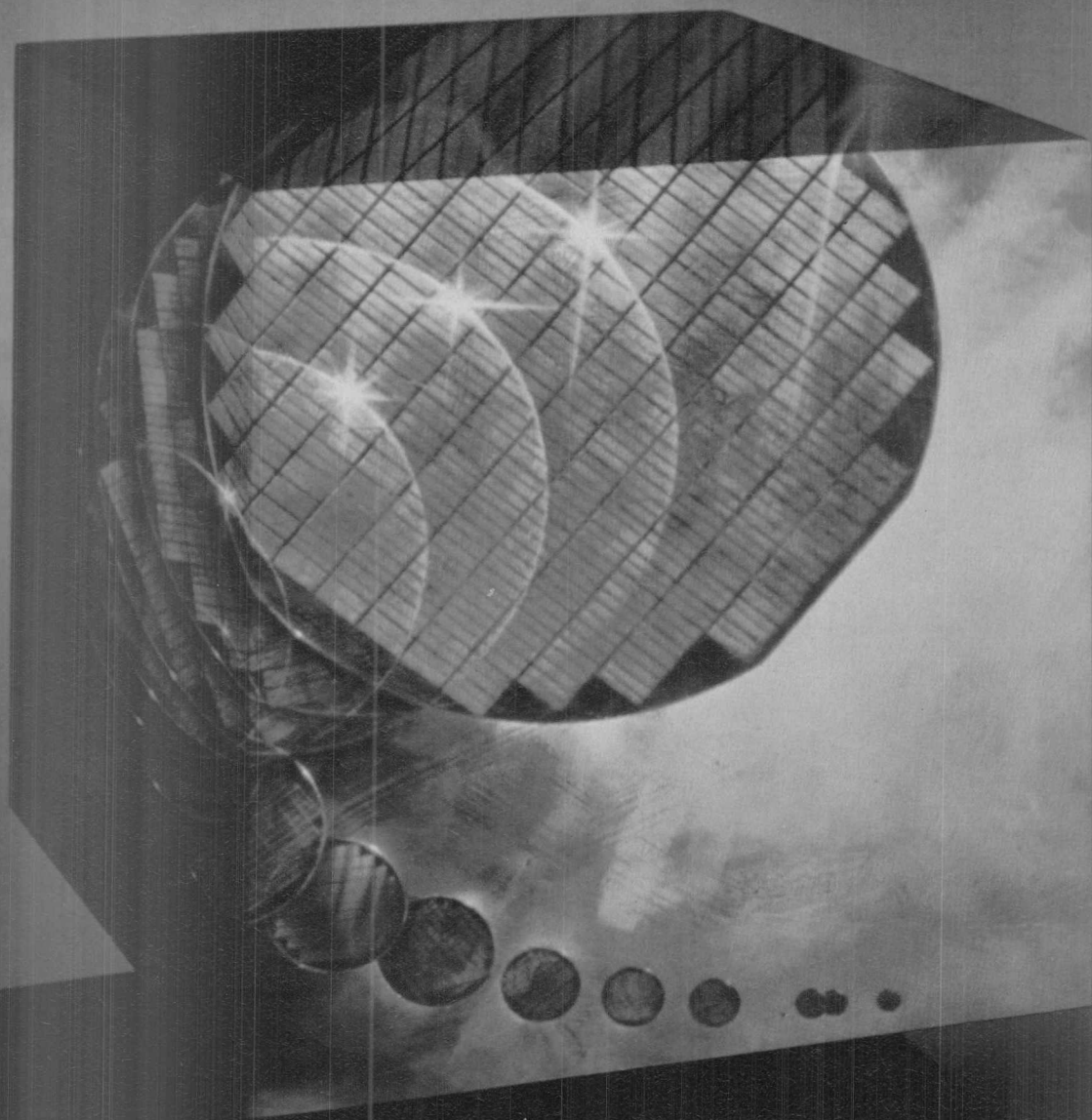
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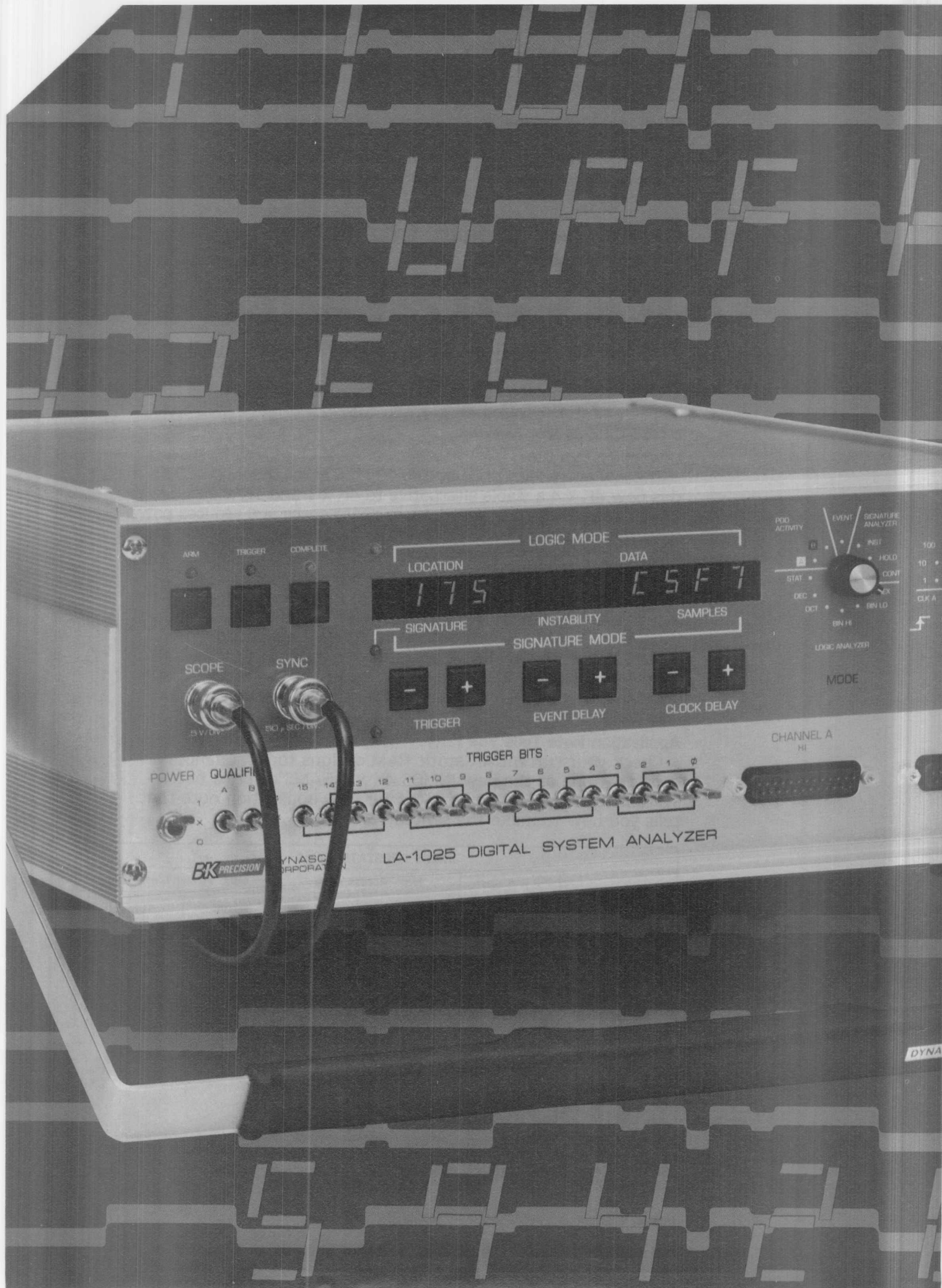
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Static RAM Family	Organization	Max. Access Time		Max. Power Dissipation	
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IMS1420-45	4K x 4	45ns	40ns	600mW	110mW
IMS1420-55	4K x 4	55ns	50ns	600mW	110mW
IMS1421-40	4K x 4	30ns	40ns	600mW	NA
IMS1421-50	4K x 4	40ns	50ns	600mW	NA
IMS1400-45	16K x 1	45ns	40ns	660mW	110mW
IMS1400-55	16K x 1	55ns	50ns	660mW	110mW



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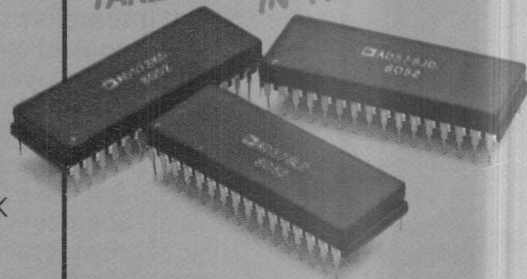
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CIRCLE 221

Development/test system expands, speeds μ P testing

Development system's software features aid pattern setup in real-time testing.

Combining a development system with a large semiconductor test system provides not only more complete test coverage for microprocessors but also speeds test time considerably. Such a hybrid system consists of the Model S-3200 semiconductor tester and the Model 8550 Microcomputer Development Lab, both from Tektronix (Beaverton, OR). The tester provides flexible device characterization while the development system brings such features as an editor, assemblers, real-time recording of bus activity, disassemblers, and debugging software.

The assemblers and the editor eliminate the need to write patterns in machine code or to develop cross-assembler software to create patterns. Patterns can be written in the mnemonics of the device under test (DUT) and converted to object code by the development system assembler. Object code is executed by the development system's emulator, thus resulting in a pattern being sent to the S-3200 pin cards as force, compare, inhibit, and mask data (see Fig.).

Pattern data are then redefined with respect to voltage levels and time. The test system varies DUT input voltages and timing to gather information about the device's operating characteristics. This information can then be displayed graphically to the test engineer.

Patterns can be easily modified or short pattern sequences cre-

ated quickly. What's more, extremely long patterns that execute in real-time can also be generated, which will shorten functional test time. Pattern data are generated in real-time, synchronously with the tester, thus eliminating pattern loads to local memory. Ordinarily, when local memory is used to hold long patterns, downloading from the disk takes much longer than the actual functional test time.

Improved debugging

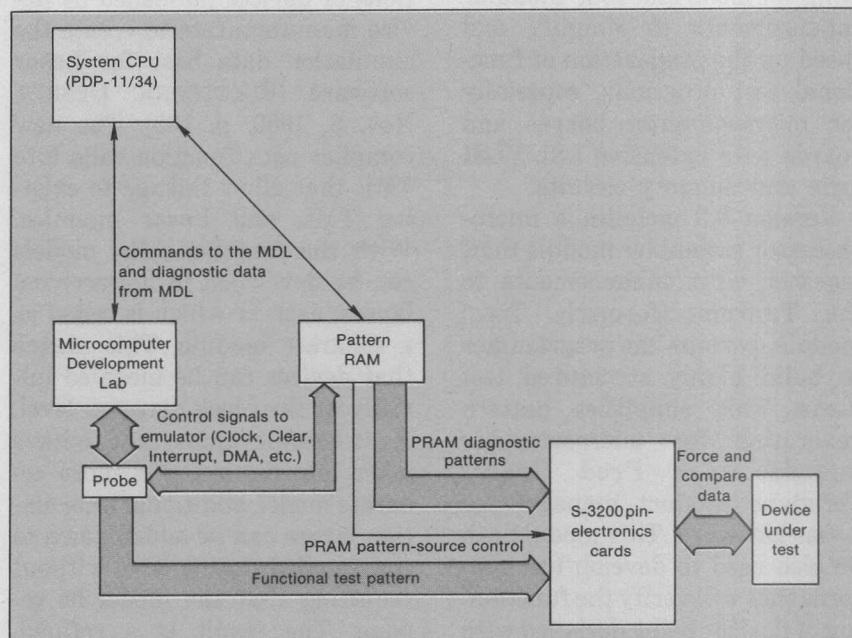
Debugging aids are also required when developing large patterns. With conventional methods, it is difficult to determine why a DUT does not randomly recognize an interrupt. With the Tektronix approach, debugging software single-steps through the pattern while interrogating the microprocessor for status at each program step. This information allows the user to verify data within the processor's internal registers, program counter, and status flags. If desired, the processor's registers, flags, or

program memory can be modified.

While the pattern program is single-stepping in a debug mode, it is not running in real time. Therefore, problems occurring only during full-speed operation will be difficult to observe. For this phase of debugging, bus data can be recorded in real time using the development system's trigger trace analyzer (TTA). Bus data in the form of address, op codes, operands, and types of memory accesses are recorded. When a user-defined word, count, time, or combination of these events occurs, the test system will "freeze" acquired bus data. This information can then be automatically disassembled into mnemonics, hexadecimal addresses, and types of bus transactions (memory read, fetch, write, etc.).

In addition, the user can probe various points to record external flags, interrupt lines, and DMA requests on the processor.

During functional testing, the tester records bus data and stops when a failure occurs. This sup-



In the Tektronix S-3200/8550 test system, the pattern RAM provides housekeeping routines for pattern control, synchronization and error monitoring.

plies the user with a record of the instructions (mnemonic listing) that preceded the DUT failure. Also, when a failure occurs, the tester can interrupt normal pattern flow and present diagnostic patterns to the DUT. These diagnostic patterns record the device's program-status register, address, general-purpose registers, and status flags. The test engineer then has a thorough diagnosis of the DUT failure, including instructions prior to failure, failure data on a pin-by-pin basis, and the DUT status immediately following failure.

Tektronix will demonstrate the S-3200/8550 at the Cherry Hill International Test Conference (Philadelphia, PA, Oct. 27-30).

Jonah McLeod

Software enhancements simplify test programs for μ C, VLSI boards

A new version of Lasar test-program-generation software from Teradyne (Boston, MA) uses "top-down" structured programming methods and four modular enhancements to simplify and speed up the preparation of functional test programs, especially for microcomputer boards and boards with extensive LSI/VLSI logic and memory circuits.

Version 5.3 includes a microprocessor assembler module that, together with enhancements to the Testcom (formerly Teco) module, permits the programmer to build highly structured test plans. This simplifies pattern generation for microcomputer boards, says Fred Grant, Teradyne product manager for Lasar software. This module can be also used to develop test patterns that will verify the functioning of devices being designed with a microprocessor development system. These patterns can, in

turn, be used by test programmers to speed the development of test programs for new devices.

The microprocessor assembler module makes all of this possible by providing a high-level language in which to generate patterns based on the assembler code of a target microprocessor. The target can be any microprocessor in Lasar's device-model library, which now contains over 3100 device models. Since the assembler module is table-driven, Grant adds, any new microprocessor, including coming 32-bit models, can be added simply by entering its assembly code.

More than 100 device models have been added to the Lasar model library since Version 5.2 was released in April, 1981. LSI families added include Z80 support families, and the Texas Instruments high-speed ALS family and its CMOS counterparts.

What's more, a new TML compiler module in Version 5.3 allows TML device models to be created from the top, down. TML is the high-level device-modeling language from Teradyne that uses the high-level functional descriptions of devices published by device manufacturers to create the simulation data base for Lasar software (ELECTRONIC DESIGN, Nov. 8, 1980, p. 103). The new compiler uses function calls into TML that allow linkage to existing TML and Lasar modules. With the function calls, models can be developed in hierarchical layers, each of which is coded as a separate module. This means that devices can be modeled initially at the block diagram level. As it becomes important to have more information or a more accurate model, additional information layers can be added down to the detailed timing level without requiring that the model be redone. The result is a refined, highly structured model.

Another new module runs off

of simulator data and functions as a sophisticated logic analyzer. Peruse allows the test programmer to probe hundreds of points on a board, and to determine the board's activity more accurately and in much greater detail than is possible with a conventional logic analyzer. Unlike a logic analyzer, which shows typically 256 board cycles, Peruse can capture all of the information on the board, including unknowns and high-impedance states, to provide an accurate representation of the board's performance. Peruse can also be used with TML to debug complex LSI/VLSI device models. To make Peruse even more useful, the speed of Lasar's simulation module, Simul, has been increased by more than 40% in Version 5.3.

A fourth new software module, Ramgen, allows a variety of RAMs to be modeled within minutes. This capability is needed, Grant says, to help test programmers deal effectively with the greatly increased amounts of memory on chips and boards.

Lasar on non-Teradyne systems

Along with the new software, Teradyne is announcing the introduction of postprocessors that will allow Lasar software to be used for the first time with board-test systems other than Teradyne's. In addition to a new postprocessor in Version 5.3 that allows functional test programs to be generated for the L200, Teradyne's latest-generation board-test system, and a postprocessor that translates Lasar software-generated test patterns into test programs for Teradyne's J283 and J325 logic test system, postprocessors are now available to translate the test patterns into Computer Automation's 4400 through 4900 series and Gen Rad's 1790 series of board-testing systems.

Edwin Hall

Intel pushes ahead with its 4-Mbit bubble memory

In the wake of a growing list of defections from the bubble-memory arena comes word from Intel that it plans to push ahead with its development of a 4-Mbit bubble-memory chip and silicon support circuits. The news from Intel comes shortly after National Semiconductor's decision to throw in the towel (ELECTRONIC DESIGN, Sept. 17, 1981, p. 32) and join Texas Instruments and Rockwell (ELECTRONIC DESIGN, June 25, 1981, p. 35) on the sidelines. Business, Intel claims, is getting too good to quit.

The 4-Mbit chip will not contain any new technology tricks, says Richmond Clover, general manager for Intel Magnetics (Santa Clara, CA). It is a straightforward permalloy design employing the folded-loop structure used in Intel's 1-Mbit device. The memory and its support chips will be virtually pin-compatible with the 1-Mbit family, and software changes will be minor—program modifications to handle the larger address space and the revised timing. In the 1-Mbit family, only positive power supplies are used, and sub-10-ms access time has been sacrificed for a wide-operating temperature range of 0 to 70°C. Access time is 40 ms, using 50-kHz cycle rate.

4-Mbit support coming too

Unlike the 1-Mbit i7110, however, the 4-Mbit bubble memory's entry into the marketplace will not be slowed by its support circuits, according to Clover, adding that all the components are expected for sampling in late 1982.

"In fact, we already have the new controller breadboarded and are internally characterizing some 4-Mbit bubble devices," Clover notes. "We are also trying

the bubble-memory subsystem components, and hope to make an announcement before the end of 1981."

From Intel's vantage point, the bubble-memory business is up and going higher. Currently, the company is shipping about 2000 units per month (including units shipped to other Intel divisions); that's three times more than last year, according to Clover. Moreover, the company has capital expansion plans that will boost production capacity to about 8000 units per month in 1982.

Describing the use of positive supplies only and the sacrifice of speed for temperature range as "right" decisions, Clover points to another decision in the same vein: Intel's plan to keep its bubble-memory business at the



Richmond G. Clover has been general manager of Intel Magnetics since April, 1980. Before that, he was the division's engineering manager, responsible for directing device designs, interface-electronics development, and device packaging. Before joining Intel in September, 1977, Clover was a department manager for five years at the Hewlett-Packard Corporate Laboratories (Palo Alto, CA). Clover holds a doctorate in solid-state magnetism from Yale University.

competition with potential board-level customers as well as much of the overhead associated with board-level systems.

In addition, Clover believes that Intel took a bold step in 1980 when it published a projected price curve for bubble systems that predicted production prices out to 1982. So far, the company has lived up to its promises.

In August, 1981, Intel met the first milestone and cut prices of the BPK72 1-Mbit system to \$600 (in 5000-piece quantities). And by August, 1982, the price is guaranteed to be less than \$300 (in 25,000-piece quantities).

When the price was up around \$1000, only systems that had to contend with harsh environments could justify the high cost. As the price drops, though, the telecommunications and portable equipment market will open up, says Clover. "And, when the price drops under \$300, we think the office and business equipment markets will show some large commitments to bubbles."

Small Winchester are fair game

The entry of bubbles into the "corporate" market will directly counter the problems of the high initial costs of small Winchester-type disk drives, Clover contends: In many cases, the disks offer too much storage capacity, are too bulky, and can't be easily transported.

Another attraction, Clover believes, is the variety Intel offers to system designers. This includes the Plug-A-Bubble cartridge and holder system which permits very portable nonvolatile storage in 128-kbyte cartridges; and two memory boards—the Multibus-compatible iSBC 254, which can hold up to 4 Mbits, and the iSBX-251 multimodule, which uses the popular SBX connector to add 128 kbytes to any SBC.

Dave Bursky

Chip-carrier/socket scheme simplifies ROM mounting, repair

A plug-in chip-carrier/socket packaging scheme for ROMs, jointly developed by Hewlett-Packard and 3M and being used in HP's Model 9835 desktop computer system, not only simplifies packaging but also permits the customer to update or repair a system without a service call.

The 64-kbit ROMs, which contain the 9835's operating system and standard routines, are mounted on ceramic chip carriers sandwiched in small plastic housings. They then plug into sockets in a thin removable drawer. Fitted with a standard card-edge connector, the drawer slides into the side of the desktop computer.

The chip carriers, which are supplied by 3M, have single-layer metallization and are made of 94% alumina. In original 9835 prototypes, ROMs were mounted on small glass/epoxy circuit boards. Malfunctions stemming from moisture and outgassing from the boards led to a switch to a ceramic substrate before the system was formally introduced, reports George Winski, production engineer for HP in Ft. Collins, CO.

Even the substrate has been

changed. Originally, a 0.062-in. substrate had been specified as a direct replacement for the glass/epoxy board, and was sized to fit the plastic housing. However, the housing has since been retooled, allowing use of a thinner (0.02-in.) and more economical ceramic chip carrier with no change in performance. The assembled carrier and housings are 11/16 in. long, 3/4 in. wide, and 3/8 in. high.

Chip carriers are ordered from 3M in arrays of six, and separated after lead bonding and encapsulating. This reduces production handling by a factor of six for bonding and encapsulating. The chip arrays are scored by 3M before firing, and thus snap apart easily.

ROMs eject easily

ROM sockets are made with a small plastic button under the center of the plug-in unit. Pushing the button from the bottom easily ejects the memory. Contact pins are gold-plated beryllium copper with a folded design that keeps constant, even pressure to maintain electrical contact and hold the ROM in place.

From each plated hole on the ceramic chip carrier, a conductive trace leads to a pad near the die, where it is connected to the 64-k ROM chip with a gold wire bond. A small ceramic cap covers and

seals the IC from exposure to contaminants and from physical damage.

The manufacturing process for ROM devices begins by fastening IC dice on the 3M ceramic chip-carrier die pad. Then the carrier is placed in a fixture on one of HP's automatic lead bonders, and the ROM chip is connected to the peripheral traces with gold wire bonds, explains HP assembly manager John Mahorney.

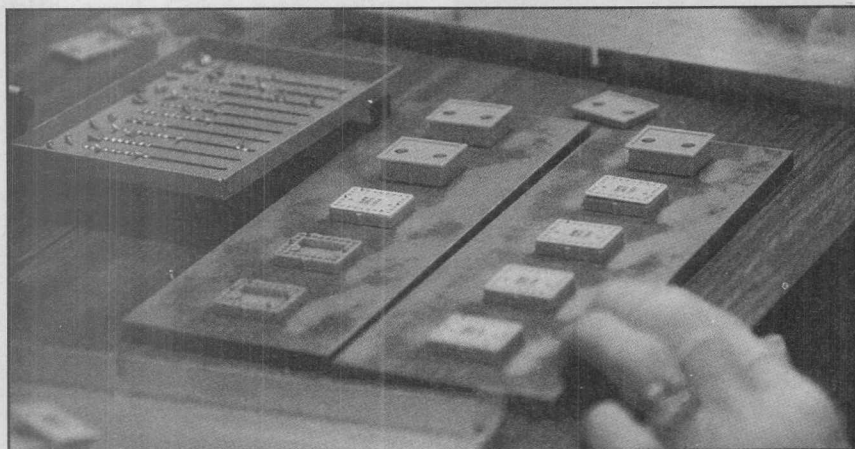
Next, the circuits are fitted with a ceramic lid having a small bleed opening at the top. The lids are secured to the carrier by a heat-activated epoxy resin. Lidded chips are then placed in a vacuum chamber and flooded with nitrogen to exclude air and any contamination. While the chip carrier is in the nitrogen atmosphere, the bleed opening on the top is sealed with a dot of epoxy to contain the nitrogen.

Each chip is then burned-in, using a high-temperature reverse-bias program, to eliminate marginal units. After each chip has been operated under load conditions, it is tested for conformance to part specifications.

"HP has found that faulty units will generally fail within a short period of time, and once this test has been completed, the confidence level is high for those memory devices that pass," Mahorney notes.

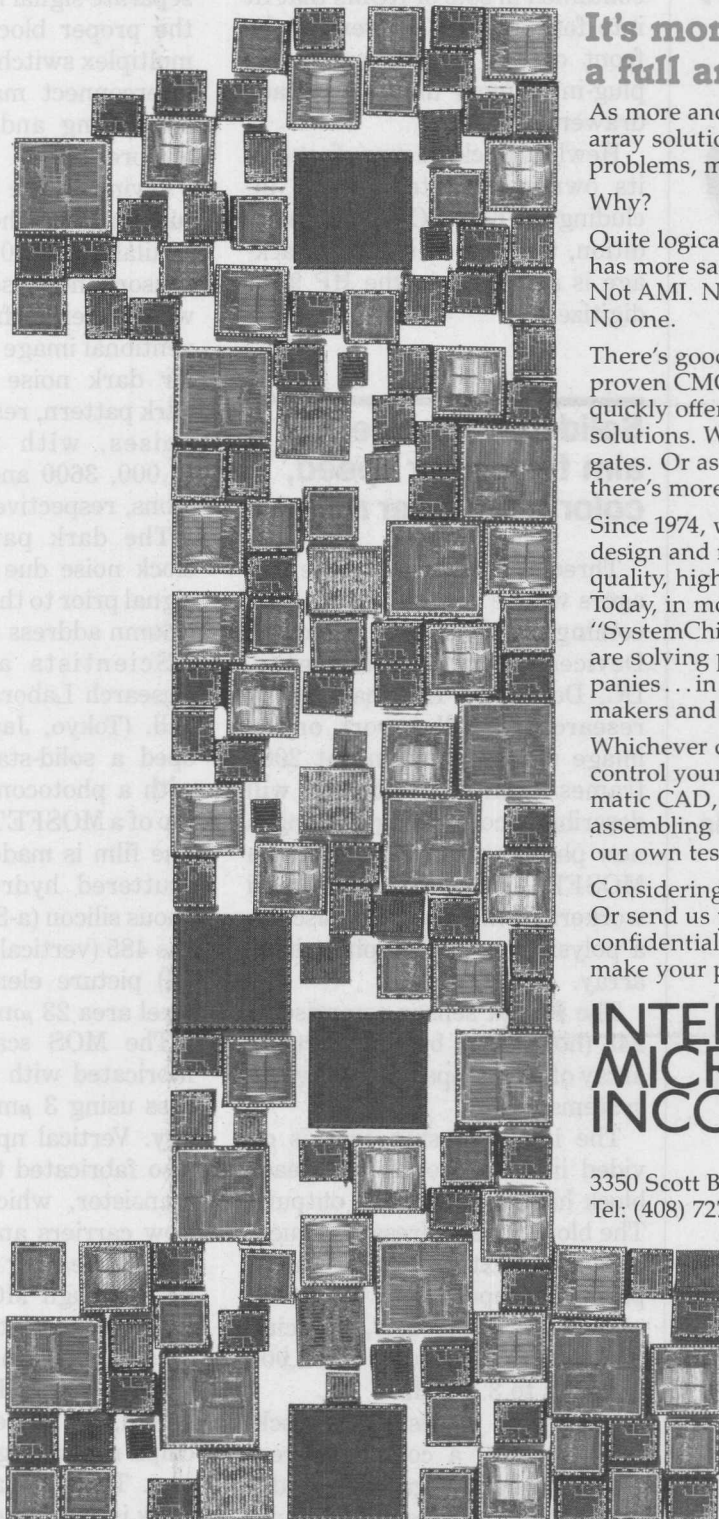
Finally, the tested and approved ceramic chip carriers are placed in the two-part plastic housing. Each ceramic carrier has two holes in its surface to accept screws that hold the package together. Raised ridges on the edges of the housing key it to the ROM socket. At this point, the ROMs are ready for final assembly in the system.

Nine ROM-based enhancement packages for the 9835 are offered, ranging from data communications to assembly language to mass-storage control.



After the chip carriers have been tested, the completed assemblies are ready for mounting in plastic housings.

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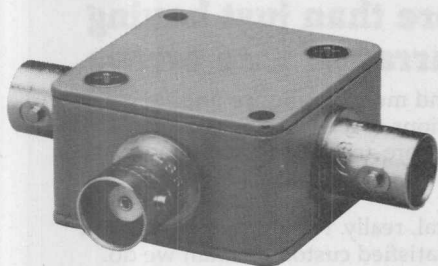
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Total range		7.0	8.5
ISOLATION, dB			
		TYP.	MIN.
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	LO-IF	45	40
10-500 MHz	LO-RF	40	25
	LO-IF	35	25
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Each package may be ordered, installed, and put into operation entirely by the customer. Optional operating-system enhancements, such as additional programming statements and commands, are contained in sets of ROMs that fit into four smaller drawers at the front of the 9835. Four or six plug-in memory units fit in each drawer.

Hewlett-Packard manufactures its own solid-state devices, including the 64-k ROM chip. In addition, the plug-in memory package is also used in the HP 9874 digitizer.

Solid-state imagers aim for higher speed, color, and lower noise

Three unusual solid-state imagers will be described at the upcoming International Electron Devices Meeting (Washington, DC, Dec. 7-9). Eastman Kodak researchers will report on an image sensor operating at 2000 frames/s, Hitachi workers will describe a color imager using a new photoconductive film atop a MOSFET scanning array, and workers from Xerox will describe a polysilicon isolated photodiode array.

The Kodak sensor comprises a 248 (horizontal) by 192 (vertical) array of photocapacitors for video systems.

The image-sensing area is divided into six blocks, with each block having 32 parallel outputs. The blocks are addressed sequentially by an external clock. The 32 parallel outputs per block are sensed simultaneously, reducing the analog data rate at 2,000 frames/s to 3.1 MHz.

Each pixel consists of a block-address gate, a column-address gate, a dc barrier gate, and a diffusion area contacted by an aluminum signal line.

A dynamic shift register scans the columns. When both block and column gates are addressed, the photogenerated charge is transferred onto the signal line. Signals are sensed off-chip via 32 separate signal lines connected to the proper block by 192 output multiplex switches and a 192 x 32 interconnect matrix. Results of addressing and readout speeds are presented.

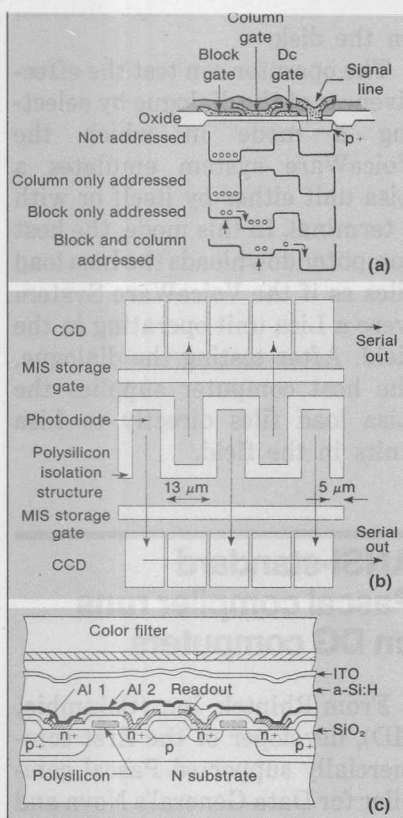
Owing to the parallel architecture and the short element time available at 2000 frames/s the sensor's noise sources are somewhat different from those in conventional image sensors. The major dark noise sources include dark pattern, reset, and amplifier noises, with magnitudes of 17,000, 3600 and 5700 rms electrons, respectively.

The dark pattern is largely clock noise due to sampling the signal prior to the full decay of the column address transient.

Scientists at the Central Research Laboratory of Hitachi, Ltd. (Tokyo, Japan) have developed a solid-state color imager with a photoconductive layer on top of a MOSFET scanning array. The film is made with reactively sputtered hydrogenated amorphous silicon (a-Si:H). The imager has 485 (vertical) x 384 (horizontal) picture elements with each pixel area 23 μm x 13.5 μm .

The MOS scanning circuit is fabricated with the LOCOS process using 3 μm n-MOS technology. Vertical npn structures are also fabricated to form a bipolar transistor, which absorbs overflow carriers and prevents them from appearing on the signal-out line through MOSFET. The p+ region beneath the n+ region increases junction capacitance.

After the LSI process is completed, the wafer is scribed into chips measuring 8.5 mm x 10.0 mm. Then, an a-Si:H film 5 μm thick is deposited on the chip with rf sputtering, masking the areas



A Kodak imager (a) transfers charges to a signal line when a block and column are addressed. A Xerox imager (b) uses narrow polysilicon strip to reduce noise. A Hitachi imager (c) uses amorphous silicon as a photoconductive layer on MOS.

other than the imaging area. Finally, on top of a-Si:H film, a transparent electrode of ITO is deposited by the sputtering.

The a-Si:H film is doped with nitrogen to improve electron mobility and to lower the operating voltage of the film. (Photocurrent saturates at as low as 5 V because of the nitrogen doping.) Dark current remains at a low level; 30 pA/cm², even at a voltage level well above the saturation. This low level of dark current is attributable to the Schottky barrier formed at the interface of a-Si:H and the upper electrode.

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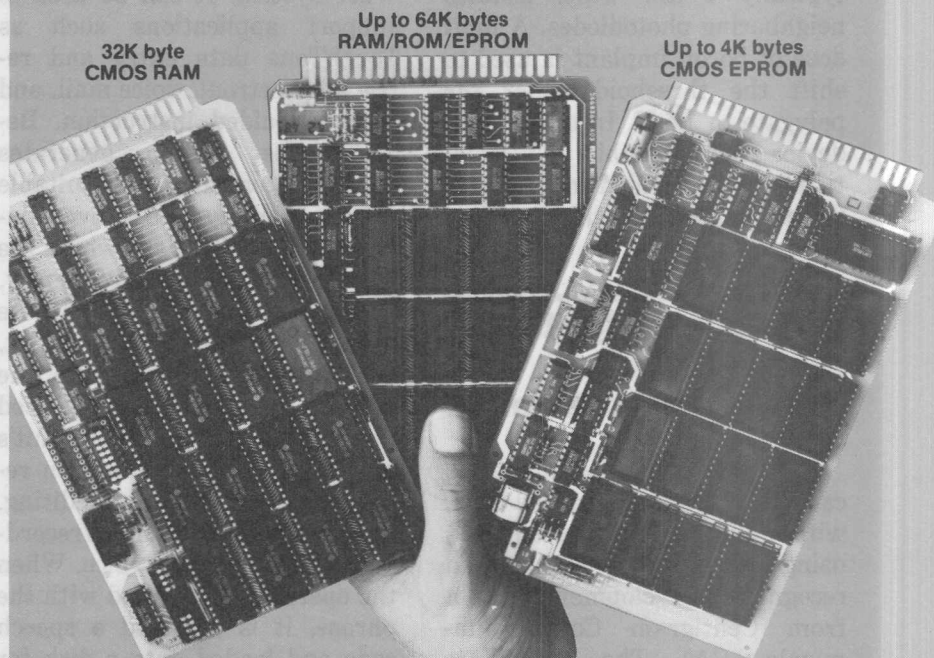
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ity is 40 nA/lux (3200 K) and the saturation current is 1.6 μ A at the surface illumination of 130 lux.

Researchers at the Xerox Microelectronics Center (El Segundo, CA) have developed a sensor that uses a narrow string of polysilicon in place of the field implant and field oxide isolation, which often produce leakage current that increases noise and signal nonuniformity. This polysilicon isolation structure has a positive threshold of +1.5V and is normally grounded in operation. By eliminating the field implant and field oxide, the defect density in the sensor area is significantly reduced.

This sensor structure has been successfully implemented in a 1744-element photodiode array imager with several other features, such as the on-chip clocks, sample-and-hold, and black reference. This design, process and performance of the poly isolation imager will be discussed with emphasis on reduction of photoreponse nonuniformity down to only $\pm 1\%$.

A narrow string of polysilicon, typically 5 μ m wide, isolates neighboring photodiodes. A light dose of boron implant is used to shift the threshold under the polygate to 1.5 V. In the normal device operation this poly isolation gate is grounded and provides the required channel isolation.

Synthesis/recognition system programs digitized vocabularies

Digitized voice vocabularies can be programmed in real time, with unlimited storage on disk, using a speech-synthesis and recognition development system from Centigram Corp. (Sunnyvale, CA). The VoiceWare system produces high-quality voice at rates as low as 4800 bits/s

using parametric waveform coding, Centigram's proprietary process for voice digitization. The low bit rate enables the system to store large quantities of data on disk, reducing the cost of storage.

The basic \$25,000 VoiceWare system includes an intelligent CRT terminal incorporating a CPU with 64 kbytes of RAM, four RS-232-C serial interface ports with local and self-testing, dual 500-kbyte 5 $\frac{1}{4}$ -in. floppy disks for voice and data storage, a voice digitizer with microphone input, and a Lisa speech synthesizer with speaker output. The Lisa synthesizer is supplied in a Multibus format and is housed within the VoiceWare System.

Options include a Mike speech-recognition system, a Mike application development support software package; a 5-Mbyte Winchester disk, a TouchTone inquiry Lisa unit, and custom hardware interfaces. Additional software enhancements will be announced as they become available, according to Centigram.

Voice applications can be custom-designed with the VoiceWare system. It can be used to support applications such as TouchTone data entry and retrieval, electronic voice mail, and computer-aided instruction. Because the system generates speech in real time, it is suitable for developing interactive dialogue and applications where the speech data changes frequently.

While the system is off line, the operator works from a script, speaking each phrase into the microphone. The voice is digitized and stored in the Lisa unit's memory. The phrase is then recalled for reviewing and editing. The voice will sound like a recording of the operator's voice. When the operator is satisfied with the phrase, it is assigned a speech code and loaded onto a disk for permanent storage. The host CPU uses the speech code to access the

phrase from its storage location on the disk.

The operator can test the effectiveness of the dialogue by selecting a mode in which the VoiceWare system emulates a Lisa unit either by itself or with a terminal. In this mode, the host computer downloads the Lisa load files as if the VoiceWare System were a Lisa unit operating in the field. After testing the dialogue, the host computer supplies the Lisa load files directly to Lisa units in the field.

ANSI-standard Pascal compiler runs on DG computers

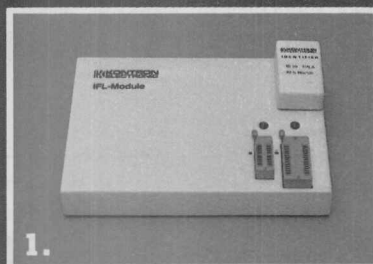
From Rhintek, Inc. (Columbia, MD), developer of the first commercially supported Pascal compiler for Data General's Nova and Eclipse computers, comes a Pascal compiler for Data General computers. It has been designed to conform to the proposed ANSI standard.

The compiler has 117 error messages, and compiles at over 400 lines/min. Generated code executes twice as fast as the code produced by the Data General Fortran IV compiler, according to Rhintek.

The executable code is automatically linked to the Pascal support library by the final pass of the compiler. This creates an executable file directly, saving the considerable time normally required to perform the linking operation manually. The multi-pass compiler can compile 4000-line programs in less than 32 kwords of memory.

Introductory prices are \$2000 for the RDOS version, \$2500 for the AOS version, and \$4000 for both, including one year of support and maintenance. Source code will be available at additional cost.

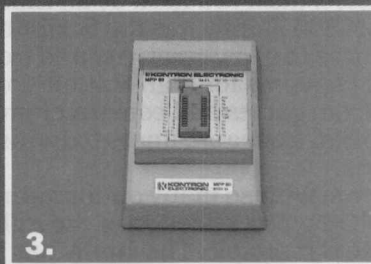
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The table suggests how easy the family is to understand and demonstrates how easy it is to select the MCU that's practically tailored to your needs.

M6805 FAMILY SINGLE-CHIP, 8-BIT HMOS MCUs

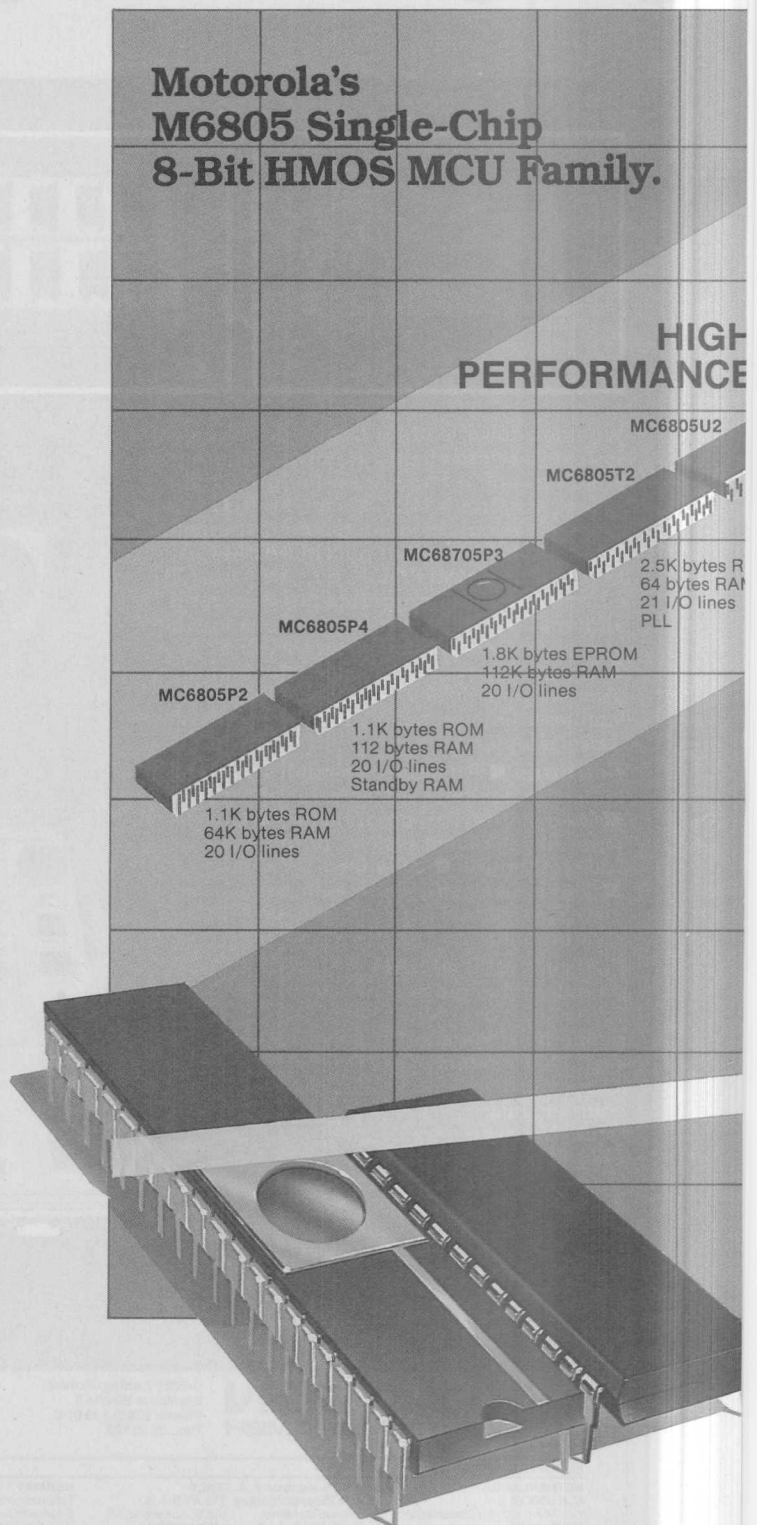
	MC6805P2	MC6805P4	MC68705P3	MC6805T2	MC6805U2	MC68705U3	MC6805R2	MC68705R3
ROM (bytes)	1K	1K		2.5K	2K		2K	
EPROM (bytes)			1.8K			3.8K		3.8K
RAM (bytes)	64	112	112	64	64	112	64	112
I/O Pins								
Input					8	8	2-5	2-5
Program Bidirectional	20	20	20	19	24	24	24	24
Special				2			1-4 Anal.	1-4 Anal.
8-bit A/D							yes	yes
Frequency Synth.				yes				
I/O Drive Capability	12 TTL/CMOS 8 LED	12 TTL/CMOS 8 LED	11 TTL/CMOS 8 LED	11 TTL/CMOS 8 LED	16 TTL/CMOS 8 LED	16 TTL/CMOS 8 LED	16 TTL/CMOS 8 LED	16 TTL/CMOS 8 LED
Timer Interrupts	1	1	1	1	2	2	2	2
Self Check	yes	yes		yes	yes		yes	
Bootstrap			yes			yes		yes
PLL				yes				

Powerful instructions and a large complement of addressing modes are a programmer's delight. The similarity and compatibility between M6800 and M6805 make transition from one to the other a simple matter. Simplicity, compatibility and the economy of programming ease movement among Motorola MCUs and reduce system design costs.

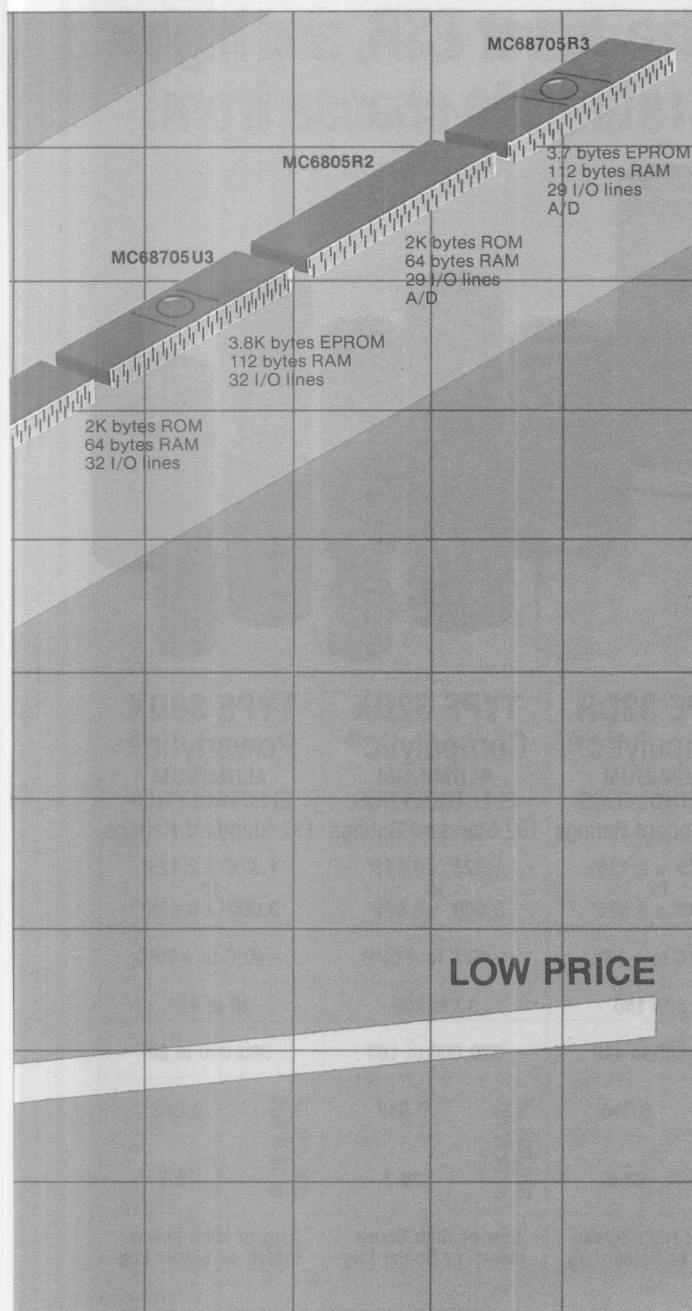
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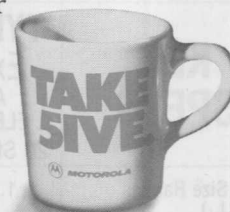
by simple variations of the MEX6805 emulator system. Each is fully compatible with both the MC6800 and MC6809-based EXORciser® and EXORterm™ development systems.

The MEX6805 provides real-time emulation capability and a complete memory map. Debugging features include trace, display of registers and memory, single-step capability, plus halt-on-address and break points. Software support is also provided on the low-cost EXORset™ development system. An inexpensive PROM Programmer supports the MC68705 MCUs.

For designers of portable, battery, battery back-up and other low-power systems, the broad M6805 Family also includes fully-static CMOS single-chip MCUs. Motorola also supplies the MC146818 real-time clock for use with most multiplexed-bus processors.

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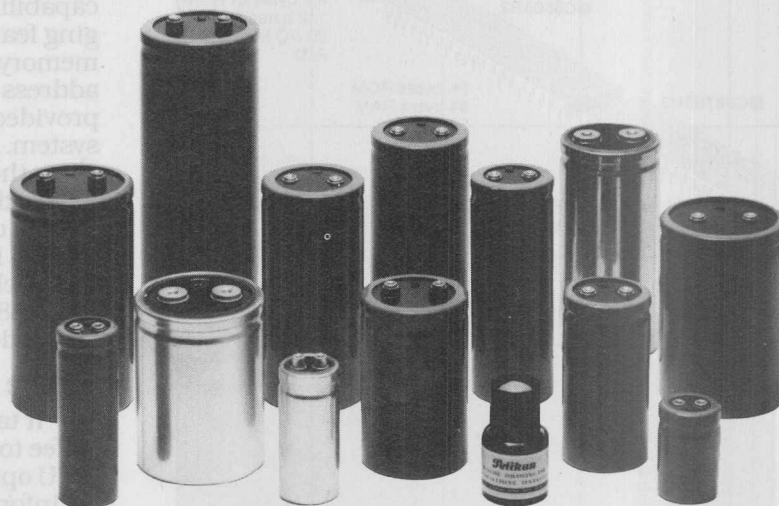
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Operating Temperature Range	-55°C to +85°C	-55°C to +85°C	-40°C to +85°C	-40°C to +85°C	-40°C to +85°C
WVDC Range	200 and 250	5 to 250	7.5 to 150	10 to 200	10 to 450
Capacitance Range (μF)	7400 to 260*	270,000 to 150	310,000 to 410	320,000 to 180	390,000 to 80
Max. ESR (ohms) at 120 Hz	7400 μF at 200 WVDC 0.020	270,000 μF at 5 WVDC 0.0062	310,000 μF at 7.5 WVDC 0.010	320,000 μF at 10 WVDC 0.017	390,000 μF at 10 WVDC 0.012
Max. RMS Ripple Current (Amperes) at 120 Hz and 85°C	20.0	36.0	23.9	18.3	15.3
Terminal Styles	Low Screw-Insert	Low or High Screw-Insert, or High Current	Low or High Screw-Insert, or Solder Lug	Low or High Screw-Insert, or Solder Lug	Low or High Screw-Insert, or Solder Lug

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Brock pushes Japanese harder to open up their markets

A soaring United States trade deficit with Japan, bolstered by still growing imports of electronic equipment, steel, and textiles, has led U.S. Special Trade Representative William Brock to demand in Tokyo that Japanese markets be opened "much wider" or the Reagan administration will "face substantial pressure" at home to close American markets. His remarks came right after he revealed that this country's trade deficit with Japan will balloon almost 50% this year to close to \$15 billion.

Brock added that the matter goes beyond trade and could affect diplomatic relations between the two countries. If the current "reservoir of good will generated by admiration for Japanese skills is to be tapped for the benefit of our overall relationship," Brock said, "Japan must overcome the widespread perception in America that it does not play fairly in the international trading arena." He made his statements at the fifth Shimoda Conference, a high-level private gathering of Japanese and American leaders, where trade issues seemed to dominate this year.

The Japanese government has blamed the growing trade deficit on the high interest rates in the U.S., which have kept the dollar strong—and American exports more costly—and the yen undervalued.

"The United States complains, but at the same time you pursue a policy of benign neglect in terms of international exchange rates," said Naohiro Amaya, special adviser to the Minister of International Trade and Industry.

Still, Japanese trade officials appear to be taking the deficit issue more seriously than they had before. The Japan Foreign Trade Council, a business group, recently called for quicker government action to increase imports, and the cabinet ministers are reportedly ready this month to review ways to open up their markets further to U.S. companies.

Brock, who knows well that remarks such as his have been made and then forgotten by the world community many times, summed up his job recently when he said: "They've got a lot of liberalizing to do here. We've got to keep the pressure on."

NAS says solar-energy satellites are not needed

An ambitious proposal to launch 60 satellites to convert the sun's rays into usable energy that could be beamed to earth has been found to be unnecessary at any cost by a study conducted at the National Academy of Sciences for the Department of Energy.

The DOE had envisioned orbiting satellites laced with silicon photovoltaic cells to collect the sun's energy. After being converted into microwaves, the energy would have been transmitted to antennas at receiving sites around the country and then placed on the electric power grid.

But after looking over the project for two years, the NAS found that higher than anticipated costs of space transportation, silicon cells, and satellites would send the price of a kilowatt-hour of electricity to \$10,000, a substantial increase from the DOE's forecast of \$4000/kWh.

The researchers also found that the amount of future energy expected from coal, nuclear,

and earthbound solar sources will more than offset the need for the solar satellites. "We just found that there wasn't a crying need anymore to go into orbit," says John Richardson, NAS staff director for the study. The DOE, which originally sponsored the project in 1979, when the nation's policy was to scurry for new energy sources, had been budgeted \$20 million through 1981 to evaluate the idea.

However, perhaps the biggest obstacle to the plan—especially in the country's current economic scrape—is the kind of domestic reaction full-fledged building would evoke. The price tag was slated at \$3 trillion, with a payoff time of 20 to 30 years before the first kilowatt-hour's worth of energy could be beamed from space.

Then, Richardson says, there's the public's often protective environmental attitudes, especially when a project will affect their backyards. "We asked ourselves, 'Are people

WashingtonReport

going to stand for microwaves pouring out of space and antenna farms 10 miles long and 8 miles wide near their towns?"

The DOE has not requested renewed funding for the solar satellite plan. But

Richardson adds that the researchers were not completely negative about the project: "Even with all its faults, I just want to say that technologically we could probably have built it. That's not the problem."

Military IC sales to double by 1985, study predicts

Spurred by the Pentagon's Very High Speed Integrated Circuits (VHSIC) program, the U.S. military semiconductor market is expected to more than double over the next five years, according to a report just released by Frost & Sullivan, Inc., a New York market research firm.

Factory shipments of ICs for defense applications will approach \$1.64 billion by 1985 from a current \$761 million this year, the study says. With total defense electronic outlays forecast to increase from \$20 billion to \$29.5 billion over that same period, semiconductor content in defense electronics systems will expand from the current 3.8% to 5.54%.

The fastest growing segments, the firm predicts, will be memories, microprocessors, and field-effect transistors. In terms of

technologies, the study says that silicon will remain the preeminent material for ICs over the five-year period, but gallium arsenide will probably pose a serious challenge between 1985 and 1990 because of its potential for faster speed and operation at higher temperature.

Despite the Pentagon's increased purchases, the military share of overall domestic chip sales through 1985 will actually shrink from 8.9% to 7.4% as the nation's market grows from \$8.52 billion to \$22.1 billion.

Currently, the top five suppliers of military semiconductors are, according to Frost & Sullivan, Texas Instruments (\$110 million), Motorola (\$90 million), National Semiconductor (\$52 million), Signetics (\$46 million), and Fairchild (\$43 million).

Personal computer makers prepare for RFI compliance

New Federal Communications Commission regulations that require internal computer design changes to reduce radio frequency interference go into effect this week for all new machines. Computer makers are responding with grudging support.

The rules, which were adopted in 1979, set up a broad outline of how much radiated energy and conducted energy may be emitted from computing devices, which are divided into business and industrial machines (Class A) and personal and home equipment (Class B). Jan. 1 was the compliance date for most already manufactured pieces of equipment, and Oct. 1 is the date for new items.

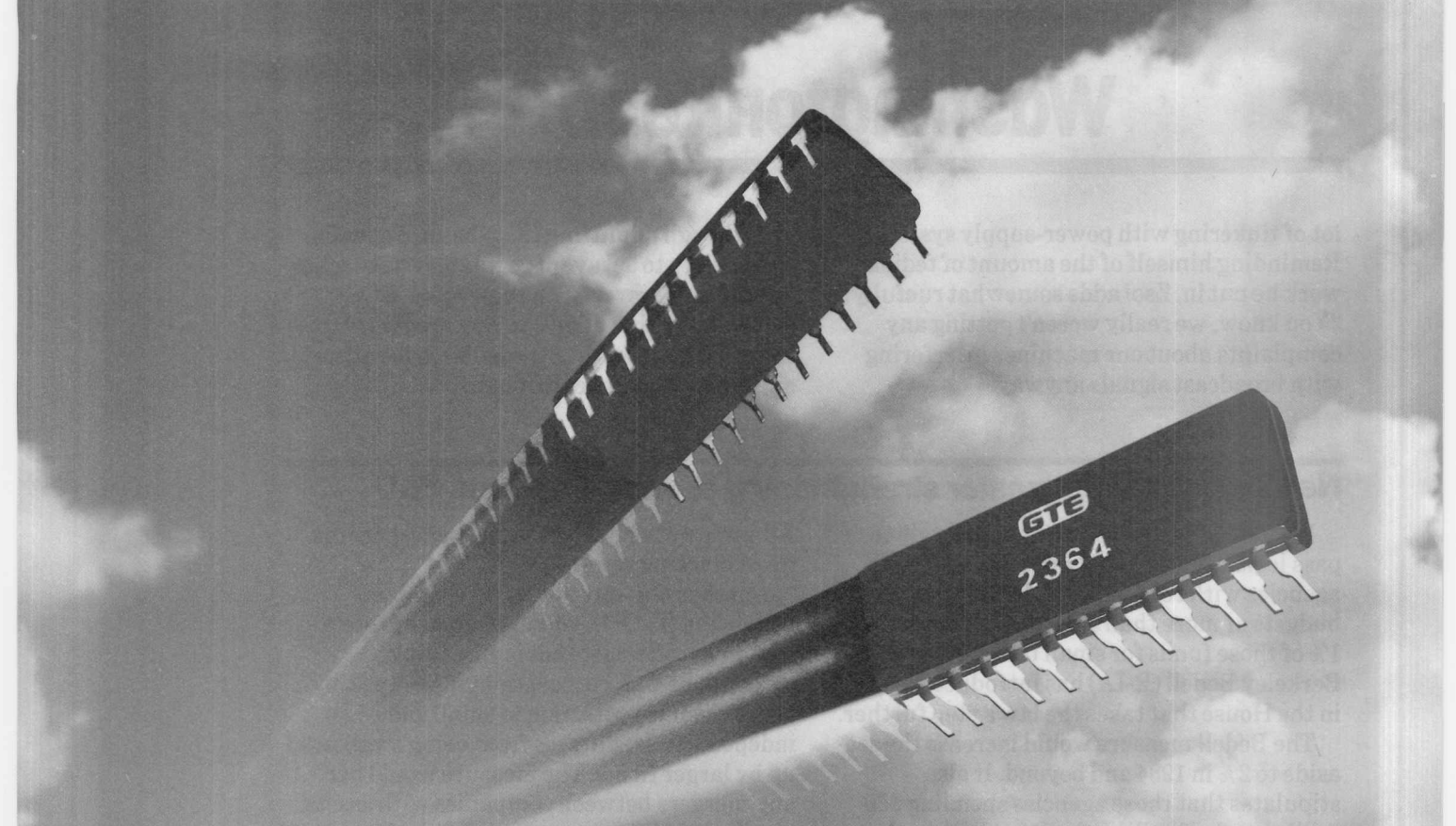
"These requirements are long overdue," says George R. Ufen, an RFI expert who plans to work with corporations to meet the FCC standards. "There is certainly interference pollution out there now. Electronic equipment these days is beginning to interfere with such common and necessary things as

electrocardiograms. The reaction to the FCC from many in the electronics community is 'help!' But a company that has always followed good engineering practices will have no trouble meeting the guidelines," suggests Ufen.

Officials at Apple Computer, Inc. (Cupertino, CA), who had to retrofit their two-year-old Apple II personal computer by January 1 of this year, see the new rules as a sadly necessary by-product of the electronics boom.

"With all the equipment being made today," John Zsoi, an Apple II engineering team leader, says, "there's always the possibility of somebody dumping a whole lot of equipment on the market without care for proper design and interference needs just to make a quick buck. It's like the CB craze. I guess the FCC just had to brake it a little."

It took six to nine months to rework the Apple II, with a lot of trial and error and a



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lot of tinkering with power-supply systems. Reminding himself of the amount of tedious work he put in, Zsoi adds somewhat ruefully: "You know, we really weren't getting any complaints about our machines interfering with broadcast signals anyway."

Although admitting that they are opening themselves to a wave of regulatory headaches and controversy over the new rules, FCC officials say that adoption was necessary to avoid a future world crowded with broadcast signals that can't get through.

New bill proposes greater strengthening of small-business R&D

While the Senate appears about ready to pass legislation that would require federal agencies with research and development budgets of more than \$100 million to earmark 1% of those funds for small businesses, Rep. Berkeley Bedell (R-IA) has introduced a bill in the House that takes the law a step further.

The Bedell measure would increase the set-aside to 2% in 1984 and beyond. It also stipulates that those agencies spending \$20 million to \$100 million for R&D, although not required to set aside funds, would have to develop guidelines for bringing in more small-business research contractors. Finally, it includes a monitoring provision that aims at ensuring compliance: Each agency would have to report annually to the Small Business

Administration, which would be responsible for overseeing the program.

Another bill, introduced by Rep. John Seiberling (D-OH), which attempts to stem the "urge to merge" that is spreading throughout U.S. corporations, offers as a by-product some protection to small and independent businesses from being swallowed up by larger firms. The measure would bar any mergers between companies with assets totaling \$2 billion or more and make it tougher for firms with assets of \$350 million to \$2 billion to merge with similar-sized companies. The law would allow such companies to buy one another only if they can prove that the merger will "enhance competition or result in substantial efficiencies."

Commerce clarifies bidding for NTT contracts

The Commerce Department has explained the bidding procedure for approximately \$3.2 billion of procurement contracts now open to U.S. firms from Japan's Nippon Telephone & Telegraph Public Corp.—part of a trade agreement signed during the Tokyo round of Multilateral Trade Negotiations.

The explanation is offered in the Aug. 20 issue of the department's international trade

magazine, *Business America*, which is available for \$2.75 from the Superintendent of Documents, U.S. Government Printing Office, Washington, DC 20402. The magazine also describes procedures for selling interconnection equipment like data terminals, telephone-answering machines, and decorator telephones to the Japanese public.

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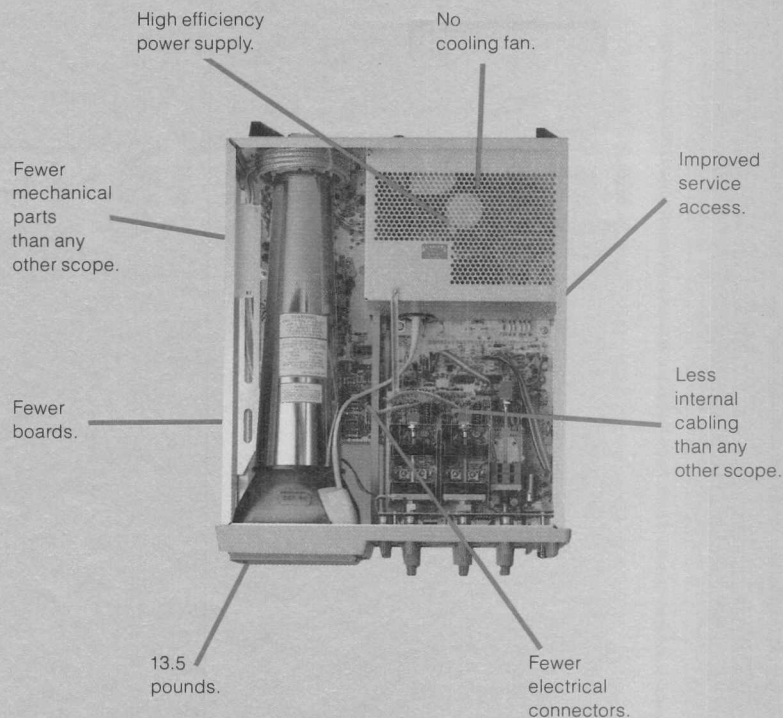
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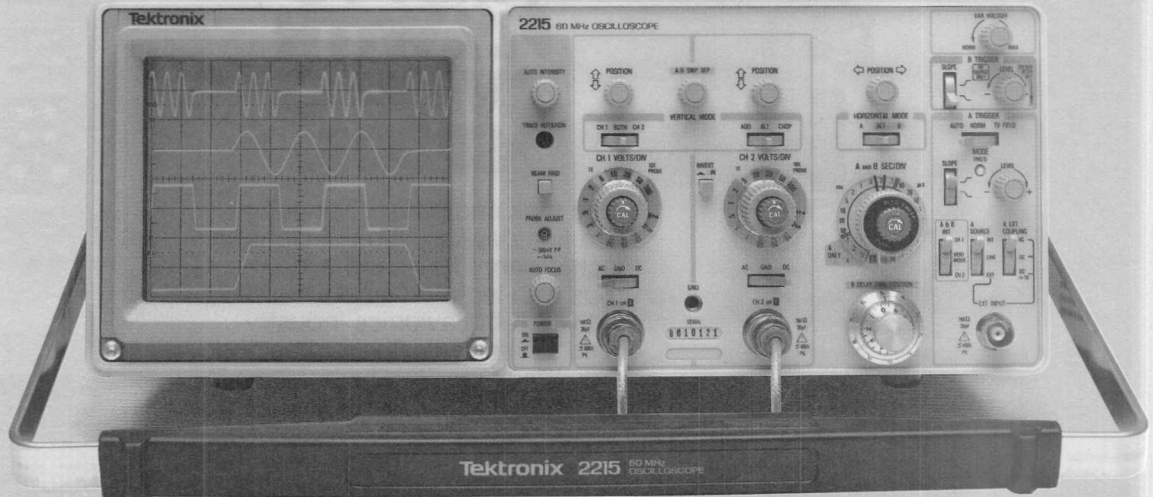
2213: standard sweep, intensified after delay, and delayed; delay times from 0.5 μ s to 4 ms. 2215: increased delayed measurement accuracy to $\pm 1.5\%$; A only, B only, or A and B alternately with A intensified by B; B sweeps run after delay or separate trigger.

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achieved with fewer boards. (The 2213 has only one). Board electrical connectors are reduced in number — virtually eliminated in the 2213 — and cabling cut an amazing 90%.

Fewer components and fewer boards mean fewer steps in assembly, less testing, less likelihood of testing errors.

These are the direct efficiencies that keep prices low and reliability high.

The 2213 and 2215 also feature a high efficiency power supply and power-saving circuitry.

These innovations eliminate the need for a cooling fan and help make the scopes smaller, lighter and cleaner.

In addition, the power supply works all over the world (90-250 Vac, 48-62 Hz) without needing a line switch or a bulky line transformer. This special power supply also regulates fluctuations in line voltage, to assure calibrated measurements.

These are just some of the innovations built into the 2213 and 2215 to

reduce costs and improve performance.

Performance that's written all over the front panels.

The bandwidth for digital and high-speed analog circuits. The sensitivity for low signal measurements. The sweep speeds for fast logic families. And delayed sweep for fast, accurate timing measurements.

The advanced trigger system features a vertical mode for true alternate triggering on both channels. It even has a convenient signal-seeking auto mode. And it also triggers on either TV lines or fields at any sweep speed for video service.

These scopes have it all. They're lightweight for field work. They've got a bright, easy to view display. Automatic CRT focus and intensity. Beam finder. And the operating simplicity to fit a wide range of operator skills.

These are the advances in performance, cost savings and convenience that break tradition. But other traditions remain. Like fast, reliable ser-

vice support. Nearly 1300 people around the world to service Tektronix products exclusively. Plus the customer documentation, training programs and applications assistance that help to make Tek service the most comprehensive in the industry. And make your 2200 scope an even greater value.

For literature on the 2213 and 2215, contact the Tek office nearest you. Or call us toll-free. 1-800-547-6711.

In Oregon, 1-800-452-6773.

For further information, contact:

U.S.A., Asia, Australia, Central & South America, Japan
Tektronix, Inc.
P.O. Box 4828
Portland, OR 97208
Phone: 800/547-6711
Oregon only 800/452-6773
Telex: 910-467-8708
Cable: TEKTRONIX

Europe, Africa, Middle East
Tektronix International, Inc.
European Marketing Centre
Postbox 827
1180 AV Amstelveen
The Netherlands
Telex: 18312

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Tektronix Canada Inc.
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Barrie, Ontario L4M 4V3
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ARINC 600. FIRST TO FLY WITH AVIONIC SPECS.

Since rack and panel connectors were first devised, the ITT Cannon Electric name has been synonymous with technological leadership. And when the avionics industry called for a new design to meet the demands of modern technology, ITT Cannon again held center stage with the ARINC 600 connector series. We were the first manufacturer qualified to commercial avionics specifications. That means we've already gone through the learning curve, and can offer you a most dependable line of Arinc connectors.

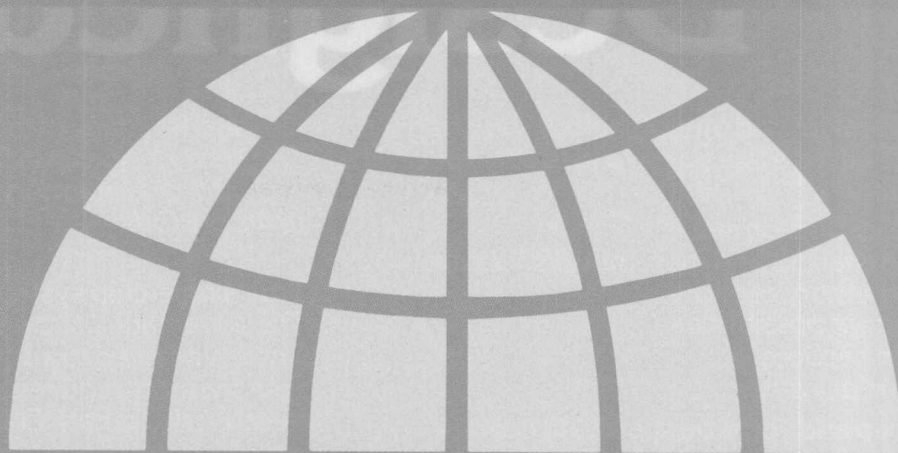
Cannon's low insertion force BKAD/E series connectors are available in environmental and non-environmental designs. Their contacts are fully interchangeable with our DPX series. And termination tooling is the same for easy retrofitting. You get greater reliability, easier maintenance and lower cost per mated line in a totally-installed system.

At ITT Cannon, we have product when you need it. And you can choose from a wide assortment of contact configurations. For immediate information, refer to our pages in EEM. For literature, the name of your local ITT Cannon distributor or other information, contact Rectangular Division Marketing Manager, ITT Cannon Electric, a division of International Telephone and Telegraph Corporation, 10550 Talbert Avenue, Fountain Valley, CA 92708. (714) 964-7400. In Europe, contact ITT Cannon Electric, Avenue Louise 250, B-1050 Brussels, Belgium. Phone: 02/640.36.00.

CANNON ITT

You can always connect with Cannon.

CIRCLE 26



ElectronicDesign

INTERNATIONAL

September 30, 1981

Benchtop tester handles variety of μ Ps, RAMs, ROMs

British step up fiber-optic efforts

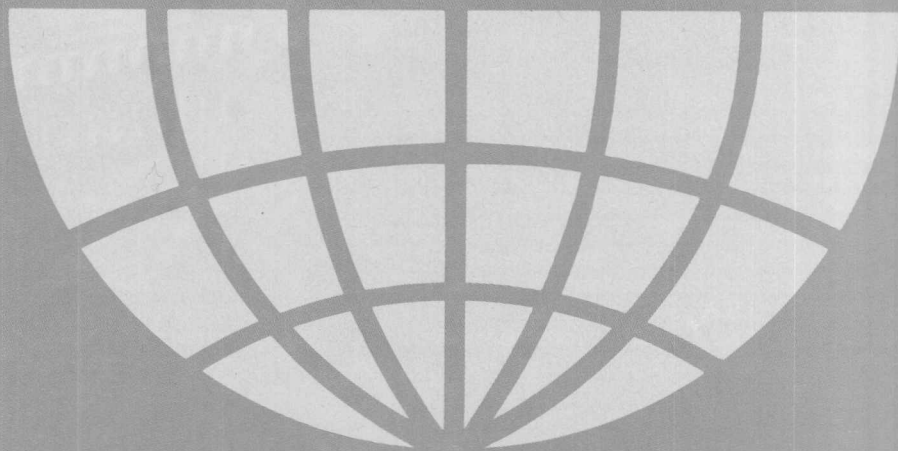
International meetings

Digital phase meter resolves 0.1°

μ C module slides into Eurocard slot

Hybrids aid 1553 bus communication

GaAs laser exhibits low aging rate



Designed with

If you could design your own μ C before you designed your next μ C-based system, you'd probably specify the following features:

- 8048 type instruction set
- hardware serial I/O and multi-transmitter capability
- choice of memory capacity
- three interrupt possibilities
- full support services
- fast, reliable delivery.

Add all that up and you'd be specifying our new 8400 μ C family, one member of which is almost certainly exactly right for you.

Europe's foremost μ C family

The 8400 family is Europe's foremost μ C family and an exciting new development. It's firmly based on the 8048, which we manufacture in both the USA and Europe. The 8400, however, has hardware serial I/O and multi-transmitter capability. Both these features

are ideal for many of the applications listed below.

Another significant feature of the 8400 family is the wide choice of memory capacity. This currently extends to 4K of ROM.

True single-chip systems

The advantages of the 8400's design are obvious. There's no need to add other chips when you add up your memory requirements. Your software gets simpler because the serial I/O and multi-transmitter facilities simplify communication between μ Cs and peripherals. And simpler software makes more effective use of available ROM capacity.

These innovative hardware features are due to the 8400's flexible architecture. This will also allow hardware customisation to be offered for large-volume applications, which could well be the competitive edge you're looking for in today's increasingly look-alike marketing world.

THE 8400 FAMILY. IDEAL FOR:

Audio

Video

Home Appliances

Telecoms

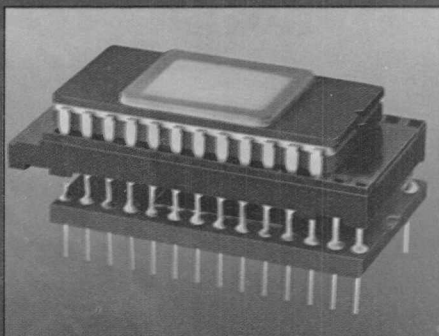
Office Equipment

Instrumentation

Process Control

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The ROMless 8400 employs a 4 or 8 K EPROM that plugs on top. Apart from program memory, it provides the same functions and has the same pin-out as the rest of the family.



Electronic
Components
and Materials

you in mind

The 8400 family is therefore a cost-effective, single-chip answer to a wide range of application requirements.

The current range

Right now the 8400 family looks like this:

Type No.	ROM K bytes	RAM bytes
8400	piggy-back	128
8405	0,5	32
8410	1	64
8420	2	64
8440	4	128

Basic spec. details are as follows: 8-bit CPU, ROM, RAM, timer/event counter and 23 I/O lines in a single 28-pin package.

Instruction set is about 90% the same as that of the 8048. Machine cycle time is 6.77 μ s at 4.43 MHz.

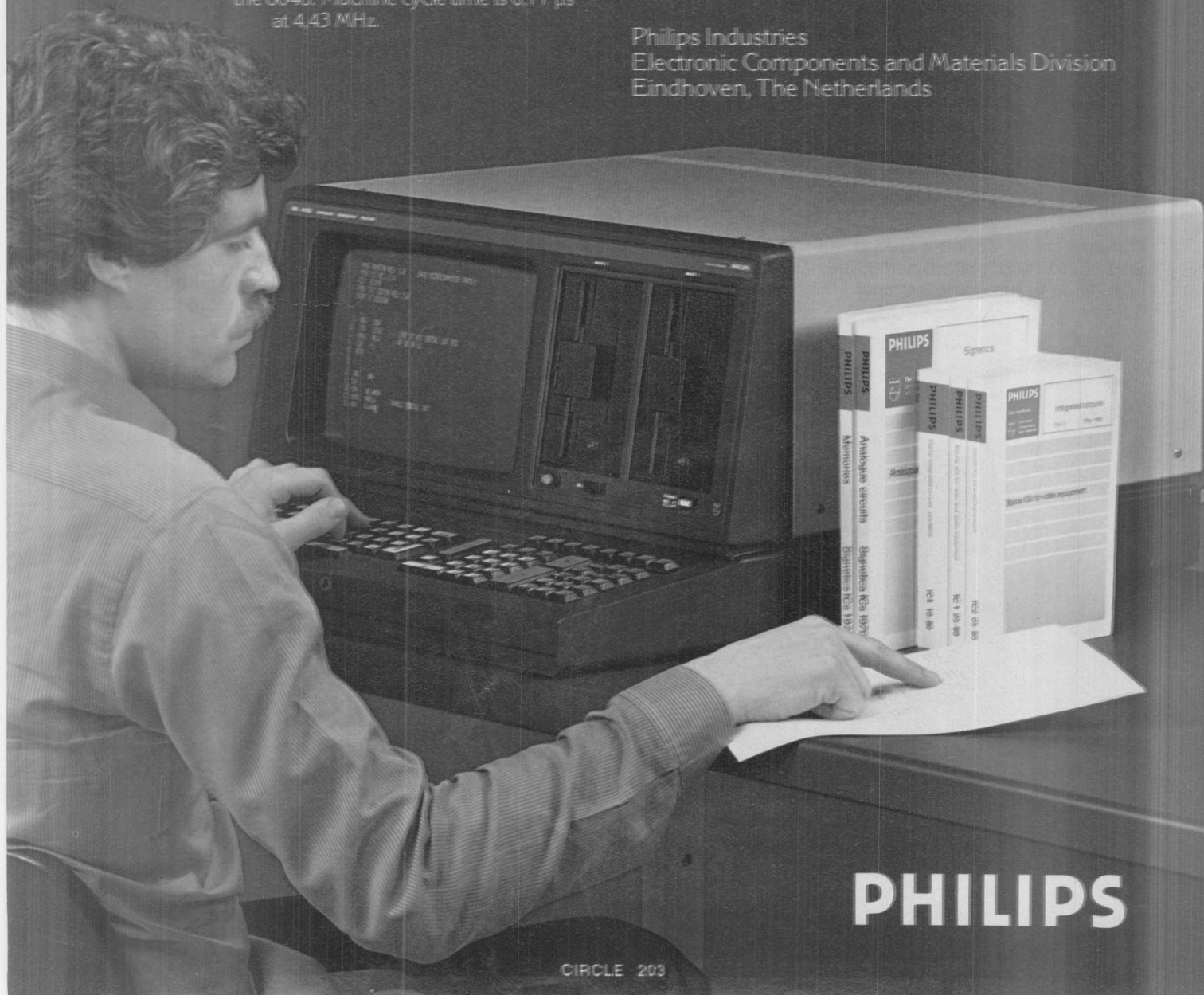
Easy development

With Philips you have three routes to easy development. One, the low-cost design aid PM 4300 for evaluation, prototyping and debugging. Two, the Philips Microcomputer Development System (PMDS), illustrated below, which is a complete development lab in itself, able to handle every 8400 family operation from preliminary design through to the final integration of hardware and software. And three, the ROMless 8400 shown below left, which employs a 4 or 8 K EPROM and is therefore ideal for prototyping, testing and low-volume production.

Nor are the PM 4300 or the PMDS limited to the 8400 family, but can handle all popular μ C and μ P types. Which is yet another feature we designed with you in mind.

Send for details today.

Philips Industries
Electronic Components and Materials Division
Eindhoven, The Netherlands



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SIEMENS

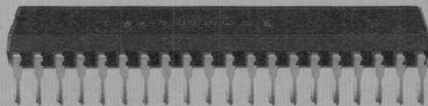
The single-chip solution saves energy, space and costs

The advantages of the single-chip solution are obvious: less expense during development and production, and less energy and space requirements.

Siemens produces a broad spectrum of powerful single-chip microcomputers with gradually increasing capabilities. This includes ROM-less versions especially well suited for small series production and for pilot runs during the development stage.

The standard devices SAB 8021/22, 8048/49 and 8051 contain all the functional elements of a digital computing system, including program memory and read/write memory – and with everything packed on one small chip.

Our application-oriented computers SAB 80210, 80212, 80215 and 80218, in addition to the computational



elements of a standard microcomputer, contain additional functions such as a/d converters, oscillators, counters/clocks, timers, LED drivers and further parallel and serial interfaces. The single-chip solution's space and cost advantages become especially apparent in the actual use of these computers – for example in entertainment, automotive, or household electronics.

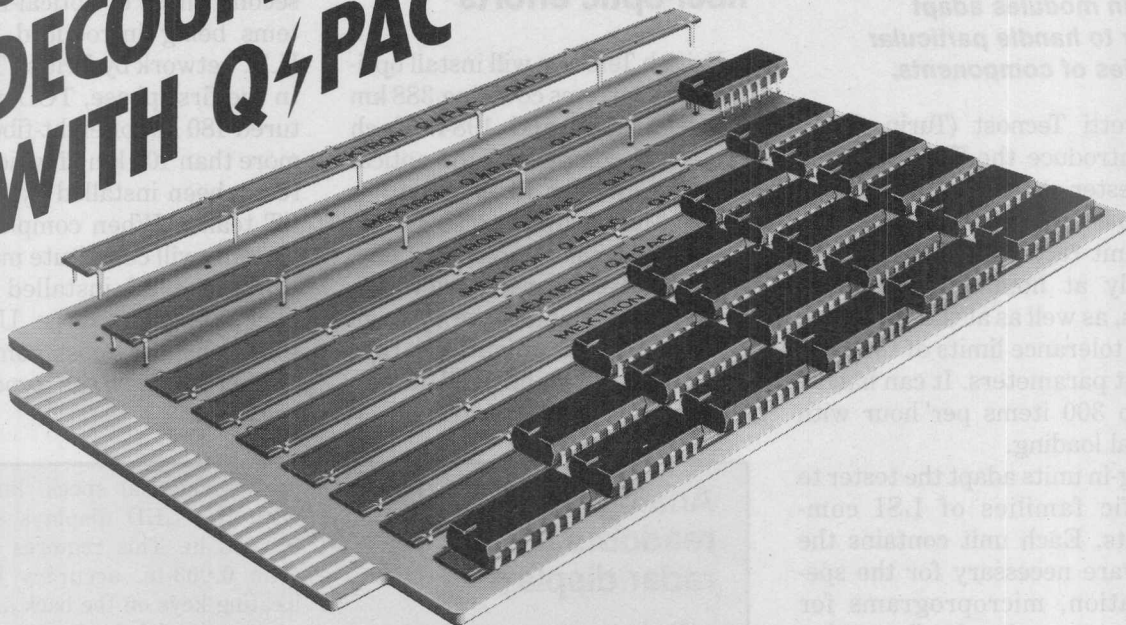
Siemens provides strong support when you're writing applications software – with system consulting, powerful development systems, an extensive program library as well as programming courses in our microcomputer colleges.

We will gladly provide further details – write to Siemens AG, Bereich Bauelemente, Infoservice, Postfach 156, D-8510 Fürth, quote "single-chip microcomputer".



Single-Chip microcomputers from Siemens

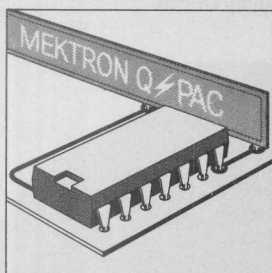
OBSOLETE DECOUPLING CAPACITORS WITH Q/PAC®



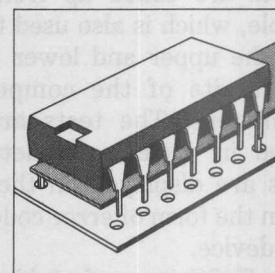
Q/Pac high capacitance power distribution components are very much a part of the story behind modern, simplified and lower cost printed circuit board design.

This was also Intel Corporation's experience when it designed its new high capacity series

90 memory system, using the Q/Pac device and two layer circuit boards. Thus the finished boards exhibited extremely low noise levels. Mektron's Q/Pac components eliminate decoupling capacitors, printed power tracks and extra board layers.



- Q/Pac components are essentially multitapped, elongated, ceramic capacitors, which also perform off the board power and ground bussing.
- Q/Pac components offer a high capacitance combined with a low inductance and hence a low impedance.
- Q/Pac components are available in capacitance values up to $0.02 \mu F$ per cm in lengths up to 400 mm.
- Q/Pac components can be obtained in two and three layer versions. Two different configurations allow mounting either vertically between the rows of IC's or horizontally under the IC packages.
- Q/Pac components simplify and speed-up board lay-out and development, and reduce cost as on-board power tracks and discrete decoupling capacitors are eliminated.
- Q/Pac components are very easy to install and increase the system reliability through reduced part count.



Mektron n.v. Afrikalaan 188 B-9000 Gent Belgium Tel.: 091/23.59.67 Twx: 11553

European subsidiary of the **ROGERS** Corp. USA.

Q/Pac: registered trade mark of the Rogers Corporation USA and Mektron.

Benchtop tester handles variety of μ Ps, RAMs, ROMs

Plug-in modules adapt tester to handle particular families of components.

Olivetti Tecnost (Turin, Italy) will introduce the T48C desktop LSI tester at the BIAS 81 exhibition to be held Oct. 6-10 in Milan. The unit tests components functionally at nominal parametric values, as well as at the upper and lower tolerance limits of the component parameters. It can handle 200 to 300 items per hour with manual loading.

Plug-in units adapt the tester to specific families of LSI components. Each unit contains the hardware necessary for the specialization, microprograms for testing an entire family, and a zero-insertion-force socket for the components to be tested. Plug-in units are available for the 8080, Z80, 8035/8048, and G800 families of microprocessors as well as for all the common RAM and ROM families.

Tests are called up from the console, which is also used to impose the upper and lower tolerance limits of the component parameters. The tests are repeated in cycles, and detected faults are displayed on the console in the form of error codes for each device.

The T48C is comfortable with acceptance testing of components quality control in extended production lines, and fault diagnosis in repair laboratories, particularly where there is already more-expensive equipment but some additional testing capacity is needed. It is also suited to situations where the production of circuit boards with LSI components

is not yet sufficient to justify a capital investment for a larger test system.

British step up fiber-optic efforts

British Telecom will install optical-fiber systems covering 388 km between 1982 and 1984. Each cable will comprise eight optical fibers, with each fiber operating at 140 Mbits/s and carrying 1920 two-way telephone conversations.

Three GEC companies will cooperate in developing the system. GEC Telecommunications Ltd. (Coventry, England) will design the overall transmission termi-

nals and repeaters. GEC Optical Fibers will manufacture the high-quality, graded-index fibers, and Telephone Cables Ltd. will make the cable.

The contracts to GEC are the second phase of optical-fiber systems being introduced into the U.K. network by British Telecom. In the first phase, TCL manufactured 180 km of eight-fiber cable, more than 100 km of which has already been installed by TCL and BT teams. When completed, the systems will constitute more than half the total installed optical-fiber capacity in the U.K. and should be the most comprehensive network of its type in the world.

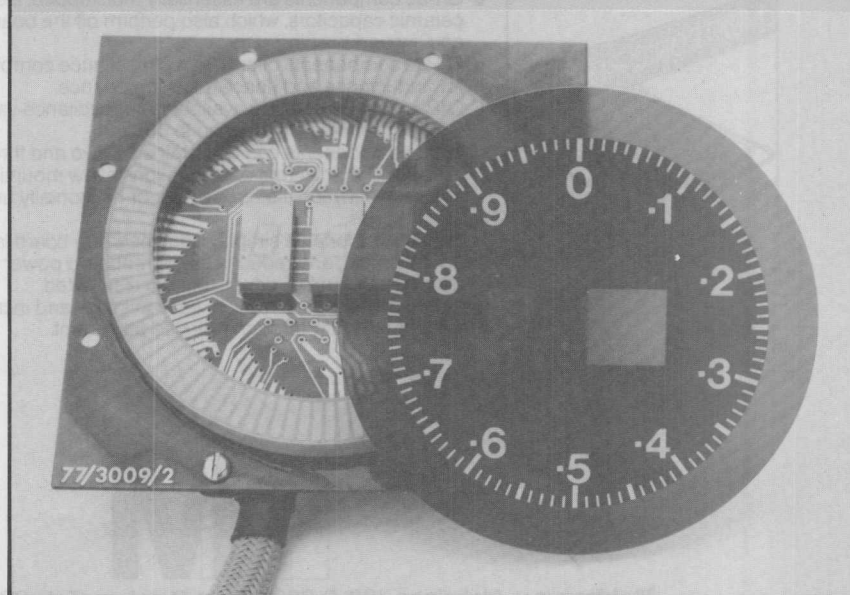
Analog-digital LED readouts aid radar displays

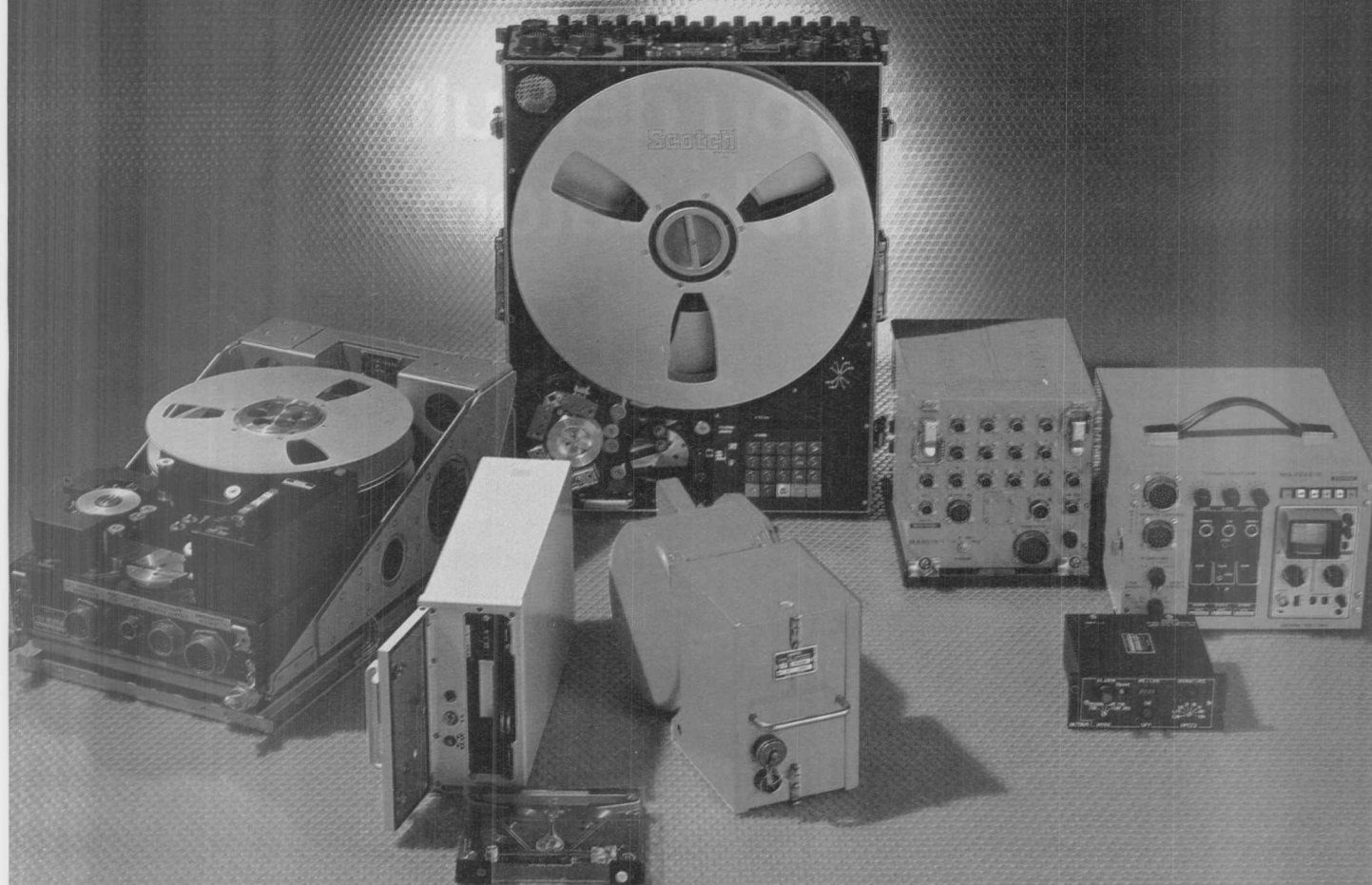
Displays with an annular ring of 100 separate LEDs combine with a three-digit readout to provide both an analog and digital data display for radar systems. They are being built by Chequers U.K. (London, England) for use in radar systems built by Racal-Decca Marine Radar (New Malden, England).

The dial, with stringent optical

and mechanical specs, lines up with the LED displays within ± 0.003 in. This requires better than 0.003-in. accuracy in the locating keys on the back and the registration of the two stages of silk-screen printing.

The dial material is a special gray filter to enhance the displays and is treated to reduce reflection and glare, thus improving legibility under all lighting conditions. Hewlett-Packard (Palo Alto, CA) is making the complete displays for Racal-Decca.





leadership in airborne magnetic recorders

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CIRCLE 206

Who lets you demultiplex and disassemble automatically?

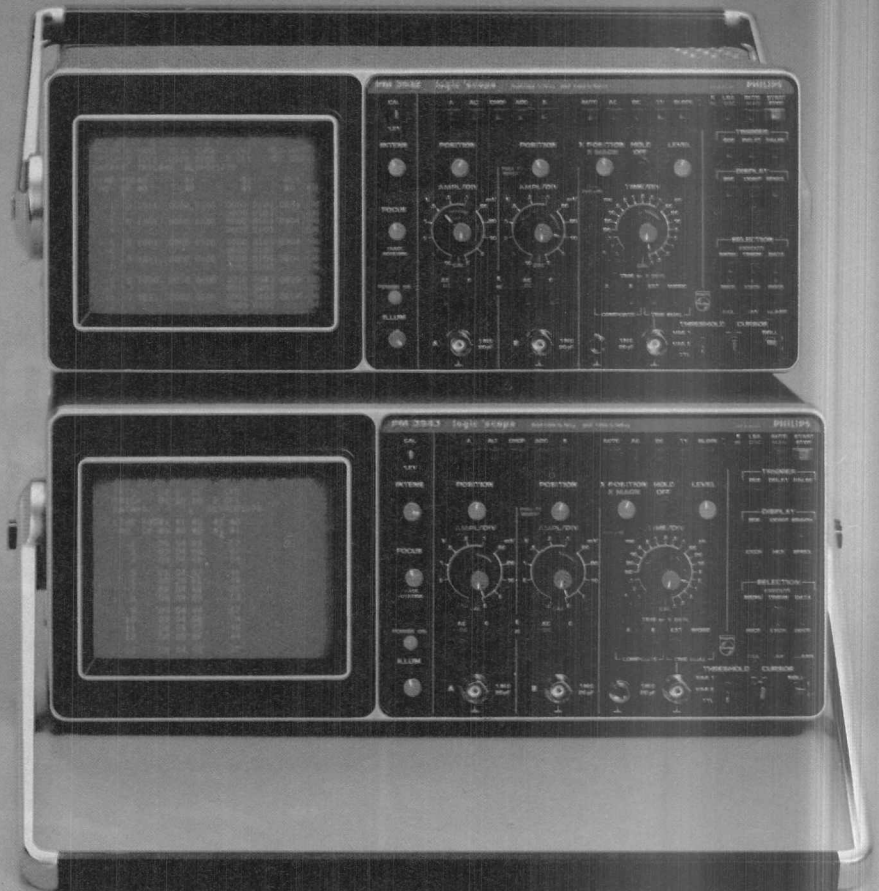
Thanks to dual clocking, both our new logic scopes separate the time-shared information found on multiplexed lines - all from the same simple connection and without need of demultiplexing latch arrangements.

Our quasiparallel triggering mode lets you trigger immediately on data sampled by each of the clocks. One clock can control address sampling and the other data sampling, so you can trigger on address and data with more bits in the word than the number of inputs to the analyser.

Add our disassembly option, and the instrument automatically sets up the sampling parameters for ease of use. With just one disassembly package, our analyzers will support the most popular 8-bit micro-processors; such as the 8048 family, 8080, 8085, Z80, 6800 family and 6500 family.

Considering this level of sophistication, you'd expect our PM 3542 and 43 to offer all the other most-wanted logic analyzer features. You'd be right.

For more information contact your local Philips office or write to:
Philips Industries, Test and Measuring Instruments Dept. Building TQ III -62,
5600 MD Eindhoven, The Netherlands.



Philips, of course



**Test & Measuring
Instruments**

PHILIPS

CIRCLE 207

International Meetings

International Electrical, Electronics Conference and Exposition, Oct. 5-7. Exhibition Place, Toronto, Ontario, Canada.

Moderne Elektronika—International Electronics Exhibition Oct. 5-9. Ljubljana, Yugoslavia.

Opto 81, Oct. 6-8. Palais des Congrès de la Porte Maillot, Paris, France.

Electrical Engineering Exhibition—ELFACK, Oct. 6-9. Gothenburg, Sweden.

International Automation Instrumentation and Microelectronics Conference and Exhibition, Oct. 6-10. Milan Trade Fair Premise, Milan, Italy.

Vidcom '81, Oct. 9-13. Palais des Festivals, Cannes, France.

Systems 81, Oct. 19-23. Munich Trade Fair Center, Munich, West Germany.

Seventh Data Communications Symposium—1981, Oct. 26-29. Mexico City, Mexico. IEEE.

International Electrical Engineering, Measurement & Control Exhibition, Oct. 27-30. Sydney, Australia.

ELKOM 81, Nov. 3-6. Helsinki Fair Centre, Helsinki, Finland.

China Comm '81, Nov. 3-13. Beijing Exhibition Center, Beijing, People's Republic of China.

Telecom '81 Germany, Nov. 4-6. Cologne, West Germany.

Isratech '81, Nov. 9-12. Binyanei Ha'ooma Convention Center, Jerusalem, Israel.

Productronica 81 International Electronic Trade Fair, Nov. 10-14. Munich Trade Fair Center, Munich, West Germany.

Automatic Testing '81, Dec. 8-10. Metropole Convention Cen-

tre, Brighton, England.

Communicasia—International Asian Electronic Communications Exhibition, Dec. 9-12. Singapore.

Data & Telecommunications/Japan, Jan. 20-23, 1982. Harumi Exposition Center, Tokyo, Japan.

Electronics OEM Assemblies Exhibition, Feb. 2-4. The Royal Horticultural Halls, London, England.

International Exhibition of Semiconductor Production Equipment, Feb. 16-18. Rein-Maine-Halle, Weisbaden, West Germany.

Seventh International Zurich Seminar on Digital Communications, Mar. 9-11. Swiss Federal Institute of Technology, Zurich, Switzerland.

International Conference on New Trends in Passive Components: Materials, Technologies, Processing, Mar. 29-31. Paris, France.

Electronic Test & Measurement Exhibition '82, Mar. 30-Apr. 1. The Forum, Manchester, England.

Sensors & Systems '82, Mar. 30-Apr. 1. The Forum, Manchester, England.

Salon International des Composants Electroniques, Apr. 1-7. Parc des Expositions, Porte de Versailles, Paris, France.

Electronics Production/Semiconductor Expo, Apr. 15-24. Beijing Exhibition Center, Beijing, People's Republic of China.

Communications 82, Apr. 20-22. The Birmingham Metropole Hotel, Birmingham, England.

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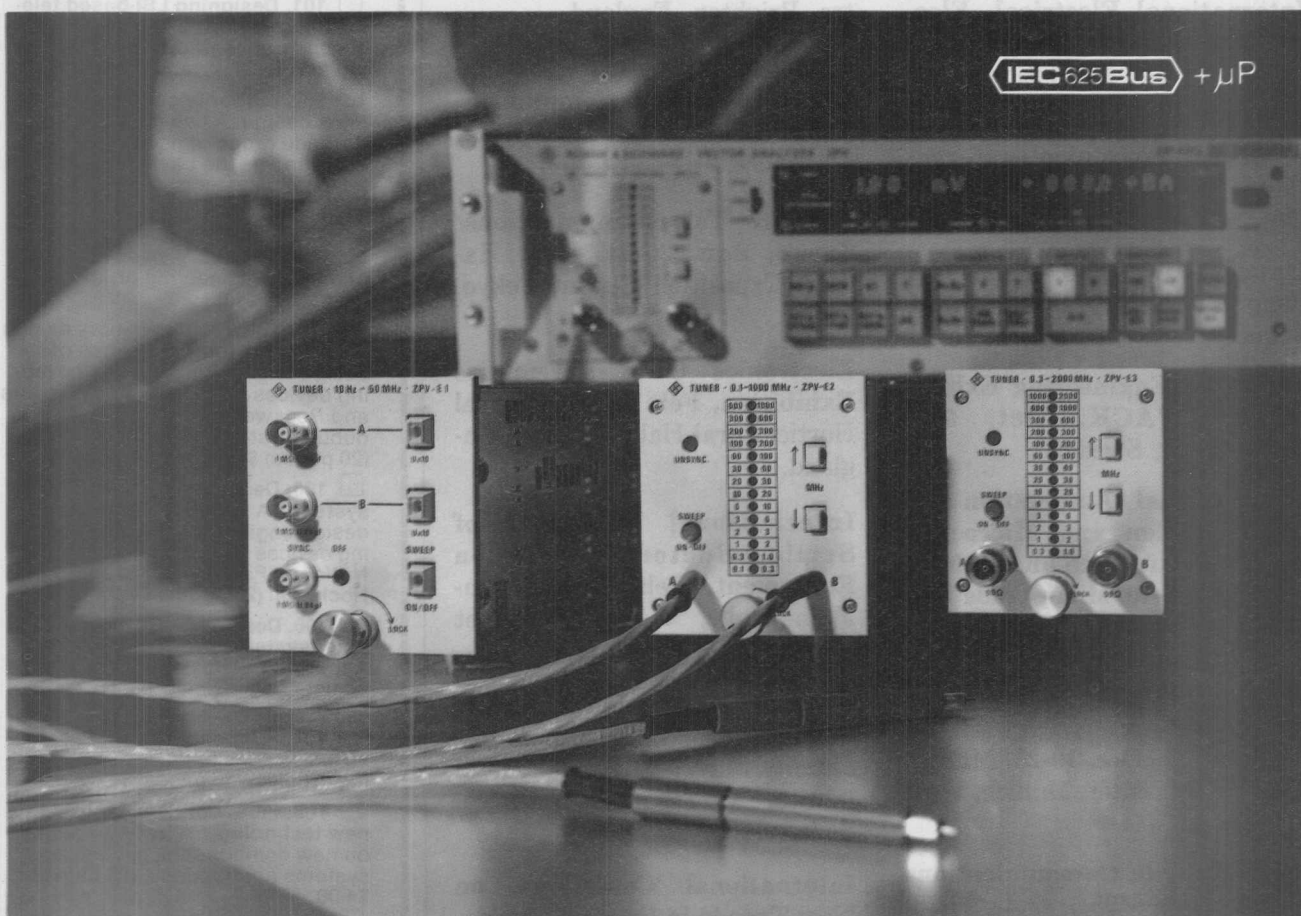
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Network analysis for AF, video and IF circuits



The new tuner plug-in ZPV-E 1 now extends the frequency range of the vector analyzer ZPV down to 10 Hz. So, together with the other tuner plug-ins, the E 2 (0.1 to 1000 MHz) and E 3 (0.3 to 2000 MHz), the ZPV now gives you an overall range of 10 Hz through 2 GHz. The ZPV-E 1 offers:

a wide choice of parameters

- voltage
- phase
- impedance
- admittance
- group delay
- reflection
- VSWR
- s-parameters

a broad range of applications

- control loops
- crystals
- crystal filters
- AF subassemblies
- video and IF subassemblies
- switching power supplies
- delay lines

and features like

- frequency range 10 Hz to 50 MHz
- dynamic range > 110 dB
- sensitivity typically 1 μ V
- listener/talker functions in line with IEC 625-1 (IEEE-488)
- high measuring rate
- switch-selected test bandwidths

One basic unit and three interchangeable plug-ins—that means the flexibility you need for uses from 10 Hz to 2 GHz, and at a price no similar unit can match. Ask for the new brochure:

Info ZPV-E 1

and if you're new to the world of the ZPV, ask for the 56-page **Info "ZPV Applications"**.

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International Products

Digital phase meter resolves 0.1°

The 3½-digit display on Feedback Instruments' DPM609 phase-angle meter displays measurements of 0° to 180° with a resolution of 0.1°. Thanks to its two front-panel mounted LEDs to indicate which of two input waveforms is leading, the meter measuring a full 360°.

The compact phase-angle meter works over the frequency range of 10 Hz to 100 kHz. For the best performance for a given input waveform, sine-wave or logic input circuitry can be chosen by means of two front-panel push-buttons. The two symmetrical input channels, each with a resistance of 1 MΩ, accept signals from 10 mV to 10 V rms for sine-wave inputs and from 1 V to 30 V peak-to-peak for logic waveforms.



For efficient screening against interference, the DPM609's ABS plastic case has an inner coating of graphite. The instrument is burned in for a minimum of 24 h before calibration. Other instruments in the 600 line of test equipment include function generators, oscillators, an electronic watt-

meter, a sweep-function generator, a variable-phase generator, a transfer function analyzer, and a digital frequency meter.

Feedback Instruments Ltd., Park Rd., Crowborough, Sussex TN6 2QR, England. (08926) 3322. Telex: 95255.

CIRCLE 500

μC module slides into Eurocard slot

All the performance and efficiency of an 8085A-based computer is available on a single Eurocard module from PEP Elektronik Systeme GmbH. The Microcomputer Module MPM 8085A is only 100 × 160 mm, yet incorporates enough computer power to function as a stand-alone single-board microcomputer in small and medium-capacity applications.

The module can mate with more than 50 memory, I/O, and control boards through its 64-way DIN 41612 style B connector. It has 46 TTL-compatible I/O lines and an optically isolated serial interface for connection with the outside world.

The module requires only a single 5-V power supply to operate. Without EPROMs, its current drain is only 700 mA. The unit can handle up to 10 kbytes

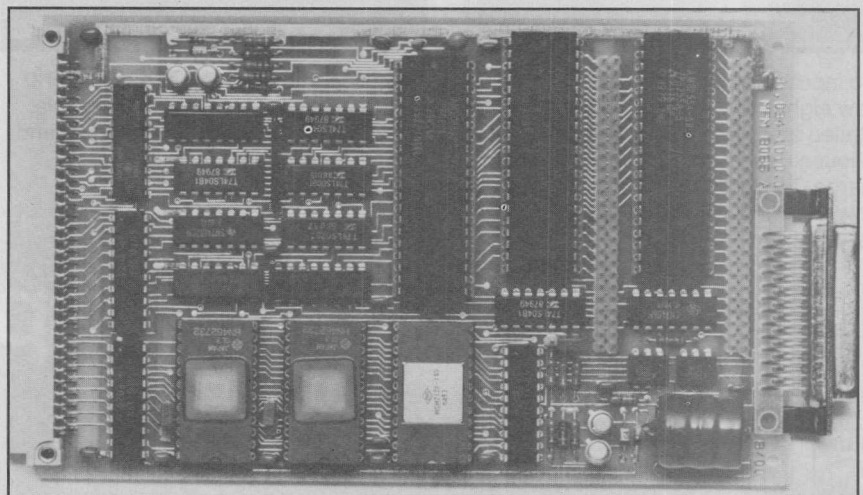
of EPROM and RAM, including 2-k × 8 bits of CMOS RAM. An on-board battery supports the RAM for 2000 hours.

Other features of the MPM 8085A include a 14-bit programmable timer, full DMA capability, five interrupt inputs, a control

input for asynchronous handshaking, and a high-performance monitor program.

PEP Elektronik Systeme GmbH, Gutenbergstrasse 9b, 8950 Kaufbeuren/Allgäu, West Germany. (08341) 5733,2429. Telex: 541233.

CIRCLE 501

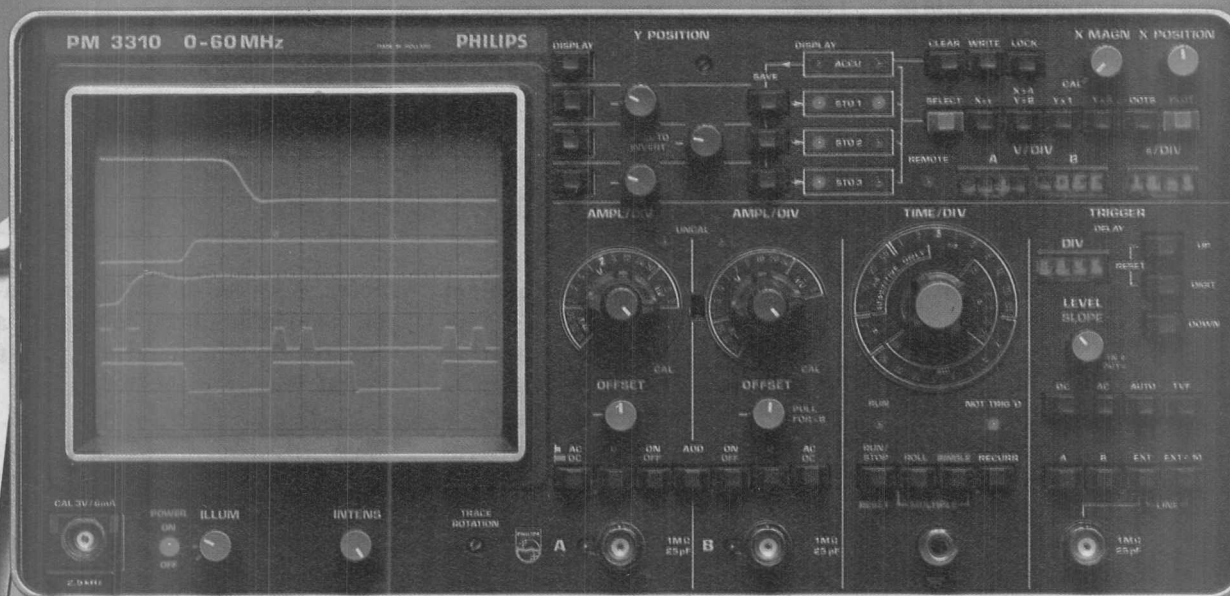


Digital storage on the PM 3310 combines easy signal capture with sophisticated signal comparison and analysis. Here's how:

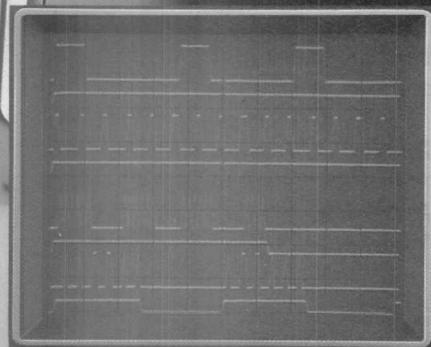
- 50 MHz clock rate (fastest yet in a portable scope) retains signal detail for fast, single-shot phenomena.
- 4 memories and 2 channels give multiple display modes over a 60 MHz bandwidth.
- A trigger delay of -9 to +9999 divisions that effectively

stretches memory capacity and provides pre-/post-triggering.

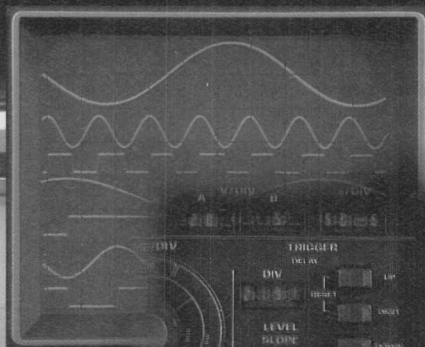
- IEEE/IEC-Bus for systems operation and further signal analysis.
- Multiple single-shot mode for capture of successive transients.
- Plus TV triggering, X-t recorder type roll mode and X-Y recorder output.



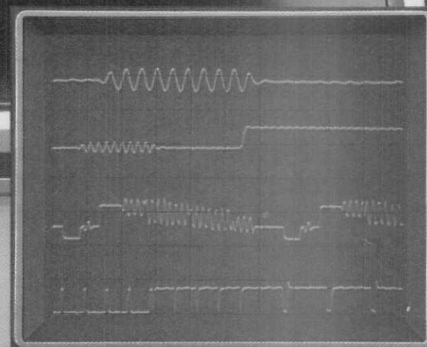
PM 3310 sets a new standard in digital storage



Two input channels and four memories allow eight traces to be displayed for detailed analysis and comparison. The in-house developed Profiled Peristaltic Charge Coupled Device (P² CCD) allows 50 MHz data to be sampled in a cost-effective manner.



Easy operation is another big PM 3310 plus. Parameter settings, for example, are stored with the relevant signals and can be recalled for display.



An accurate -9 to +9999 division trigger delay extends the basic benefits of A/D conversion. This facility is used here to pick out a particular TV colour burst.

Philips Industries, TQ III-4-62,
Eindhoven, The Netherlands.

From Philips, of course



**Test & Measuring
Instruments**

PHILIPS

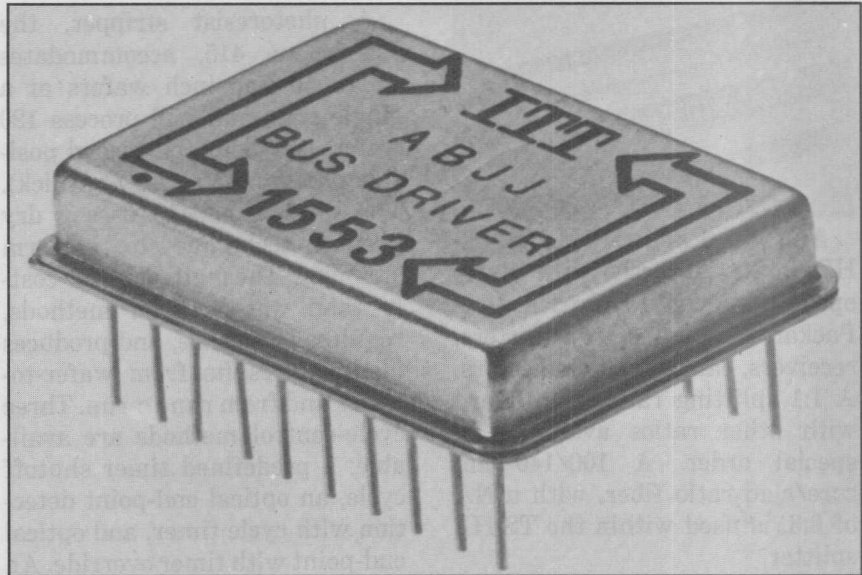
Hybrids aid 1553 bus communication

Two hybrid circuits perform all the major functions required for communications on the MIL-STD-1553 data bus. The two packages—a bus driver/receiver and an encoder/decoder—are the first in a family dedicated to the 1553, a versatile time-division-multiplexed serial data bus.

A 1553 system transfers Manchester II biphase-encoded data at 1 Mbit/s with a bit error rate of only 1 in 10^7 . It operates asynchronously in a command-response fashion, allowing up to 32 systems to communicate on the same bus using a single master controller.

To improve the signal-to-noise ratio, the FC15535 bus driver/receiver includes filtering on the receiver input. Other features are surge suppression on the bus inputs and integral bus time-out circuit. The FC15535 is fully compatible with transformer or direct-coupled connections. Power dissipation is low—only 5 W at a 100% duty cycle.

The FC15533 encoder/decoder validates data, performs Man-



chester II encoding and decoding, and provides the interface between a 16-bit parallel data bus and the 1553 multiplexed data bus. It contains a receiver, a driver, and bus time-out circuitry, a sync and parity generator/validator, and terminal address inputs.

The FC15533 can be used as an additional redundant facility in

conjunction with the FC15532 dual-redundant remote terminal. The terminal implements all 1553 protocols and contains 32 words of FIFO memory and a 16-MHz oscillator.

ITT Components Group, Film Circuit Unit, Brixham Rd., Paignton, Devon TQ4 7BE, England. (0803) 550762. Telex: 42951.

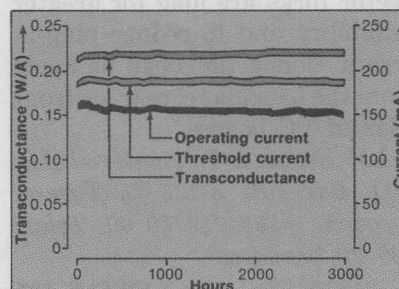
CIRCLE 502

GaAs laser exhibits low aging rate

Siemens' latest laser diodes are slow-aging devices that deliver consistent performance over their 100,000 to 1,000,000 hours of operating life. The diodes emit in the 880-nm wavelength for enhanced data-transmission rates and distances in recently designed fiber-optic cables.

Changes in operating parameters of only $10^{-3}\%$ /h have been recorded during continuous operation at a 100°C case temperature. The very slight changes were noted after an operating period of several thousand hours. The extremely low aging rate recorded at high temperatures is

expected to bring about a change in operating parameters of only $10^{-5}\%$ /h at room temperature. Real operating times of over 40,000 hours—about 5 years—have been measured at room temperature for diodes from an earlier stage of development.



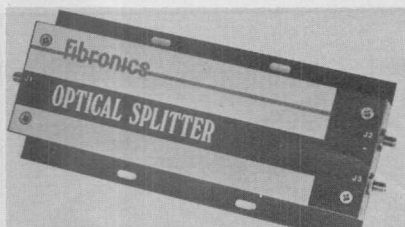
The specified output of the laser diodes is 5 mW for a strip size of $3 \times 400 \mu\text{m}$. At room temperature, the threshold current is approximately 100 mA. After continuous operation and case temperatures of up to 100°C, the threshold current only rises to 160 mA.

The increase to an 880-nm wavelength from the 820-to-850-nm range currently found in data-transmission systems will reduce the attenuation loss in fiber-optic systems.

Siemens AG, Postfach 103, D-8000 Munich 1, West Germany. (089) 2341. Telex: 52100-25.

CIRCLE 503

Optical splitter mates to HP cables/connectors



An optical splitter, Model TS-HP, mates directly with fiber-optic components from Hewlett-Packard, including transmitters, receivers, cables, and connectors. A 1:1 splitting ratio is standard with other ratios available on special order. A 100/140 μm core/clad ratio fiber, with a NA of 0.3, is used within the TS-HP splitter.

Fibronics, M.T.M. Industrial Park, Haifa 31905, Israel. (04) 536217. Telex: 46774.

CIRCLE 504

Microwave absorbers take high temperatures

Because of their high-temperature capability, Eccosorb HT microwave absorbing bricks can be used in high-power applications. The material is especially suited for lining metal housings used to cap radiating antennas. Although the exact power-handling capability of the material is dependent on the heat-transfer conditions, a typical value is from 10 to 15 W/in.². The lightweight, unicellular foamed ceramic bricks are 12 \times 18 in. and have a nominal thickness of 2 or 3 in., depending on frequency coverage. The bricks can be stacked to produce a self-supporting wall. They also can be set into a housing with mortar, masonry-style. The edges can be mitered to create cylindrical structures.

Emerson & Cuming (U.K.) Ltd., Colville Rd., Acton, London W3, England. 01-992-6692.

CIRCLE 505

Stripper processes 120 wafers per hour

A photoresist stripper, the Plasmaline 415, accommodates up to 50 four-inch wafers at a single time and will process 120 wafers per hour (patterned positive photoresist at 1.5- μm thick). The Plasmaline 415 uses a dry plasma technique to perform stripping. The method is less costly than wet-chemical methods, requires less space, and produces identical results from wafer-to-wafer and from run-to-run. Three cycle-control methods are available: a predefined timer shutoff cycle, an optical end-point detection with cycle timer, and optical end-point with timer override. An impedance matching facility automatically tunes the rf input power for maximum processing uniformity. The Plasmaline 415 measures 61 \times 61 \times 43.2 cm (24 \times 24 \times 17 in.) and weighs 396 kg (180 lb).

Microsystem Services, Duke St., High Wycombe, Bucks HP13 6EE, England. (0494) 41661. Telex: 837187.

CIRCLE 506

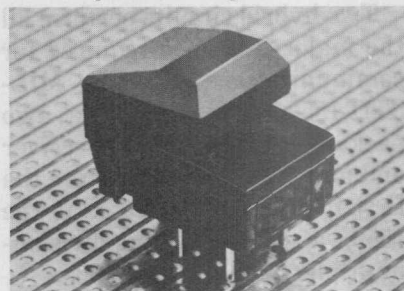
Locking spring simplifies connector installation

A locking spring on the covers, rather than on the connectors, simplifies installation of a series of inversed and standard PC-board connectors. The connectors, which range from 8 to 96 points, feature selective gold plating on the female contact surfaces. Connector forks are long for greater reliability and to reduce plug-in errors. Connections can be made from the backplane, rear, or front edge of PC boards.

LM Ericsson Telemateriel AB, P.O. Box 401, S-135 24 Tyreso, Sweden. +468 742 40 00. Telex: 109 20 lmsbo s.

CIRCLE 507

Half-key option uncovers panel legends



A "half-key" option for Keylite switches allows legends to be marked on the key or the panel only. Legends marked on a panel simplifies enclosure production. In addition, even with an operator's finger on a key, obscuring the key marking, the function legend remains visible on the panel. The half-key option does not impair the use of LEDs with the Keylite switch.

N.S.F. Ltd., Keighley, Yorkshire BD21 5EF, England. (0535) 61144. Telex: 51270.

CIRCLE 508

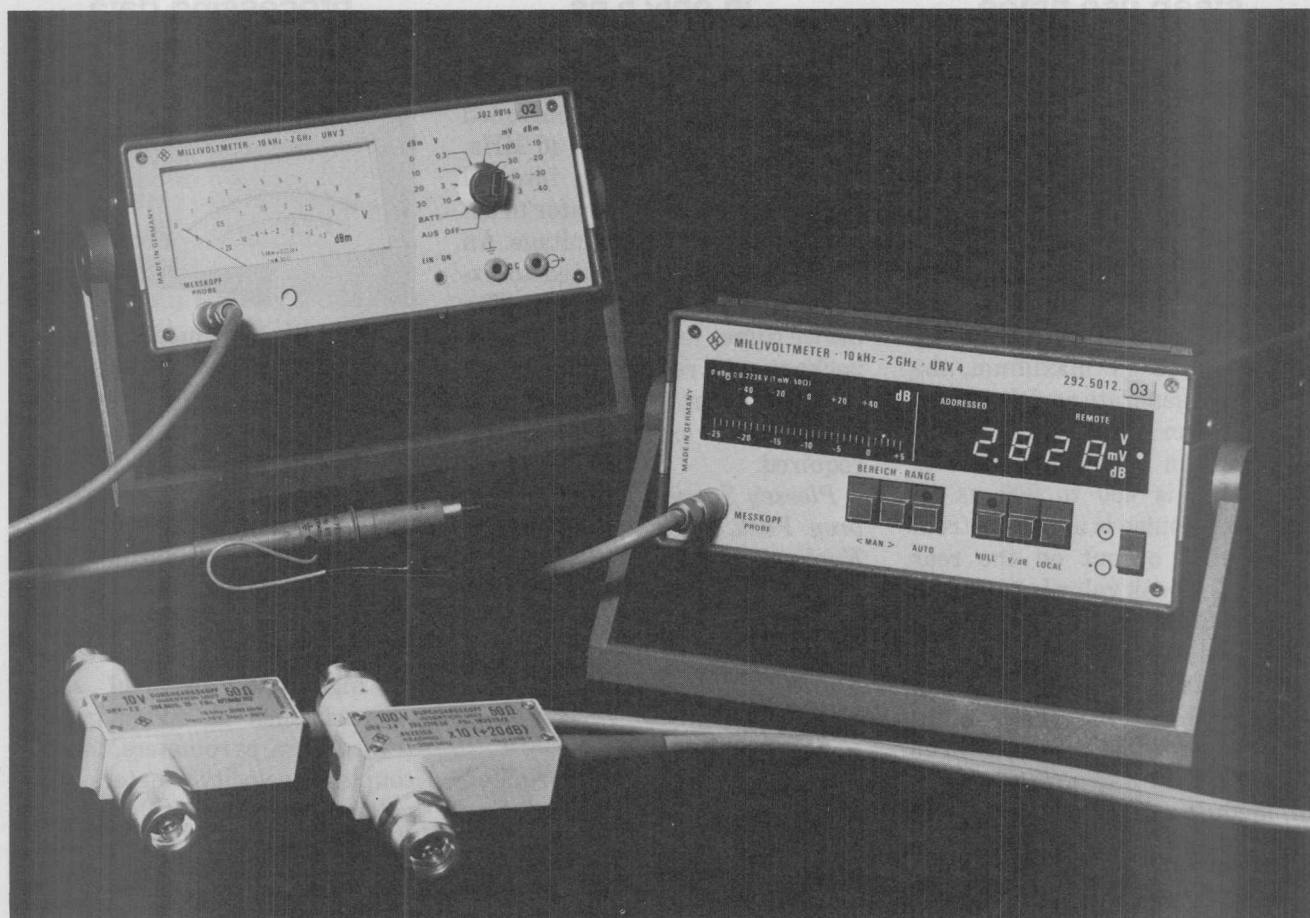
Shaft encoders count up to 20,000 pulses/rev

Resolver-to-digital shaft encoders provide counts of up to 20,000 pulses/revolution. The converters are mounted on standard Eurocards with DIN 41612 connectors. The absolute converter provides a combined accuracy (including resolver) to within ± 10 minutes of arc with a maximum slew rate of 3000 rpm. The output is 12-bit binary. TTL and control functions are provided for Busy and Inhibit. The incremental module provides 4000 counts/revolution using a two-pole resolver or 20,000 pulses/revolution using a 10-pole resolver.

Moore Reed and Co. Ltd., Walworth Industrial Estate, Andover, Hampshire, England. (0264) 4155. Telex: 47654.

CIRCLE 509

Millivoltmeters measure 2 GHz: high performance/low price



- 700 μ V to 1000 V
(-50 to +73 dBm)
- for system impedances of
50, 60 or 75 Ω
- high-impedance probe with
add-on dividers (20 and 40 dB)
- insertion units for up to 350 V
for coaxial measurements
- all measuring heads directly
interchangeable – even with
those of its predecessor,
the URV

Analog millivoltmeter URV 3

The standard voltmeter at a really low price

- rapid analog indication
 - line- or battery-powered
 - ideal for mobile use too
- Simple and easy-to-understand operation with just a single range switch. For powering it you can use a battery, accumulator or line supply (consumption only 0.2 W). There's also a battery check and a recording output. The mechanical design in a compact and rugged case ensures good screening against high electromagnetic fields.

Digital millivoltmeter URV 4

A must for systems applications

- digital and analog display
- resolution 1 μ V
- IEC-bus interface

RF voltages or levels can be displayed digitally and at the same time their tendency indicated in quasi-analog form.

The measuring range is selected automatically or manually. Zeroing is automatic and there's digital storage of the derived correction. That all means maximum operating ease: Just switch on and read off the value. What's more there's a level-proportional recording output covering 83 dB.

Over an IEC bus you get complete programming of all functions and conditioning of the measured values ready for further use.

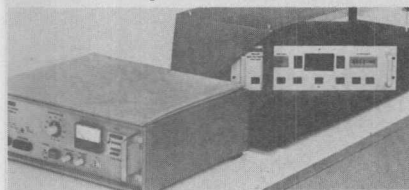
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D-8000 München 80
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Radio Communications. Development,
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Known for "electronic precision".
Independent concern (establ. 1933),
represented in 80 countries.



ROHDE & SCHWARZ

Impulse tester generates steep rise times



A high-voltage, high-current impulse tester, the PEMI-12, generates pulses with extremely steep rise times. With a charging voltage of 12 kV maximum, the tester will generate peak impulses of more than 10 kV with rise times of less than 10 ns. The time to half-value is 400 to 800 ns. A current impulse is available from a separate output on the rear panel. The peak value is 1 kA. The rise time of the first oscillation is approximately 200 ns. An antenna is available to help generate an electric field of 50 kV/m and a magnetic field of 150 A/m. The tester is built into a standard 19-in. module and operates from 115 or 230 V ac, 50 or 60 Hz.

Emile Haefely & Co., Ltd., Lehenmattstrasse 353, CH-4028 Basel, Switzerland. (061) 41 18 17.

CIRCLE 510

Spring-loaded probes make test contacts

Spring-loaded test probes make reliable contacts on PC boards or terminals. The probes have brass bodies and center pins of spring steel. The probes are finished in hard gold over copper. Part No. 455-5185-01-03-00 is pointed for making contact with PC boards. Part No. 455-5185-02-03-00 is cup shaped for making contact with a terminal or connector pin. The probe can be mounted on a 0.1-in. pitch. The recommended insertion tool is the 435-5188-01-00-00.

Cambion Electronic Products Ltd., Castleton, nr. Sheffield S30 2WR, England. (0433) 20831. Telex: 54444.

CIRCLE 511

8-bit ECL DAC settles in only 5 ns

An 8-bit ECL d-a converter, the SP9768, settles in only 5 ns. When used as a digital gain-controlled amplifier, bandwidth is 40 MHz. The device contains an internal reference voltage generator to derive the analog output voltage. An external reference is used to extend performance to 40 MHz. The device comes in an 18-pin ceramic package and requires +5 V and -5.2 V. Apart from supply decoupling, no external parts are required.

Plessey Semiconductors, Kembrey Park, Swindon SN2 6BA, England. (0793) 694994.

CIRCLE 512

CAD/CAM system meets future needs

An interactive computer-aided design and manufacturing (CAD/CAM) system, called the CAM-X, expands via additional hardware to suit the growing requirements of a design and manufacturing facility. A complete system consists of design and drafting facilities, a three-dimensional modeller, a records data base, and numerical-control production information. A basic system includes a design workstation with a graphics display unit, an alphanumeric display, a keyboard, a tablet digitizer, and a pen-like stylus. Design instructions are made to the computer, a DEC VAX, via menu commands. The modeller derives an accurate "solid" model of a part from details put in by the designer. The model can be displayed on the screen and rotated on any axis.

Ferranti Cetec Graphics Ltd., Bell Square, Brucefield, Livingston, West Lothian EH54 9BY, England. (0506) 411583. Telex: 727898.

CIRCLE 513

Scanner acquires processing data



A multipoint measuring and monitoring unit, the PM 4011 scanner extension system, automatically supervises and acquires data on a wide variety of industrial processing parameters. The unit connects to several hundred different measuring points for automatic data reduction and presentation in useful form. The PM 4011 has inputs for a variety of high and low-level signal sources, such as strain gauges, transducers, pyrometers, thermocouples, velocity meters, and voltage and current levels. The PM 4011 can be used in conjunction with the PM 4001 data logger, or the PM 4012 acquisition unit to create a complete system.

N.V. Philips' Gloeilampenfabrieken, P.O. Box 523, 5600 AM Eindhoven, The Netherlands. 040-757005. Telex: 51573.

CIRCLE 514

Compact relay offers low leakage

A compact relay, the SGR 282, offers air gaps in excess of 14 mm to assure low leakage. The unit meets the safety regulations of VDE 0631/0730 and satisfies the CENELEC standard EN 50 020. The bottom of the relay is sealed and is unaffected by flow soldering. Switching capacity is 220 V ac at 6 A.

Elesta AG Elektronik, Elestasstrasse, CH-7310 Bad Ragaz, Switzerland. 085-9-02 02. Telex: 74298.

CIRCLE 515

Interface supports 4 floppy-disk drives

A floppy-disk interface card, the PEZ8009, supports up to four 8-in. or three 5-1/4-in. drives. The card, based on a Eurocard format, interfaces the Pronto Z80 Eurocard family to single or double-density drives using single or double-sided floppy disks. The card interfaces directly to Shugart SA400, 450, 800, 850 and equivalent drives. The PEZ8009 is based on the FD1793 floppy-disk controller. A host Z80 microprocessor is synchronized to data transfer operations by the insertion of wait states. This eliminates the cost and programming overhead associated with SMA. A DIN 41612 connector is used.

Pronto Electronic Systems Ltd., 466-478 Cranbrook Rd., Gants Hill, Ilford, Essex IG2 6LE, England. 01-554-6222. Telex: 8954213.

CIRCLE 516

Darlington transistors switch fast

Two fast-switching Darlington transistors, the BU806 and BU807, operate in industrial switching circuits or function as the output transistors in TV receiver horizontal deflection circuits. Maximum power dissipation is 60 W with a dc collector current of 8 A. Both devices have integrated speed-up diodes. The BU806 has a collector-to-emitter voltage rating of 200 V and a collector-to-base voltage of 400 V. Figures for the BU807 are 150 V and 330 V respectively. Both devices have a fall-time of 0.2 μ s at a collector current of 5 A. The transistors are supplied in TO-220AB packages.

N.V. Philips' Gloeilampenfabrieken, P.O. Box 523, 5600 AM Eindhoven, The Netherlands. 040-757005. Telex: 51573.

CIRCLE 517

μ C uses CMOS for low-power operation

A single-board computer uses all CMOS parts for low-power consumption. The board, based on an NSC-800 processor, includes sockets for eight 24-pin memory ICs, two serial I/O ports, and an interruptible real-time clock. A NiCd battery provides power backup for the clock and for 2 kbits of CMOS RAM. Operating current is typically 35 mA at 5 V. An optional Akkumulator-Board permits operation, independent of power lines, for up to 48 hours. The board's processor is software compatible with the Z80 CPU. The board itself measures 100 \times 160 mm and is hardware compatible with Eurocard-sized Z80 systems.

Elsa Gesellschaft für elektronische Systeme m.b.H., Grevenberger Str. 38, 5102 Würselen, West Germany, (02405) 3737.

CIRCLE 518

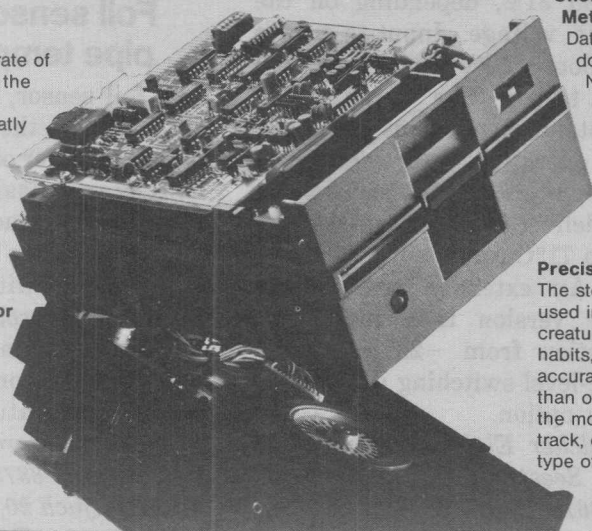
TEAC TOOK OUT BRUSHES TO BUILD IN RELIABILITY.

Controlled Frame Expansion

We matched the thermal expansion rate of the frame to that of the media. Head misalignment is greatly reduced.

Unique Long Life Brushless DC Motor

So reliable (lifetime 10,000 hours) that we let it run continuously. No motor start-up time. No electrical noise to bother CRT displays either.



Choice of 2 Recording Methods: MFM/FM

Data capacity can be doubled using MFM. No write precompensation is necessary.

Precision Head Seek

The stepping motors used in floppy disks are creatures of strange habits, stopping more accurately at some steps than others. TEAC steps the motor 4 times per track, eliminating this type of error.

The super-reliable brushless DC motor used in our FD-50 series 5 1/4 Floppy Disk Drives lasts 10,000 hours.

3 Models FD-50A/50C/50E, 3 Formats

The FD-50A is a single-density, 48 tpi, 40/35 track model. In 35-track mode it is fully compatible with the Shugart SA-400. The FD-50C is a double-track-density, 100 tpi, 77 track model, and compatible with the Micropolis 1015. The FD-50E is an industry-standard double-track-density 96 tpi, 80/70 track model.

TEAC

TEAC CORPORATION: 3-7-3 Naka-cho, Musashino, Tokyo, Japan Tel: (0422) 53-1111 Tlx: 2822451, 2822551

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• **Australia** Jacoby Mitchell Pty. Ltd., Tel: (02) 26 2675 • **South Africa** Mayfair Sales (Pty) Ltd., Tel: (011) 29-2921 • **United Kingdom** Tekdata Electronics Limited Tel: 0782 813631 • **West Germany** nbn Elektronik GmbH, Tel: 08152/390 • **Holland** Simac Electronics B.V., Tel: 40-533725 • **Belgium & Luxemburg** Simac Electronics, Tel: 02-219.24.53 • **France** Tekeltec Airtronic S.A. Tel: (1) 534-75-35 • **Italy** A.E.S.E.S.P.A., Tel: 54.64.741-2-3
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* If no distributor is listed above in your area, please contact us directly for further details about our products.

CIRCLE 211

Supply generates photomultiplier power



A high-voltage power supply, the Photon 1500, generates the power required by photomultipliers. The unit is capable of positive or negative outputs at up to 1500 V at current levels up to 3.3 mA. The output voltage is set via a built-in potentiometer, a remote potentiometer, or a remote voltage-programming signal. An output voltage monitor is provided. Ripple and noise are 2 mV pk-pk at maximum output. Load regulation is ten parts per million for a 0 to 100% load variation and a 10% line voltage variation. Stability is to within 0.005%/h. The supply requires a 22 to 30-V dc input at a maximum current of 0.5 A.

Hartley Measurements Ltd., Kenward House, Hartley Wintney, Basingstoke, Hampshire RG27 8NY, England. Hartley Wintney 3535. Telex: 858733.

CIRCLE 519

Software aids μ P data exchange

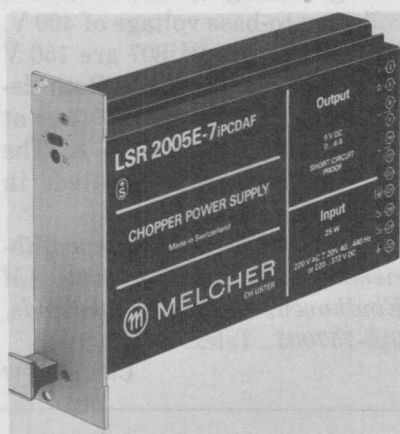
A communication software package, The RT2848, aids the exchange of data between from two to 31 microprocessors of the 8080/8085 or 8048 type. The communication protocol (similar to IBM's 2848) establishes connections, handles error control (including retransmission), and gives software warnings for debugging. Three versions of the package are available for the 8080/8085. One runs under the

Intel RMX/80 operating system, one under Siemens' RTOS, and third which requires no operating system. The 8048 version of the package is given in assembly language source code.

Elema S.p.A., Via Legnano, 26, 20121 Milan, Italy. (02) 654908 630839. Telex: 314033 elema i.

CIRCLE 520

20-W switcher offers 5, 12, 15, or 24 V dc



A range of 20-W switching power supplies, the LSR 20 E series, provides outputs at 5, 12, 15, or 24 V dc. Input voltage range is 220 to 372 V dc or 220 V ac, $\pm 20\%$. A built-in line filter attenuates noise in accordance with VDE 0875. Efficiency is between 75 and 81%, depending on the output voltage. Input-to-output isolation is 4 kV rms. The unit is SEV tested. The outputs will withstand continuous open-circuit operation and continuous short-circuit conditions. The unit will deliver its 20-W output over a 0 to 71°C range with no derating. An extended temperature range version is available for operation from -25 to +71°C. Logic-level switching is available as an option.

Melcher Elektronische Gerate AG, Seestr. 8, P.O. Box 248, CH-8610 Uster, Zurich, Switzerland. 01 9409858.

CIRCLE 521

Ceramic pots withstand high temperatures



A range of ceramic rheostats, available in 17 sizes from 4 to 500 W, withstand high temperatures. Brush contacts are solid copper graphite or silver graphite. The winding core and the base are manufactured from a ceramic with a high heat resistance. The winding, the carrier, and the base are fused with a heat-treated vitreous enamel resulting in low wire temperatures and considerable overload capability.

The Ashburton Resistance Co. Ltd., Threemilestone Industrial Estate, Truro, Cornwall TR4 9LG, England. (0872) 77431. Telex: 45453.

CIRCLE 522

Foil sensor checks pipe temperatures

A foil sensor, the Thermophil 4024, detects the temperature of pipes and other objects with large heat-transmission areas and small heat capacity. The sensor quickly acquires the temperature of the object with which it is in contact. The probe wraps around a pipe and fastens to it with a bur lock. The sensor material withstands temperatures up to 185°C.

Ultrakust-Geratebau GmbH & Co., KG, D-8375 Ruhmannsfelden, Postfach 20, West Germany. (09929) 1322. Telex: 069124.

CIRCLE 523

Let your fingers find the best deal around!

Look no further. The factory or workshop you need is ready for you now. For qualifying manufacturing industry there are full 22% Regional Development Grants and tax allowances.

For many more sound reasons for choosing Skelmersdale, telephone John Leigh today.



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Lancashire WN8 8AR.
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Telephone: Skelmersdale (0695) 32123.

A large, detailed illustration of a hand with a pointing finger directed towards a rotary telephone. The hand is rendered in a stippled, shaded style. The rotary telephone is shown from a side-on perspective, with its handset resting on the base. The entire scene is set against a light, textured background.

Skelmersdale 32123

Logic Analyzer!

Simultaneously displays the timing of 8 channels at a sampling rate of up to 100 MHz and the state of 16 channels at a sampling rate of up to 20 MHz so that it's ideal for the analysis of the time relationship between timing and state.



IWATSU SL-4601 LOGIC ANALYZER

The Iwatsu SL-4601 analyzes the mutual relationship between software and hardware in real time. Timing and state data obtained at different sampling rates can be displayed on the same frame; the timing relationship between the two can be analyzed easily. 8 channels of combination trigger and glitch trigger are provided; it also has a missing trigger function.

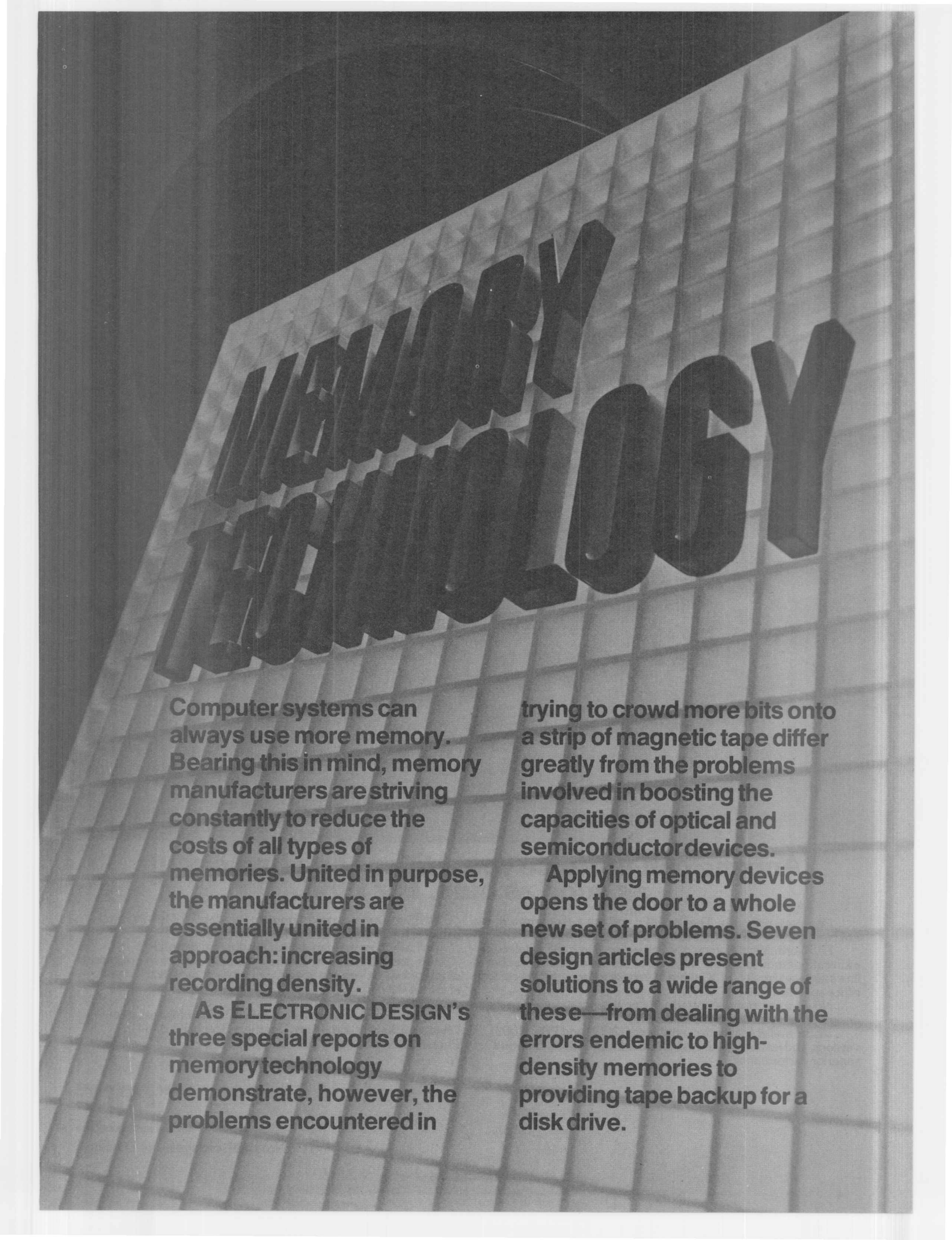
- 3 ns glitches detectable
- 1024-bit main and reference memories
- 7-inch electrostatic deflection CRT
- 2 external clock inputs for time-sharing bus signal measurement
- 4-level sequential trigger
- Easy time delay setting
- Set parameters protected by back-up battery



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MEMORY TECHNOLOGY

Computer systems can always use more memory. Bearing this in mind, memory manufacturers are striving constantly to reduce the costs of all types of memories. United in purpose, the manufacturers are essentially united in approach: increasing recording density.

As **ELECTRONIC DESIGN**'s three special reports on memory technology demonstrate, however, the problems encountered in

trying to crowd more bits onto a strip of magnetic tape differ greatly from the problems involved in boosting the capacities of optical and semiconductor devices.

Applying memory devices opens the door to a whole new set of problems. Seven design articles present solutions to a wide range of these—from dealing with the errors endemic to high-density memories to providing tape backup for a disk drive.



Anyone can promise you a telephone line circuit as good as ours. For 1983.

Promises, promises. They're OK if you can put everything on hold and gamble on the outcome. But you don't have to.

ITT North Microsystems specializes in service to the telecommunications industry. Over 500,000 of our solid state subscriber line interface circuits (SLICs) are in service today, meeting central office specifications.

Now we are proud to introduce a new generation of a proven design. VES™, Value Engineered SLIC.

VES is available in both central office (2001) and PBX (2002) versions, and features lower cost, improved power dissipation and superior performance.

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For more information, contact ITT North Microsystems Division, 700 Hillsboro Plaza, Deerfield Beach, FL 33441. Phone: 305/421-8450; TLX: 51-2329; TWX: 510-953-7523.

ITT

ITT North Microsystems Division

Technology

Advances in read/write heads, magnetic materials, and protective coatings will expand capacity and reduce costs while maintaining magnetics' supremacy in nonvolatile storage.

R&D benefit all aspects of magnetic recording

Research into virtually every aspect of magnetic recording technology promises the benefits usually associated with solid-state advances: greater density and lower cost. As a result, higher-capacity storage devices for computer peripherals are in the offing, and at prices that will maintain magnetics' cost/performance advantage over semiconductors for nonvolatile storage. Besides, although semiconductors win hands down for main memory, because of their speed, even if their price was competitive, they cannot compete with the nonvolatility, removability, and portability of disks and tape in loading programs, storing operating systems, and backing up the storage of critical data.

The major push by industry is to increase bit density, and to that end, most magnetic research is focused on the interface of the recording head with the recording material (Fig. 1). Although the physics of writing and reading 1s and 0s is straightforward, the interactions between the magnetic coating of the medium, the head, and the electronic circuitry is complex. Furthermore, a complicated interaction among flux density, coercivity, the physical properties of the material, ambient conditions, and even the size of the magnetic particle must be taken into account. Only by understanding these interactions will magnetic recording approach its limits.

Fundamental limit

According to Geoff Bate of Verbatim (Sunnyvale, CA), an estimate of the fundamental limit to bit and

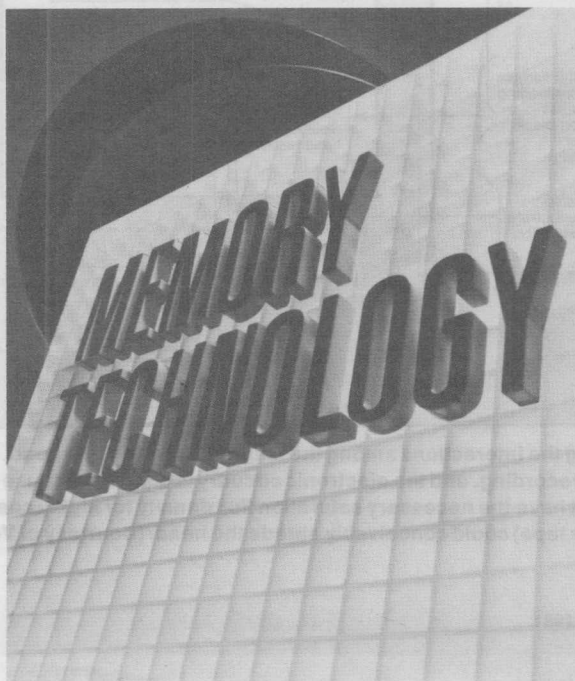
track density on flexible disks may be derived in the following way. Since the signal obtained from the recording medium depends on the number of magnetic particles per unit volume, n , and the particle noise depends on \sqrt{n} , the signal-to-noise ratio can be maximized by maximizing that parameter. Of course, the goal is to have the largest possible number of particles in each unit of volume.

To achieve that, the manufacturer can use smaller and smaller particles, but the size of the particles at which stable ferromagnetism ceases to exist sets a limit to this process. The time for which a given magnetic state is stable is an extremely sharp function of the ratio of the volume of the particle to the absolute temperature.

Bate cautions that the stability time is such a steep function of this ratio—decreasing by ten orders of magnitude for every doubling of the latter—that particles of almost all shapes and compositions become unstable at room temperature when the size drops below 200 Å. Choosing 500 Å as an average particle size at which the state is stable for archival

times of 30 years, Bate estimates that the ultimate bit density is 2×10^4 bits/mm, or 5×10^5 bits/in.

Magnetic media for high bit densities will usually have to be highly coercive to resist the increased effects of demagnetization that follow a reduction in bit length. The remanent magnetization, which is the product of the magnetic particle's remanence and the loading factor, or external mechanical force on the head (Fig. 2), will have to be optimized carefully, since



Len Yencharis, Computers
& Peripherals Editor

whereas too high a remanence yields self-demagnetization, leading to low amplitude, overlapping pulses, and peak shifts. The oxide coating must be thick to reduce both recording demagnetization and self-demagnetization, which ensures that old data is erased by the writing of new data (Fig. 3).

In the case of a flexible-disk drive, striction effects may occur between the smooth diskette and the head and cause speed variations or, in extreme cases, prevent the disk from rotating. The ability to achieve high track densities inexpensively—that is, with simple track-following servos or, better still, with no servos at all—depends on how accurately the track location can be controlled or predicted.

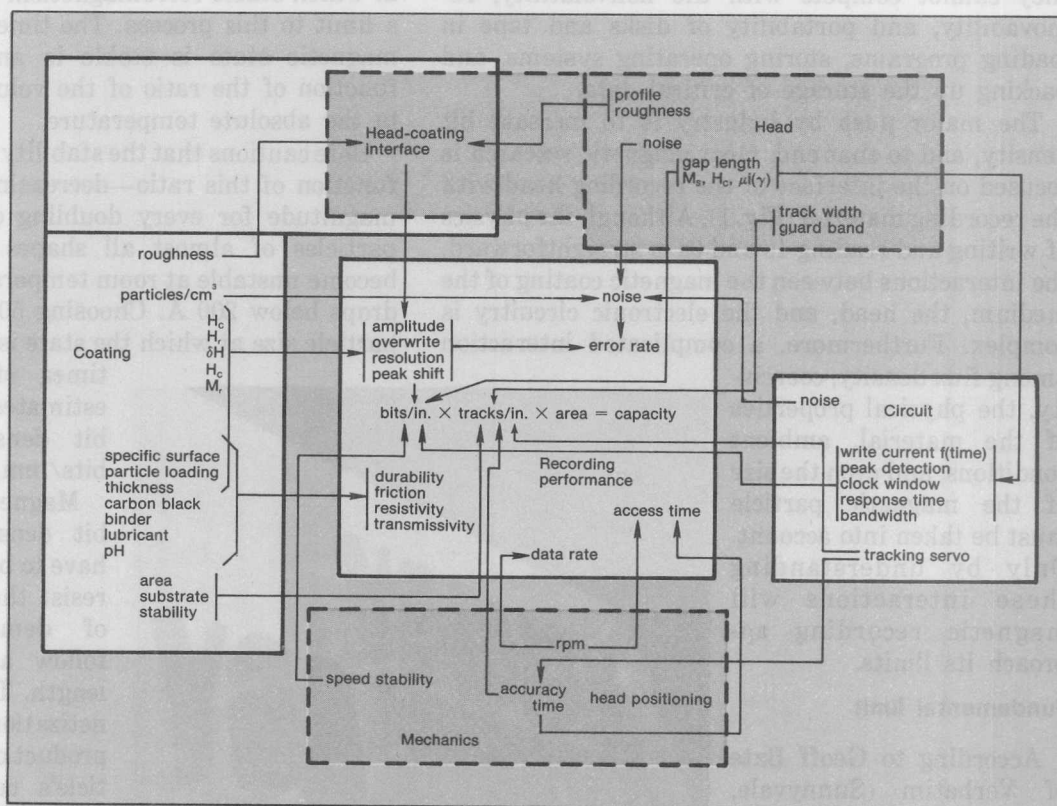
At present, all flexible disks use films of polyethylene terephthalate (PET) 3 mils thick as substrates. Keep in mind that PET has a thermal coefficient of expansion of between 15 and 21 ppm/°C and a hygroscopic expansion coefficient in the range of 9 to 15 ppm/% RH. Furthermore, these properties are anisotropic, so that a circular track can become an irregular oval. This instability limits the achievable track density to slightly more than 100 tracks/in. on drives that do not have a track-following servo.

To achieve a 150-track/in. floppy disk, the

for by measuring the positions of the inner and outer-diameter servo tracks and then using a linear interpolation to predict the position of the data tracks. The process can be repeated frequently when a disk is first inserted and less frequently as the disk stabilizes.

The choice of magnetic particles for a flexible disk goes beyond the selection of a highly coercive material (see Table 1). The particles must be uniform in shape and size and as free as possible of dendrites and pores. They must also have a narrow switching field distribution. What's more, the particles have to be nonabrasive to minimize head wear. Finally, they must be chemically compatible with the binding polymers and easily dispersible.

In contrast to rigid disks, where the particles are oriented circumferentially and each disk is coated individually, flexible disks are coated in web form (that is, as a continuous piece of material, before the disks are cut out). Since circumferential orientation cannot be achieved with flexible disks, a random distribution of particles is needed to reduce the modulation of the signal envelope as the disk rotates. To minimize the amount of mechanical orientation that takes place during coating, particles have to be

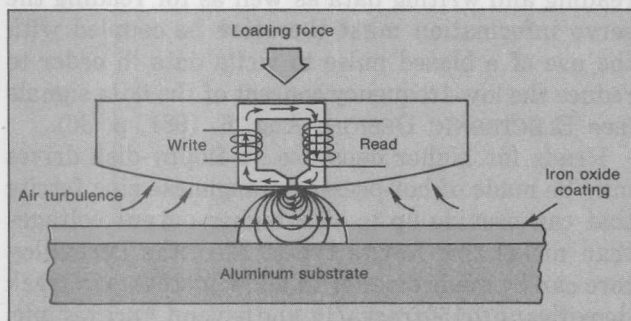


1. Optimizing the interactions among the magnetic coating, the head, the mechanical properties of flexible disk recording, and the electronic circuitry is difficult because of their complexity. A recording head may not have the necessary saturation flux density for highly coercive materials, while the coating of the disk (or tape) could conceivably abrade the head. (Courtesy of Verbatim Corp., Sunnyvale, CA.)

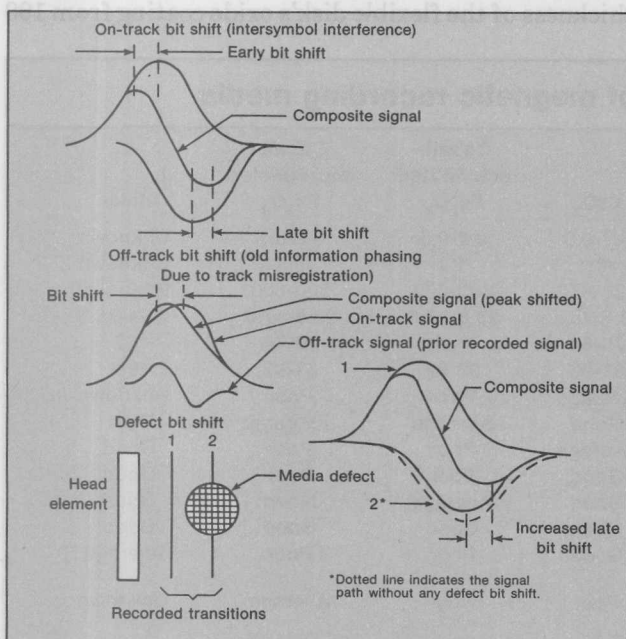
of low acicularity (crystallike).

Conductive carbon blacks are commonly added to tape and flexible-disk formulations to decrease their resistance to the point where static charge cannot build up. Accumulation of charge is undesirable because, in extreme cases, the force of attraction between a charge and its image induced in a conductor can be strong enough to affect the motion of the disk. More commonly, the discharge of accumulated charges creates noise spikes in the head.

The most severe problems with recording media are related to physical, chemical, and mechanical interactions which take place at several interfaces:



2. The loading force on the read/write head in disk recording technology determines the flying height of the head above the disk. The decrease in loading force from 350 to 10 grams with Winchester technology makes it easier to achieve higher recording densities.



3. Read/write errors in magnetic recording for disks are the result of time-domain failures, designated as bit shifts. The major contributors to bit shifting are pulse crowding, where adjacent bits can cause interference with shifts in timing pulses of the read-back signal, and the phasing in of old information with the read signal, which is produced by track misregistration and disk defects.

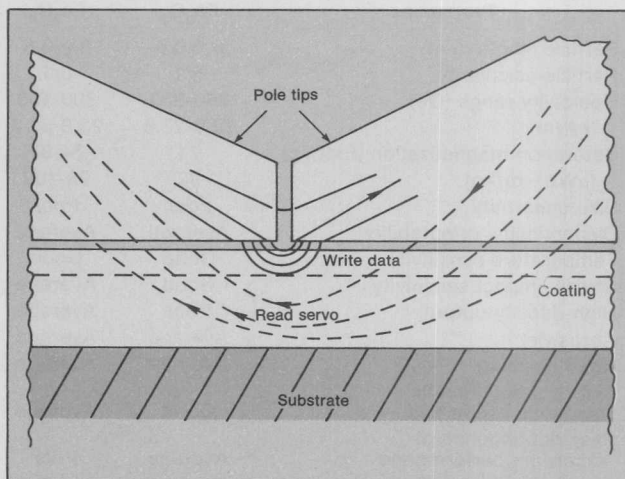
between the substrate and the coating, between the binder polymer and the particles, and between the coating and the head.

The coercivity of iron oxide particles can be increased by adding a small amount of cobalt. If the cobalt is first adsorbed on the surface of the acicular particles of iron oxide and the particles are then heated, a surface layer having a structure approximating that of cobalt ferrite is created. In this way, it is possible to make particles of cobalt-impregnated iron oxide whose coercivity reaches 800 oersteds. Chromium dioxide's coercivity, in contrast, is 470 Oe. Recently, CrO_2 particles have been made with coercivities in the range of 560 to 680 Oe, but print-through becomes a problem as the coercivity reaches 700 Oe. Print-through is the transfer of a magnetization pattern from one layer of the recording medium to adjacent layers; it is caused by the instability of the magnetic properties of the particles with respect to temperature and size. In this case, the thermal instability of CrO_2 is incompatible with the high curing temperatures of the epoxy binders used in, for example, Winchester disk coatings.

Even optical properties are important

For many applications, the electrical and optical properties of the coating are important. The timing signal of flexible disks comes from a light beam passing through holes in the disk and its jacket. The correct operation depends on the opacity of the coating at a wavelength of 900 nm, which in turn is determined by the combination of binder, lubricant, and dispersant.

Coercivities can be increased to levels of 500 Oe for iron oxide, 700 Oe for CrO_2 , 800 Oe cobalt-



4 When used as a bidirectional transducer, an inductive head can read servo information and write data simultaneously. This capability, which can be applied to the buried servo scheme, depends on the widths of the magnetic wavelengths entering into the pole tip region. (Courtesy of IBM, Tucson, AZ.)

Memory Technology: Magnetics

modified iron oxide, and 1100 Oe for metal particles.

Of all the particles developed for tape and rigid-disk coatings, no one is best in all respects. Iron oxide particles have the highest coercivity and saturation magnetism, but such particles made from lepidocrocite, the most commonly used magnetic material, have the narrowest switching field distribution in tapes and the highest magnetic orientation ratios. Chromium dioxide particles, on the other hand, have more particles per unit volume and larger specific surface area by virtue of their small size, lower density, and higher packing factor.

Positioning the head

Current head-positioning servo methods require a spatial separation between the servo information and the data. This separation limits the accuracy with which a head-positioning system can follow a data track. A possible way around this drawback is the buried servo track. This technique allows information to be recorded in the same area of the disk as is used for data. In fact, a single head can be used for both servo information and data (Fig. 4).

Compared with dedicated head-positioning and sectorized servo tracks, the buried servo concept clearly has the potential for higher track densities, since the servo information takes up space that could otherwise be used for data. What's more, a dedicated servo track requires a separate read head that must be fixed positionally with respect to the read head,

and that is difficult and costly to accomplish. In sectorized servo tracks, with interleaving sectors of servo information and data on the same track, a common head reads both the data and the servo signal, but at different times, which, like the physical separation of a dedicated servo track, limits the positioning accuracy. In addition, a compromise must be made between the amount of the track used for the servo information and the performance of the head-positioning system.

To "bury" the servo information, data must be written over the servo signals without altering them. The simultaneous use of a single head for both reading and writing data as well as for reading the servo information must therefore be coupled with the use of a biased pulse to write data in order to reduce the low-frequency content of the data signals (see ELECTRONIC DESIGN, Aug. 6, 1981, p. 36).

Heads for higher densities on floppy-disk drives may be made of hot-pressed manganese zinc ferrite that can provide up to 40% higher output voltages than nickel zinc ferrite types. Also, the Permalloy core can be made smaller to allow increases in track densities up to 150 tracks/in. and beyond. For example, Burroughs (Westlake Village, CA) reduced the core structure up to its MD122 floppy-disk drive to a third its former size. It is now made up of 4-mil read/write and 2-mil erase geometries.

Perhaps even more significant is the reduction in thickness of the flexible disk's oxide coating from 100

Table 1. Comparing properties of magnetic recording media

Properties	Standard Fe ₂ O ₃	Fe ₂ O ₃ / Fe ₃ O ₄	CrO ₂	Cobalt- substituted Fe ₂ O ₃	Cobalt- impregnated Fe ₂ O ₃	Metal
Particle length (μm)	0.2-0.5	0.2-0.5	0.2-0.5	0.2-0.5	0.2-0.5	Unknown
Particle acicularity	5:1	5:1	10:1	1:1	5:1	Unknown
Coercivity range (Oe)	250-350	300-400	450-575	300-600	300-600	1000-1150
(kA/m)	19.9-27.8	23.8-37.3	35.7-45.7	23.8-47.6	23.8-47.6	7.94-91.3
Saturation magnetization (EMU/g)	74	74-82	70-80	70-74	70-74	160
(μWb = m/kg)	92	92-102	87-99	87-92	87-92	198
Size uniformity	Poor	Poor	Average	Poor	Poor	Unknown
Dispersibility, orientability	Average	Average	Good	Average	Average	Poor
Temperature sensitivity	Good	Good	Average	Poor	Poor	Good
Stress, impact sensitivity	Good	Average	Good	Poor	Poor	Good
High-density output	Poor	Average	Good	Average	Good	Good
Abrasivity	Average	Average	Poor	Good	Good	Good
Head cleaning	Average	Average	Good	Poor	Poor	Average
Time dependence of magnetic properties	Good	Average	Poor	Poor	Average	Unknown
Pass dependence of recording performance	Average	Poor	Good	Poor	Average	Unknown
Approximate cost (\$/lb)	0.50	1.0	5.00	1.50	2.00	9.00 (estimated — not yet available as particles)

Source: Verbatim Corp.



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to 40 μm . This thinner coating allows an increased density of 7000 bits/in. and 150 tracks/in.

Another noteworthy reduction is the size of the disk that Sony decided to use in its recently announced floppy-disk drive (ELECTRONIC DESIGN, June 11, 1981, p. 46). The 3½-in. disk features a coercivity of 500 Oe and is coated with cobalt-modified ferric oxide. In addition to having an impressive recording density of twice that of conventional minifloppies, the drive incorporates a tunnel erase head with a narrow track width. The head's core is manganese-zinc crystal ferrite, and the read/write gap is 2 μm .

Magnetic recording has evolved from an entertainment medium into a highly sophisticated method of information storage that extends into virtually every sphere of data communications and processing. Rigorous applications, such as those of large, modern tape drives used with computer systems, subject the write/read magnetic head to nearly continuous operation at high tape speeds—frequently on the order of 100 to 200 in./s. Eventually, the head wears out because of the abrading action of the magnetic tape's oxide coating against the head's face (the pole

tip). Obviously, the faster the tape moves and the more frequently, the faster the head is abraded.

Magnetic heads used in data processing are multichannel types that form the vital transducing links between the magnetic tape and the sensitive electronic read/write drive circuits. These circuits are readily affected by changes in the head performance due to wear, requiring continual adjustments to prevent loss of data as wear progresses. These adjustments are inevitable when recording heads are constructed from conventional materials, like Mu-metal, aluminum, or brass. Even chrome-plated heads ordinarily must be replaced during the lifetime of most tape drives.

Ceramic-coated materials have shown better wear-resistant properties. The hard coating protects the soft magnetic core from the harsh abrading action of the tapes. One restraint is that the ceramic coating must not cover the gap area in the magnetic core, as that is the sensing portion of the magnetic head.

Normally, the spacing between the recording medium and the gap should not exceed 20 $\mu\text{in.}$, and in some cases must not exceed 10 $\mu\text{in.}$ However, such a thin wear-resistant coating would not extend

How a thin-film head is made

Recording heads are now being fabricated with thin-film semiconductor processes as part of the drive for higher recording densities in magnetic storage. Such heads made with the same processing steps as for ICs—photolithography, electroplating, vacuum deposition, and plasma etching—are already in a few disk and tape drives, and many more are in the works that will eventually find their way into, for example, gigabyte disk drives.

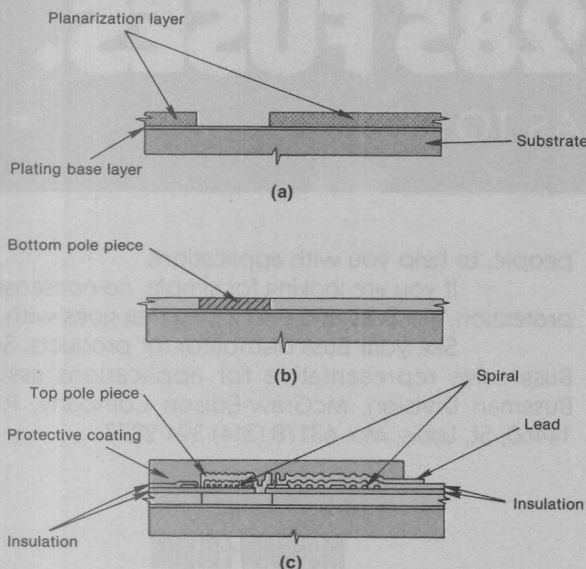
As an example, consider the 18-channel thin-film head from Nortronics (Minneapolis, MN) used in ½-

in. tape drives. Instead of being a coil of wire, the head's inductive circuit is a thin-film conductor deposited as a spiral on the substrate. The core is Permalloy, a mixture of nickel and iron. As major steps in fabrication, the company employs plasma etching, electroplating, and sputtering.

A planarization layer of polyimide is employed around the bottom pole for good step coverage of subsequent thin-film layers. The polyimide is plasma-etched in electrically excited oxygen gas to form the pole region (a). A high-frequency electric discharge at low pressure breaks down the oxygen molecules into a variety of ions and free radicals. The free radicals attack the polyimide but do not react with the aluminum mask.

Next, the pole region is back-filled with Permalloy by electroplating (b) in order to achieve the necessary thickness in an adhering stress-free form. The process is set up with an acid sulphate bath whose pH is carefully controlled. The solution is then electrolyzed, using a galvanostat to control the current density to ensure that the film is void of magnetostrictive elements. A magnetic field is applied during deposition to induce the preferred magnetic anisotropy.

During sputtering, ions of an inert gas like argon are accelerated into a target consisting of a suitable material. These ions knock free atoms from the target, which deposit themselves as a film on the substrate. Sputtering allows layers of different materials to be vacuum-deposited on top of each other to form a completed circuit (c).



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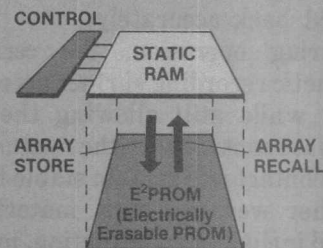
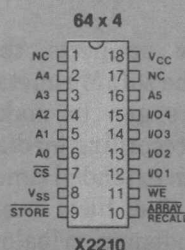
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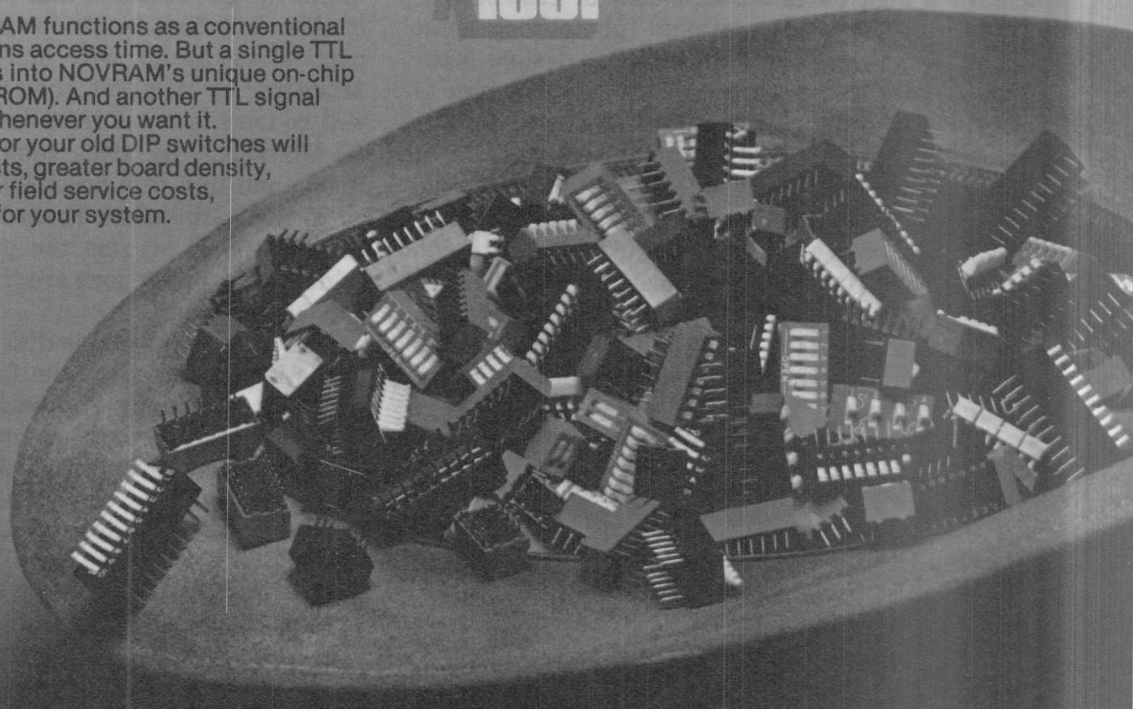
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magnetic head life appreciably, since it would wear off relatively quickly.

In the case of Life Time Ceramic (LTC) heads from Nortronics (Minneapolis, MN), ceramic extends from both sides of the magnetic head area that is in contact with the recording medium. Of course, it does not cover the magnetic core gap itself, nor does it cover the necessary width of the magnetic core on either side of the gap, which must be exposed to the recording surface for signals to be recorded and played back accurately.

During operation, the ceramic supports the magnetic recording surface across the soft Mu-metal cores while still allowing the core gap to make intimate contact with the magnetic recording media. This contact will remain stable for an extended time.

Other wear-resistant materials that have been tested include chrome plating, molybdenum, tribaloy and tungsten, and tungsten carbide.

The shallow-throat problem

Two well-established types of inductive thin film-head design—the helix and the spiral—have evolved for disk drives, both having a yoke structure common to virtually all thin-film conductors. Each type has a long list of advantages and disadvantages. As for the latter, neither type of head, for example, can achieve a high magnetic efficiency or ease of film processing using conventional photolithographic techniques. Another drawback of both designs is the small height of the throat, which runs the risk of early degradation of the head's electrical performance due to even a small amount of wear.

The first commercially announced thin-film head for tape drives (ELECTRONIC DESIGN, Nov. 8, 1980, p. 28) eliminates the accepted yoke structure and replaces it with one that lends itself to the application of thin-film conductors away from the critical throat area of the yoke (see "How a Thin-Film Head Is Made"). The output characteristics of the isolated coil design compare favorably with these of a

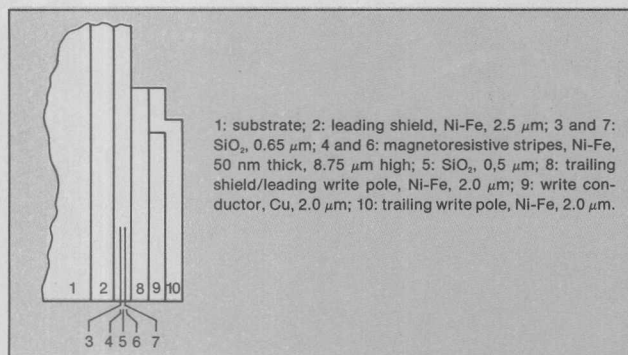
magnetoresistive (MR) read head. Furthermore, it makes optimum use of the track width for any number of turns.

The design, aimed at ½-in. tape, features over 20 turns/track and can be made with a minimal number of processing steps. Even better, placing the top pole to the side of the bottom pole yields a less restricted throat height. That results in turn in a longer magnetic yoke length, but it is more than compensated for by the reduced flux leakage between the poles.

Both floppy and Winchester disk drives do not yet have the luxury of two-gap heads or separate erase heads, as these, for all practical purposes, require a magnetoresistive approach (Fig. 5). Only the tape drive heads fall into this category for the time being. The problem is the development of magnetoresistive heads. Such activity for Winchester disks has intensified in the past few years, but the only announced product development has been by IBM at technical conferences (ELECTRONIC DESIGN, June 11, 1980, p. 46).

Present ferrite-based digital recording head technology, which now supports 3 to 6 Mbits/in., is rapidly reaching practical limits. Thin-film technology offers areal densities of 10 Mbits/in. initially and the potential of reaching densities of 100 Mbits/in. The scenario that many experts agree on is this: thin-film heads in conjunction with thick particulate media will increase densities to 15 Mbits/in.² by late 1981, then thin particulate media will be used to boost areal densities to greater than 20 Mbits/in.². By 1985, combinations of thin-film media and thin-film heads will push areal densities to 35 to 40 Mbits/in.². From 1990 on, when vertical recording will become the primary technique for digital data, projections are that areal densities will hit 60 Mbits/in.².

The drive to announce disk drives with thin-film heads is undeterred by the fact that there are two different processing approaches to fabricate such heads. One approach is to use an inductive read/write transducer in which the coil structure can be arranged in two layers to maximize the coil's efficiency and to minimize the distance from the head's gap to the magnetic yoke closure. This approach also lends itself to fabricating and integrating the read/write transducers into or onto rails of a conventional flat air-bearing slider using semiconductor processing. Preliminary tests on commercially available thin-film heads indicate that an 85% encoding efficiency at 10,000 flux reversals/in. can be achieved. The flying height of the head to the disk surface on the inner diameter can now be reduced to less than 13 μ in., and in some cases to less than 5 μ in.

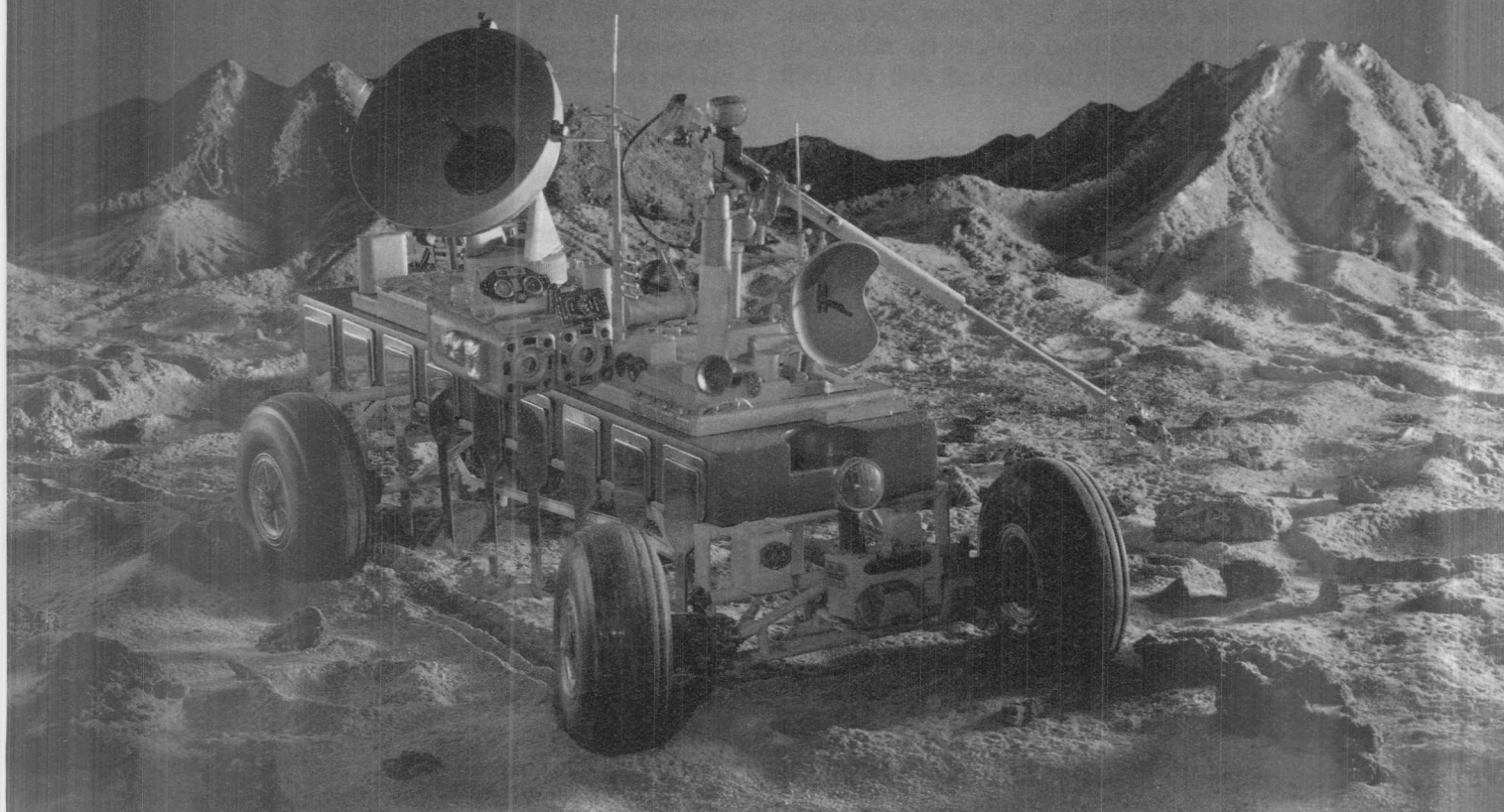


1: substrate; 2: leading shield, Ni-Fe, 2.5 μ m; 3 and 7: SiO₂, 0.65 μ m; 4 and 6: magnetoresistive stripes, Ni-Fe, 50 nm thick, 8.75 μ m high; 5: SiO₂, 0.5 μ m; 8: trailing shield/leading write pole, Ni-Fe, 2.0 μ m; 9: write conductor, Cu, 2.0 μ m; 10: trailing write pole, Ni-Fe, 2.0 μ m.

5. A magnetoresistive read head lends itself to applications in recording systems with very high track densities because of the high ratio of its output signal to the track width. (Courtesy of Information Magnetics Corp., Goleta, CA)

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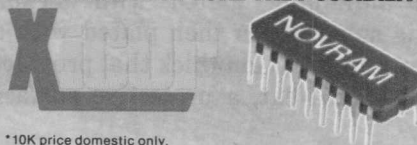


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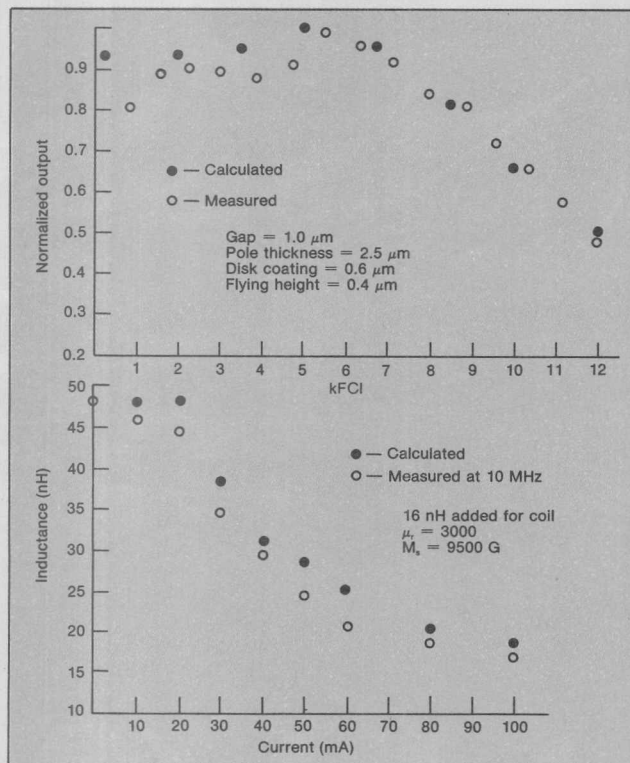


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The geometries that have been made public from Dastek (Los Gatos, CA) are: pole tips of $2\text{ }\mu\text{m}$ read/write gap of $1\text{ }\mu\text{m}$, and a closure distance of $75\text{ }\mu\text{m}$ (Fig. 6). The heads also feature an inductance of 60 nH (ELECTRONIC DESIGN, March 31, 1981, p. 129).

In another approach to manufacturing thin-film heads, vacuum deposition, photolithography, and dry etching are used to make the critical magnetic pole pieces. This approach, by Magnex (San Jose, CA), is expected to yield head designs for achieving densities of 12 to 16 kbits/in. and 600 to 1000 tracks/in.



6. Thin-film head designs can be modeled by computer for both resolution (a) and saturation characteristics (b). Such modeling takes into account the coil inductance and the transfer function of the head. (Courtesy of Storage Technology Corp. Louisville, CO.)

Future plans at many manufacturers are to introduce both multigap heads for improving access time and multiple heads per disk. Furthermore, products with magnetoresistive heads will be introduced for both floppy-disk and tape drives.

The most recent example of a thin-film disk being considered for a future product comes from Datapoint Corp.'s Peripheral Operations Division (Sunnyvale, CA). The company chose to make the thin-film disk from aluminum plated with nickel-phosphorous. This substrate is then plated with a cobalt-nickel layer 0.15 to $0.3\text{ }\mu\text{m}$ thick that provides a coercivity of 625 Oe . Next, a protective surface

coating of carbon, ranging in thickness from 0.1 to $0.15\text{ }\mu\text{m}$, is deposited.

To evaluate the wear resistance of the carbon coating, Datapoint tested the following thin-film types: carbon-coated, hard cobalt oxide, soft cobalt oxide, rhodium, and 3350-particulate media. The results favored carbon-coated thin-film disks on which the data had been recorded before coating. At the end of 10,000 start/stop cycles, no errors or defects could be found. What's more, the signal response did not degrade even after permanent wear marks occurred on the surface.

One of the major recording problems to be overcome when using thin-film disks is the head fringing effect—two magnetic components paralleling the edge of the head that can also read or write data. Winchester heads have the comparative advantage of producing only one parallel component. The way to minimize the fringing effect is to either narrow the transducer read/write gap or develop a chemical process that offers the best noise level.

Thin-film media

What are the chances that thin-film or plated disks will be in widespread use by 1982? Probably not as remote as experts had predicted one to two years ago. The industry has seen Winchester products announced in 1980 and 1981 that employ plated disks. Now comes the acid test of long-term stability.

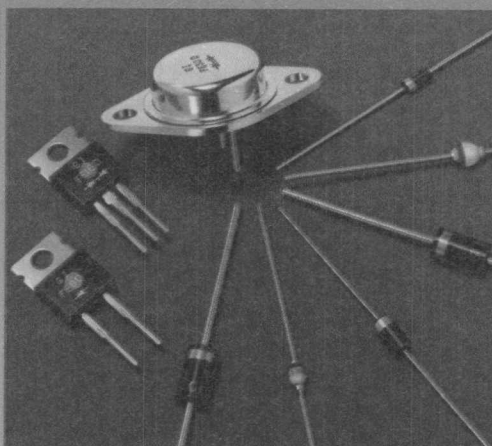
Long-term stability was, in fact, the primary obstacle to industry acceptance of thin-film and plated media. Disk drive designers questioned the ability of the media to hold up under environmental stresses like long-term oxidation of the media, the difficulty of reproducing the magnetic properties in a manufacturing environment, and its relatively poor wear resistance.

However, the advantages are considerable. These thin continuous metal films boast thinner oxide coatings, higher coercivities (as seen in the research of floppy disks), and other more favorable magnetic properties. For example, thin-film coatings are typically 1 to $5\text{ }\mu\text{in.}$ thick, versus 40 to $120\text{ }\mu\text{in.}$ for particulate coatings. The thinner oxide layer leads to better demagnetization properties at high bit densities and to better off-track performance at high track densities. What's more, the thinner the recording surface, the easier it is to overwrite old data.

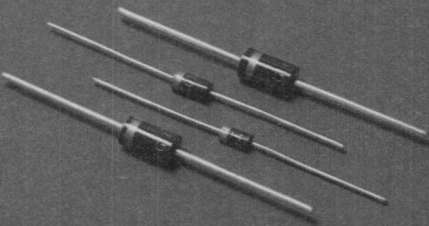
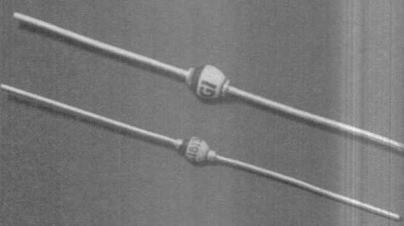
According to Francis K. King of Datapoint, the combination of thin-film disks and conventional Winchester heads, which fly over the surface at a stable height of $8\text{ }\mu\text{in.}$, do not push the technology limits. The next generation of products can boost the recording density up to 16,000 flux reversals/in. More speculatively, future thin-film heads may well increase the recording density of 25%. □

WANTED:

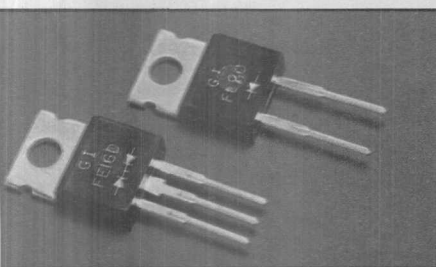

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Maximum Forward Voltage	.82-.95 volts	.82-.95 volts
Maximum DC Reverse Current	50 ua $T_A = 150^\circ\text{C}$	50 ua $T_A = 150^\circ\text{C}$
Maximum Reverse Recovery Time	25, 35 and 50 nSec	25, 35 and 50 nSec
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CIRCLE 42



The limits on speed and density keep getting pushed back, thanks to ever-tighter processing controls, redundant elements, and automatic error-detecting and error-correcting chips.

Semiconductor memories— there's no end in sight

Memories of all types have been the spur, and the testing ground for almost every new process for semiconductors. Recently, the results have been startling, to say the least:

- 64-k dynamic RAMs and lab samples of 256-k memories
- 64-k CMOS static RAMs
- Sub-40-ns NMOS static RAMs
- 16-k EEPROMs
- 128-k UV EPROMs
- 64-k bipolar PROMs.

These are just some of the developments that have become a reality this year, and as sure as there will be a tomorrow, even denser, faster devices will be coming.

Making all these advances possible, of course, are improvements in processing and lithography, which permit tighter and tighter control of impurities and line spacings and widths. The better the control, the smaller and closer together the devices can be placed on the chip, and thus the denser—and faster—the memory will be.

The problems of density

Try as they might to make every part perfect, memory manufacturers are always faced with what to do when one of just a few bits are bad in a memory chip. Until Bell Laboratories (Murray Hill, NJ) announced it had extra bits on a memory chip that could be programmed into the array to replace defective cells, few firms had given serious thought to the

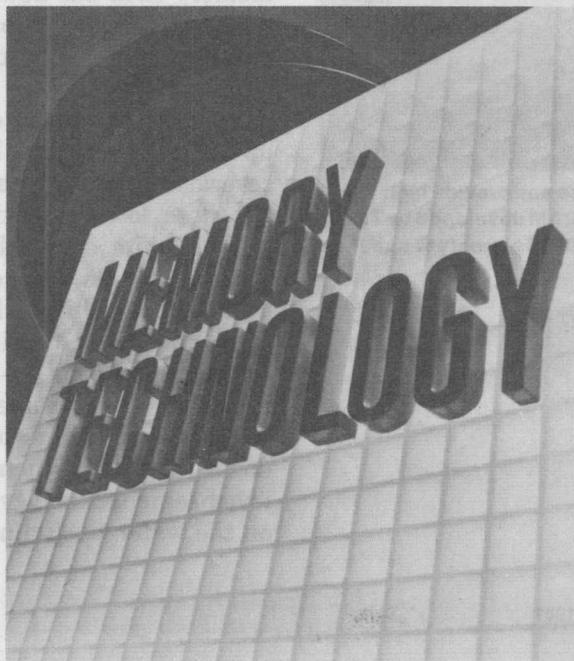
use of redundant cells, and the defective chips were either scrapped or sold as partials.

There were, of course, other reasons as well why redundant techniques were not used any sooner. Memory densities did not justify the added complexity that redundancy requires—at the 16-k dynamic RAM level, for example, the redundant circuitry would take up close to 10% of the chip area. However, at 64 k, the redundancy is only 1% or 2% of the chip area. For future generations, the extra circuitry will take up an even smaller percentage of the chip area, thus making it even more economical.

But redundancy is not a panacea: There are still many possible failures that it cannot correct—those of the bias generators, clocks, input or output buffers, and other subfunctions. Also, arrays that do not need to connect each cell to the power bus (dynamic RAMs, for example) will have a higher percentage of defects that can be fixed than other types of cell structures.

Whatever its virtues, many companies are still at odds with each other over what form the redundancy should take, how much to include on chip, and how it should be programmed into the array. For example, many manufacturers can refer to their own studies to say that so many rows and/or so many columns of extra cells should be used.

The number of rows or columns added does have a practical limit—if increased beyond that point, the chip yield will not only stop increasing but will actually start to decrease, since defects in the redundant areas will become more notice-



Dave Bursky
Semiconductors Editor

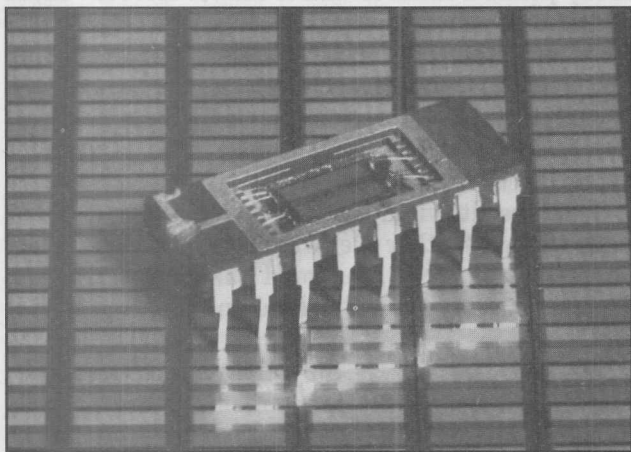
Memory Technology: Semiconductors

able. Various manufacturers have solved the problem in different ways. For instance, Inmos (Colorado Springs, CO) uses two redundant columns for its IMS1400 16-k static RAM.

Two choices for redundancy programming

Not only do the number of rows or columns differ from one manufacturer to another, but so does the programming technique. Intel and Inmos, for example, both use current pulses to burn open the fuse links to program the redundant areas, whereas Mostek has taken the laser path. Both methods are well-established production techniques, but few companies have adopted the laser approach, because it raises a question of long-term reliability. The problem is that the laser beam burns out the link under a layer of glass passivation, and that may lead to the regrowth of the link or some form of contamination.

Still, the laser is gaining acceptance, especially since Bell Labs announced that all of its 64-k dynamic RAMs are being programmed with laser zapping. Since then, only Hitachi (San Jose, CA), in addition to Mostek, has publically committed itself to laser programming. The two firms have opted for the laser for additional density: Since no large currents have to wend their way around the memory, the fuses can be placed anywhere on the chip and be made with minimum feature sizes. Current-zapped fuses, on the



1. Using an epi layer to minimize noise and provide high performance, the TMS 4164 64-kbit DRAM developed by Texas Instruments is the first commercial NMOS memory to use an epi layer.

other hand, are usually limited in number and located before the decoders, and they require some large transistors to control the high currents needed for programming.

Laser zapping, however, requires special dedicated systems on the test floor. These laser systems typically cost several hundred thousands of dollars, and companies are reluctant to spend that much, especially when reliability questions are still unanswered. For current-pulse programming, in contrast, low-cost additions to already existing test equipment can easily be added to blow the links, and many firms will take this lower-initial-cost route.

In the labs

What researchers do in the laboratory usually takes several years to become produceable in any sort of volume, so that a look at such work reveals what may be in store. In the dynamic memory area, bits and pieces of 256-k RAMs are now being evaluated at most major RAM manufacturers. In Japan, several firms have already started to sample first silicon of entire 256-k devices internally. The Japanese companies have taken two approaches—although Nippon Telegraph & Telephone Public Corp. (Tokyo) has developed a 256-k chip that includes redundant cells, Nippon Electric Co. (Tokyo), Toshiba (Tokyo), and Hitachi (Tokyo) do not agree that redundancy is the way to go, especially if the memory moves very rapidly down the learning curve.

Most of the samples now being evaluated are much slower than their makers would like—access times are about 200 ns, which will be too slow for most applications when the RAMs are introduced in 1983 or 1984. System manufacturers will need devices accessing in 100 to 150 ns, with 100 ns the target by 1985.

As for 64-k dynamic RAMs, just about every memory firm has now started to supply customers with sample production parts. In fact, several companies—Texas Instruments (Dallas), Motorola (Austin, TX), Fujitsu (Santa Clara, CA), Toshiba (Irvine, CA), and a few others—have already cranked up their production lines and are churning out several hundred thousand units a month. Very shortly, those low quantities will increase to about a million units a month, especially as the price of dynamic RAMs has now been driven down to less than \$20 per chip in high volumes.

Of all the 64-k chips introduced, most had no surprises technically—improved processing, fineline lithography, and some redundancy were the major points most vendors pushed. There were two standouts from that, though. Texas Instruments employed some technology tricks and an epitaxial layer on the wafer to eliminate the need for the backbias

generator and therefore its chip uses a grounded substrate (Fig. 1). The latter, in turn, simplified the design of the memory and gave a very small chip size, along with some top performance specifications.

The other surprise came from Inmos in the form of a part that offered a serial nibble output, in addition to its regular 1-bit output, and CAS-before-RAS self-refreshing. Although it is questionable how many people will use the self-refreshing, those that need top performance will probably be happy with the nibble output. This

mode permits the memory to serially send very quickly 4 sequential bits, with the first bit requiring the normal access time and the next three requiring just 50 ns each.

The next aspect of these parts to be enhanced will be speed. Most companies initially expected to have a considerable number of 150-ns devices available immediately, but it turned out that the bulk of the units access in 200 ns. Now, with some fine-tuning of the production line and a tweak of the masks, most manufacturers anticipate that by year-end the ma-

Bubble memories are alive and well

Although three of the main proponents of magnetic-bubble technology—National Semiconductor, Rockwell, and Texas Instruments—have withdrawn from the commercial market, the other vendors believe that the technology is alive and growing. Still offering the largest commercial array, Intel (Santa Clara, CA) will quadruple density in late 1982 with the introduction of a 4-Mbit device. In the meantime, Fujitsu (Lake Bluff, IL) is trying to get its 1-Mbit unit on the market.

Prices for bubble memories are also staying in line with Intel's predictions, with the 1-Mbit set, the BPK-722-2, cut to \$995 for a single unit and down to \$595 a piece for 5000 units. Also, users who fear the lack of an alternative source may fear no longer—Intel is expected to close a second-source agreement in the near future.

Manufactured with many of the same lithography and processing steps needed to produce ICs, magnetic-bubble memories draw even faster on the advances in process technology than do memory ICs, since there are fewer masking steps and therefore fewer critical alignments. However, the exotic techniques that might eventually eliminate the external magnets and coils of wire are still several years away, even though researchers at Bell Laboratories (Murray Hill, NJ) and at IBM (San Jose, CA) have reported good results from experimental devices.

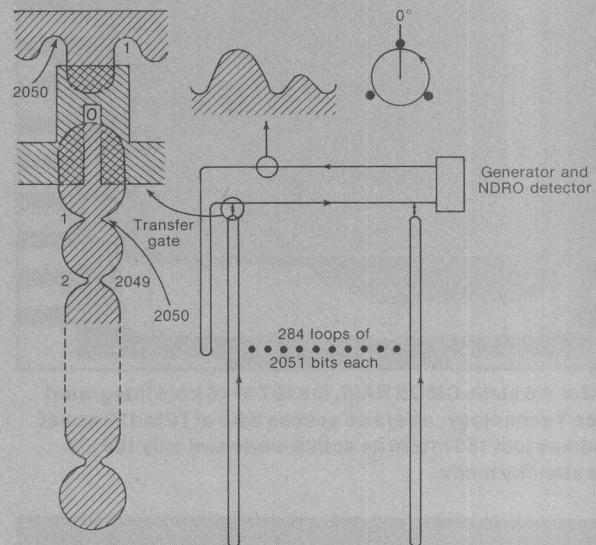
For example, researchers at Bell Labs are using ion implantation to pattern half-megabit chips. Bubbles with diameters of 1.7 μm were used on a 6-to-8- μm period and were propagated by rotating fields of 40 Oe at 50 kHz. These chips, which are 5.22×9.3 mm, have 284 loops of 2051 bits each (only 258 loops are required for the chip to be functional). They have shown that ion-implantation technology can yield large-capacity nonvolatile bubble memory devices.

Magnetic-bubble technology, though, can go well beyond 4 Mbits on a chip. In fact, Bell Labs has already made an experimental 8-Mbit part.

Before getting out of the business, National Semiconductor had discussed a 4-Mbit unit that put out 4 bits, thus eliminating one of the faults in bubble systems—the long serial input and output times. Instead of formatting data from an 8- or 16-bit parallel

word into a serial data stream, 4 bits at a time could be stored. Although this chip was only experimental, it showed that multiple-channel memories are possible.

Intel's planned 4-Mbit part, on the other hand, is a single-channel unit, and an external formatter must arrange the data for storage or recall. Like all bubble memory chips, it requires an entire family of silicon support components for the coil driving, function control, formatting, and error detection and correc-



tion. In 1982, Intel will introduce not just the 4-Mbit chip, but a complete set of support components as well.

What with all this activity by bubble manufacturers, the memories are now starting to find their way into end-user microcomputer systems. In Japan several companies have designed in the Fujitsu Bubble Cassette, and in the U.S. all vendors have one type or another of plug-in bubble cartridge for easily removable and transportable storage. Currently, Intel offers a 1-Mbit plug-in bubble cartridge; and Fujitsu offers a 256-kbit unit, with a 1-Mbit version planned for later this year.

Memory Technology: Semiconductors

jority of units shipped will be 150-ns parts.

Another enhancement that is bowing this year is a dynamic RAM with a nibble-wide output. Organized as $16\text{ k} \times 4$ bits, the memory fits right into several system organizations. For example, systems that do not have to grow in 64-k increments are prime targets. Moreover, only two chips would be needed to add 16 kbytes to the system—a very compact alternative to adding eight $16\text{-k} \times 1$ chips or eight $64\text{-k} \times 1$ devices. Housed in a 20-pin DIP, the nibble-wide RAM will be a major option for small-system users that want the benefits of dynamic RAM but don't want to expand the system in large increments.

Living with soft errors

As the dynamic RAM memory cell becomes smaller and smaller to fit more bits per chip, the capacitance of the cell decreases, and that makes the cell more prone to soft errors due to alpha

radiation. Memory manufacturers have taken various precautions to minimize the radiation that hits the chip—such as polyimide coatings and low-radiation packages—but chips still get random hits, and systems must take precautions to make sure those soft errors don't cause the computer to make a mistake.

Coming to the aid of the various memory vendors are a half-dozen or so error-detection and correction (EDC) circuits. Firms that offer or will offer such circuits include Intel, Advanced Micro Devices (Sunnyvale, CA), Monolithic Memories (Sunnyvale, CA), Motorola, Texas Instruments, National Semiconductor (Santa Clara, CA), and Fujitsu. Most of the chips can detect both single and double-bit errors and correct single-bit errors, and all are oriented to 16-bit systems. However, all of the circuits are also expandable to larger-word memory systems.

EDC chips are intended for dynamic memory systems, though they can be used in static ones too. It's just that most static memory systems are generally much smaller than dynamic systems, and EDC is rarely used for systems of less than 64 kbytes. To complement the EDC chips, the manufacturers usually have a complete dynamic RAM support chip set that ties into the EDC circuit. These support chips provide the refresh control for the RAMs, bus buffering for large systems, and in some cases error logging and warnings to the main system.

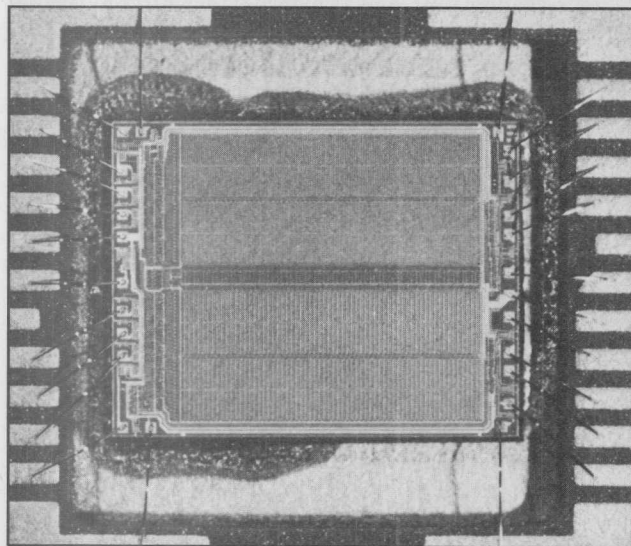
One of the problems with EDC circuits is the delay they typically introduce into the memory cycle. Most vendors have been able to keep the delays relatively short—below 50 ns—so that errors can be detected within the regular memory cycle. However, if an error is found, another 50 to 80 ns might be required to correct it and rewrite the data into the memory.

This speed penalty is another reason why EDC is rarely used with static RAMs. Most static memory subsystems often access in less than 100 ns, and an overhead of 50 ns or so would drastically slow down the overall system. Static RAM, subsystems that do use EDC usually must have the circuitry built with ECL-based technology to obtain extremely fast detection.

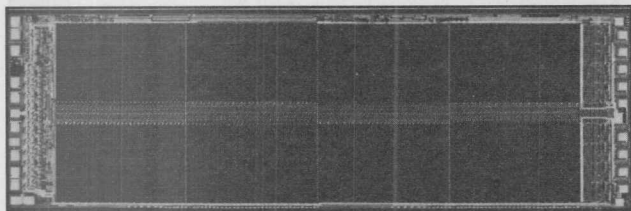
Static RAMs get faster and faster

As mentioned, static RAMs are most often used when small amounts of memory are needed or system access times are extremely short. Over the last few years, process developments such as Intel's HMOS and Mostek's Scaled Poly 5 have shrunk cell sizes to about 1 square mil. This small size yields two major results—high density and high speed.

In terms of density, many manufacturers have introduced or will shortly introduce very fast 16-k statics. Some are organized as $16\text{-k} \times 1$ bit; others



2. A $2\text{-k} \times 8$ static CMOS RAM, the IDT 6116 from Integrated Device Technology, offers an access time of 70 to 120 ns yet consumes just 180 mW in its active mode and only $100\text{ }\mu\text{W}$ in the standby mode.



3. Containing 2048 bytes of static RAM storage, the MK4802 from Mostek offers access time of less than 100 ns.

are set up as $2\text{-k} \times 8$; and by early 1982 some firms will offer $4\text{-k} \times 4$ versions. When it comes to speed, the leading edge is in the 1 and 4-bit-wide parts, but some of the 8-bit-wide memories aren't too far behind.

Already available from three sources, with at least another three sources expected shortly, the 2167 type of NMOS RAM has surpassed its bipolar counterparts in density and rivals the best system speeds of all memory types except for the highest-performance ECL versions. Access times are in the 55-to-70-ns range for the fastest devices right now, and by next year versions should be appearing that access in as little as 40 ns. Intel, Inmos, and Mostek are the three companies now supplying the 16-k units, and all of them use redundant cells.

Going to CMOS to keep power low, Hitachi has come out with a version of the 2167, called the HM6167, that accesses in 70 to 100 ns. Hitachi's process uses double polysilicon and has channel lengths of $2\text{ }\mu\text{m}$.

The main difference between Hitachi's memory and the NMOS versions is in power dissipation, not speed. Typical standby power consumption is about $100\text{ }\mu\text{W}$, and the operating power rises to a mere 150 mW. In comparison, the 2167-type part draws about 75 mW on standby and well over 500 mW when active. However, prices for the CMOS versions are still much higher than for the NMOS ones, so that unless power is a critical concern, NMOS remains the mainstay technology.

Although the $16\text{-k} \times 1$ devices have the limelight, the 2147-type $4\text{-k} \times 1$ and 2148 $1\text{-k} \times 4$ memories retain plenty of life. Intel, for instance, has started supplying samples of the next mass revision of the 2147, which promises sub-35-ns access times. In addition, the chip's reduced size should translate into higher yields and lower prices. This version will also cut power dissipation by about 60%—down to just 40 to 60 mA when active and 10 to 12 mA on standby.

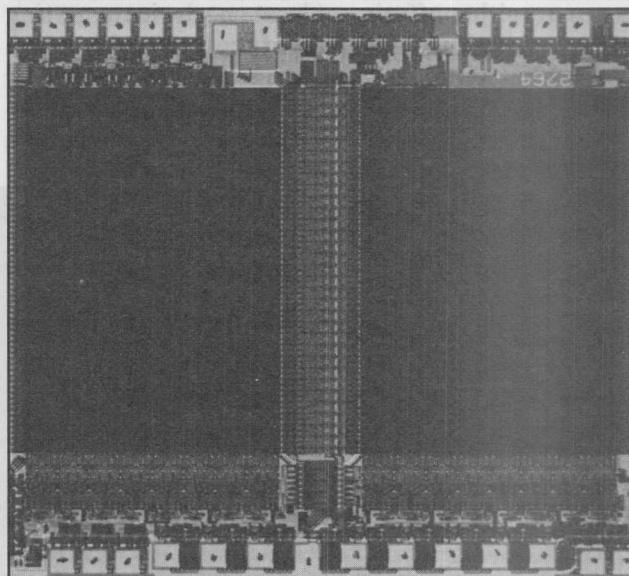
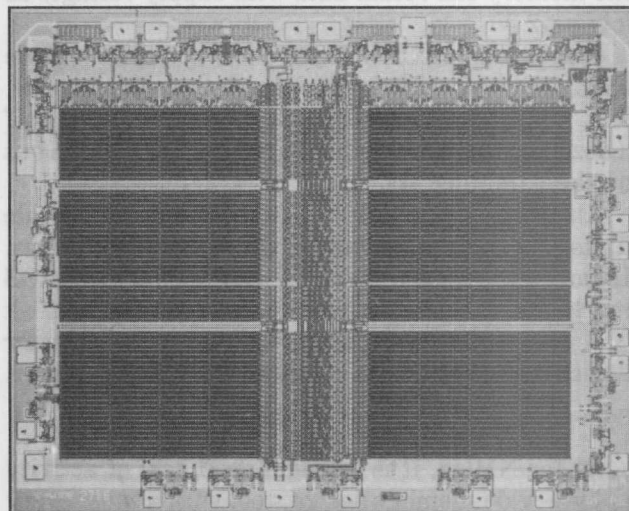
Intel is applying its shrinkage capability to other memory products, too, to get the benefits of smaller chip size, whether or not it also results in higher speed. As an example of what shrinkage can do, the 2114 was first reduced from 142×238 mils to 11×190 mils in the A revision. Now, the B version is ready, and it is just 99×155 mils—less than half its original size. This same shrinkage capability can be applied to all memories but does not stop there—all NMOS devices can be scaled down using the same rules.

CMOS memories cool things down

In maximizing speed, NMOS memories typically consume a lot of power, and that power consumption limits the memory capacity of the chip. CMOS does away with most of the power restrictions without

too great a speed penalty, as Hitachi illustrated with its HM6167. And in areas where blazing speed isn't needed, CMOS technology stands out even more as a low-power alternative.

Density has been one problem CMOS vendors have been trying to reduce, since with typical bulk CMOS the chip area for a 16-k RAM would be prohibitive. However, with the development of NMOS-compatible processing like Intel's HCMOS or the Iso-CMOS technology from Mitel (Ottawa, Ont., Canada), CMOS is rapidly catching up with NMOS's density and performance.



4. Using its UVEPROM compatible HMOS II process, Intel has been able to squeeze a 64-kbit UV EPROM (bottom) into a chip that is smaller than its production 2716 16-k UV EPROM (top).

Concentrating on CMOS technology, Toshiba has been able to make two versions of a 64-k RAM. Both are organized as $8\text{-k} \times 8$ bits but are made with different design rules. One uses polysilicon loads and is just entering the sampling stage. The other will use active loads and offer greater speed.

One recent entrant to the memory market is a new company, Integrated Device Technology (Cupertino, CA). Its first offering is a $2\text{-k} \times 8$ fully static RAM that accesses in 70, 90, or 120 ns (Fig. 2). When active, it draws just 180 mW, and that drops to 100 μW on standby. What's more, for emergency data retention the memory can retain data with supply voltages as low as 2 V.

Others making CMOS byte-wide memories include NEC, Hitachi, Harris Semiconductor (Melbourne, FL), and RCA (Somerville, NJ). About another half a dozen vendors are trying to get their memories out of the sampling stage.

Although most CMOS activity is in byte-wide units, work is also taking place in other areas. Important to note is the entry of Intel into the CMOS market with two alternative-source products, a $1\text{-k} \times 1$ and a 256×4 device—the prelude to faster devices made with the company's HCMOS process.

Byte-wide activity is not all CMOS

As for NMOS, it is seeing a good deal of activity in byte-wide memory design, too, with almost every company either offering at least one device or getting ready to sample one. Several of those out adopt some interesting schemes to compete with CMOS's low power consumption. For example, Mostek has developed a version of its fast 4802 $2\text{-k} \times 8$ NMOS static

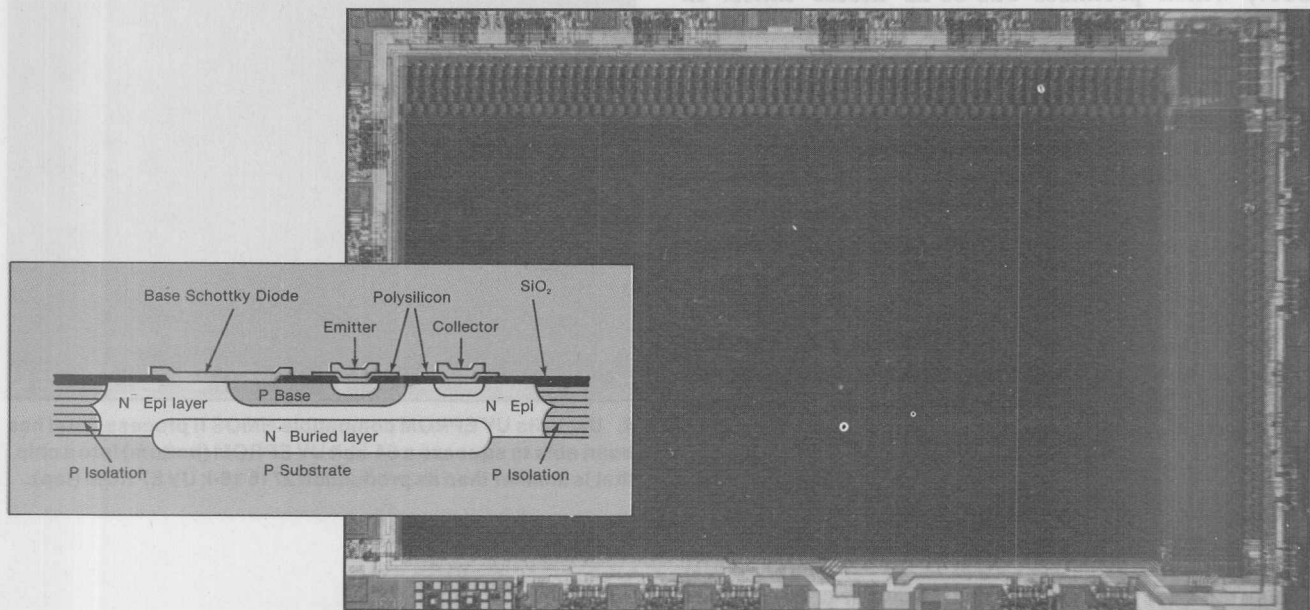
RAM (Fig. 3) with what it calls DataSave. DataSave permits the MK48D02 RAM to keep alive the memory array on just 100 μA if the power should fail. Although the memory uses a battery backup, it doesn't do so in the usual manner. Instead, to keep the array alive, a voltage of 2 to 6 V is placed on the write-enable input. Thus, the memory draws just 55 μA when normal power is shut off.

Clocked periphery saves power

Other techniques to save power yet keep speed high include the use of a clocked periphery along with a static array. In this case, the high-power components—the sense amplifiers, buffers, and decoders—are turned on only when needed. That means that they can afford to pay for higher speed with higher speed with higher power consumption, since they do not pull power all the time.

The alternative to a clocked periphery is the use of dynamic cells and full refresh support on the same chip—the pseudostatic RAM. Intel, Zilog (Cupertino, CA), Mostek, and National Semiconductor are the four companies making byte-wide self-refreshing memories. In addition, Mostek and Motorola have bit-wide dynamic RAMs that could be classified as pseudostatic.

In the fast byte-wide area, Mostek offers the 4801 and 4802 1 and 2-kbyte chips, which access in well under 100 ns. Toshiba also has a very fast 2-kbyte part, the TMS2016HP, which accesses in 35 to 45 ns. For access times in the 100-to-250-ns range, the number of manufacturers increases considerably. At the 1-kbyte density, GTE Microelectronics (Phoenix, AZ), NEC, and Mostek have several versions; and



5. Using four extra word rows, the Intel 3632 32-kbit PROM is the first commercial PROM to use redundancy to improve yield yet access in 35 ns.

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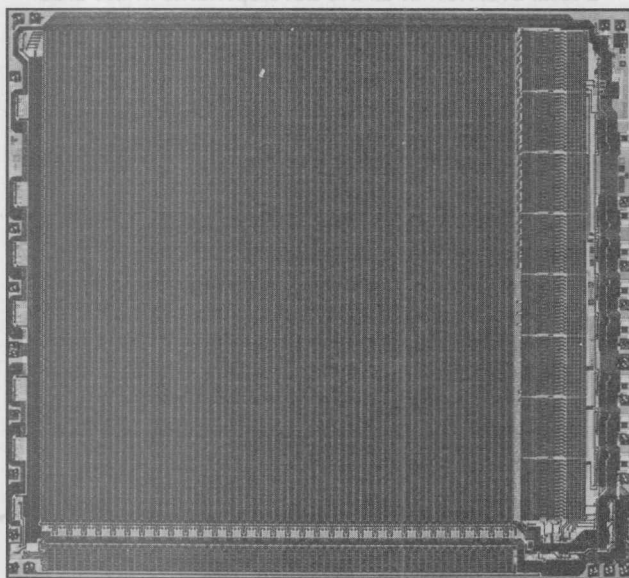
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Memory Technology: Semiconductors

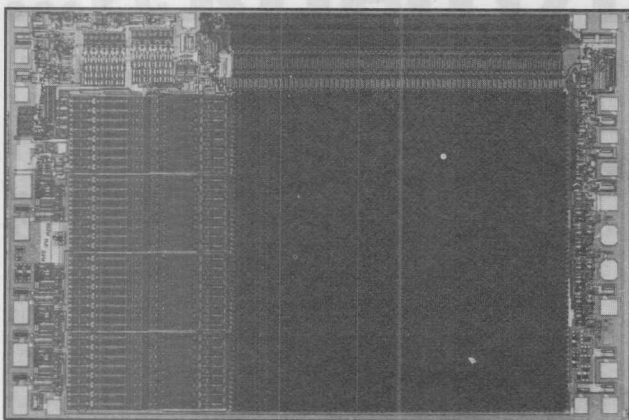
at the 2-kbyte level, Oki (Santa Clara, CA), Texas Instruments, Toshiba, and Mostek offer a mix of speeds.

Besides trying to reduce the standby power, some memory manufacturers have been working toward the ideal memory—the nonvolatile RAM. Several of those efforts are well along the way. Xicor (Milpitas, CA) of course, has already introduced three such products, organized as $1\text{-k} \times 1$, 256×4 , and 64×4 bits. In addition, General Instrument (Hicksville, NY) and Hughes Aircraft (Newport Beach, CA) plan to introduce nonvolatile RAMs in 1981, and Xicor expects to have a $1\text{-k} \times 4$ version ready then.

Xicor's parts operate from a 5-V supply for both reading and storing data and have much of the needed control circuitry on chip. To make the parts, the company combines a static RAM array with a one-for-one match of nonvolatile storage elements.



6. Packing 32-kbits onto a chip, the 82S321 from Signetics accesses in 80 ns and draws just $20 \mu\text{W/bit}$.



7. Offering a $4\text{-k} \times 8$ organization, the Am27S40/41 bipolar PROM, developed by AMD, has a 50 ns maximum access time and comes in a 20-pin 300-mil DIP.

In the electrically erasable nonvolatile memory area, the major firms are Intel, Hitachi, Hughes, General Instrument, Motorola, and Nitron (Cupertino, CA). Expected to enter the 16-k fray soon, is Motorola, and National Semiconductor is also readying a 2-kbyte unit.

Hitachi and Intel both have $2\text{-k} \times 8$ devices that are basically pin-compatible but employ different technologies—Intel a floating-gate NMOS structure and Hitachi n-channel MNOS technology.

Going it alone in CMOS, Hughes offers both a 512×8 and a $1\text{-k} \times 8$ EEPROM. Their speed matches that of the n-channel units, with the added benefit of much lower power.

One problem with most of the EEPROMs is that the system CPU must do all of the control when data is being stored. Addressing that problem, Intel will shortly unveil a controller that takes care of all the timing. That, of course, will be the forerunner of a chip that has both the nonvolatile memory and all the control circuitry. General Instrument is very close to supplying customers with samples of such a device, albeit with only 128 bytes of storage.

UV EPROM densities double

The UV EPROM has doubled in density about every 18 months in answer to designers' need for increased nonvolatile storage, and this year is no exception. Enter the 128-k chip from Texas Instruments. Designated the TMS25128, it uses a new cell structure that was unveiled at the 1980 Solid State Circuits Conference.

The UV EPROM market has been relatively stable except for the glut of 16-k devices that occurred in early 1981. Motorola, Mostek, Intel, TI, and National Semiconductor all have their 64-k units in production and are actively trying to make 128-k parts. Surprisingly enough, the Japanese are glaringly absent from the list of 64-k device manufacturers. However, expect to see most of the gaps filled in during the last quarter of this year and early next.

As mentioned earlier, Intel plans to scale down to improve density, and that will apply to the UV EPROM area too. In the works is a 128-k unit built with the firm's HMOS-E process. That process has already yielded a 64-k EPROM, the 2764, that is actually smaller than the 16-k part built with standard NMOS, the 2716—even though it has four times the capacity (Fig. 4).

One problem faced by manufacturers as memories are shrunk is that of scaling down and keeping track of the programming voltage. Because a shrinkage doesn't necessarily require the manufacturer to change the part number, users can readily get confused about the correct programming voltage. To eliminate that problem, one JEDEC committee has

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Memory Technology: Semiconductors

begun discussing standardizing some form of signature memory on the memory chip that would be programmed during manufacturing and would be read out by the programming tool so that it can automatically set the proper voltage levels and timing.

Such a signature memory will probably be adopted by EPROM makers and by JEDEC in 1983. However, the concept can be applied to any type of memory and will just as nicely fit the bipolar PROM families, which also depend on specific timing and current levels for programming.

Many directions for PROMs

Fuse-link PROMs, directed at the high-performance system, will continue in that direction, with higher densities and faster access times. Just introduced, for example, was a 64-k part from Harris Semiconductor. This device, the HM1-76641, gave up some speed for density, but is still pretty swift at 85 ns, maximum. Expected to be available in sample form next month, it is slated for full production by January, 1982.

Harris has also taken its CMOS technology and married it to the PROM to come up first with a 512×8 part and now with a $2\text{-k} \times 8$ device that accesses

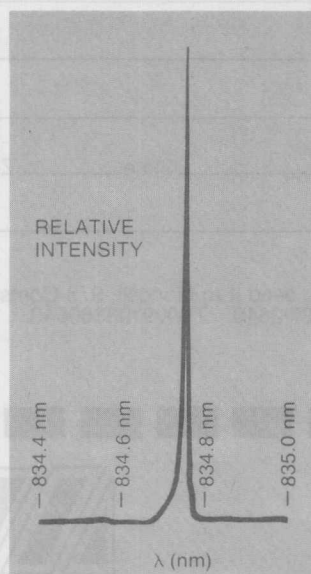
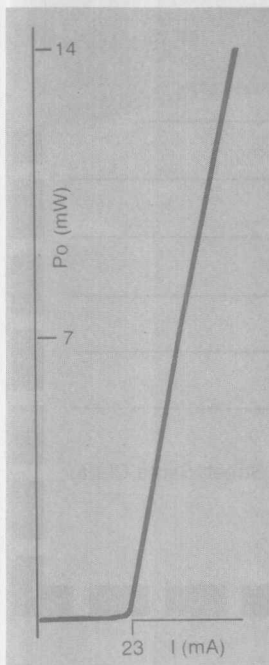
in about 200 ns.

Using its stacked-fuse technology unveiled at the 1980 ISSCC, Intel has just introduced a 35-ns 32-k PROM—claimed to be the fastest device at that density, and possibly even at the 16-k level (Fig. 5). Additional work at AMD, Monolithic Memories (Sunnyvale, CA), and Signetics (Sunnyvale, CA) is aiming at very fast devices—ones accessing in less than 20 ns as well as the high-density devices such as the 82S321 from Signetics (Fig. 6). Memories with this speed could serve as programmable logic, since PROMs provide every possible intermediate product term, whereas logic arrays and other forms of programmable logic only supply the final terms as outputs.

Although byte-wide parts are the most popular PROMs, demand for 4-bit organizations, such as the Am27S40/41 from AMD (Fig. 7), is considerable. This configuration fits very nicely into 300-mil-wide 24-pin DIPs, providing the designer with a very compact package for relatively deep storage (up to 4096 nibbles currently).

Finally, since many PROMs used in pipelined systems, many more units are starting to appear with output registers. That reduces the amount of external circuitry needed in the system. □

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MCDONNELL DOUGLAS	BUS25679 BUS27765	BUS8555 BUS8556	BUS8937	YES

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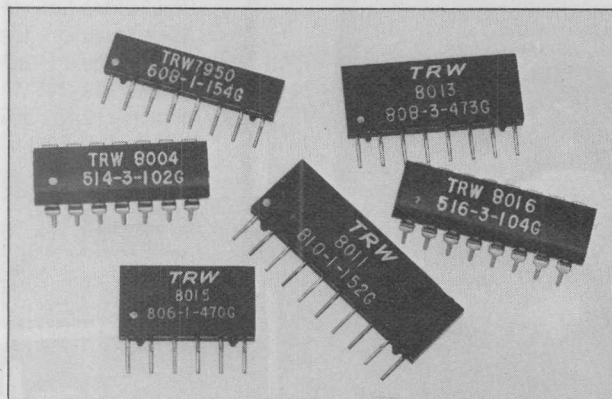
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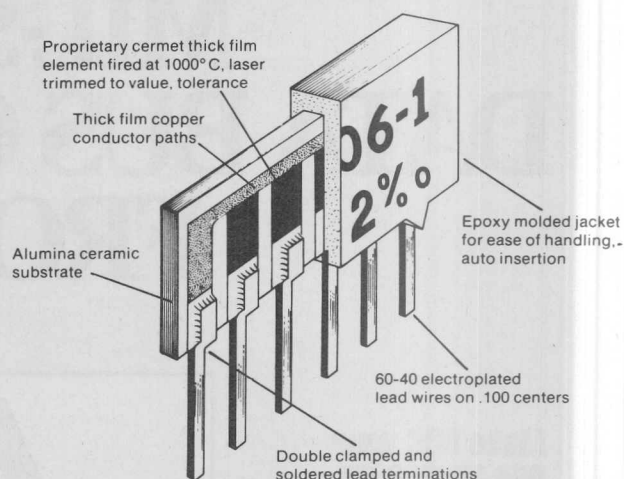
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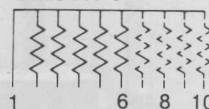
33	180	1.0K	5.6K	33K	180K
39	220	1.2K	6.8K	39K	220K
47	270	1.5K	8.2K	47K	270K
56	330	1.8K	10K	56K	330K
68	390	2.2K	12K	68K	390K
82	470	2.7K	15K	82K	470K
100	560	3.3K	18K	100K	560K
120	680	3.9K	22K	120K	680K
150	820	4.7K	27K	150K	820K
					1 MEG

ELECTRICAL SPECIFICATIONS

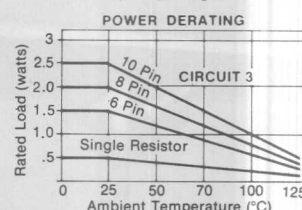
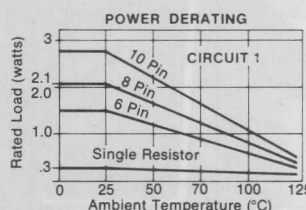
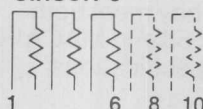
Resistance Range: 33 ohms to 1 Meg
Resistance Tolerance: $\pm 2\%$, $\pm 5\%$
Temperature Coefficient: ± 200 ppm/ $^\circ C$
TC Tracking: 50 ppm/ $^\circ C$ typical
Power Rating at $25^\circ C$: (see derating curve)
Circuit 1 6 Pin 8 Pin 10 Pin
Total package 1.5W 2.1W 2.7W
Single resistor .3W .3W .3W
Circuit 3
Total package 1.5W 2.0W 2.5W
Single resistor .5W .5W .5W
(Rating at $70^\circ C$ is 67% of $25^\circ C$ rating)
Maximum Continuous Working Voltage: 50V
Operating Temperature: -55° to $+125^\circ C$

STANDARD CIRCUITS (Resistors all same value)

CIRCUIT 1

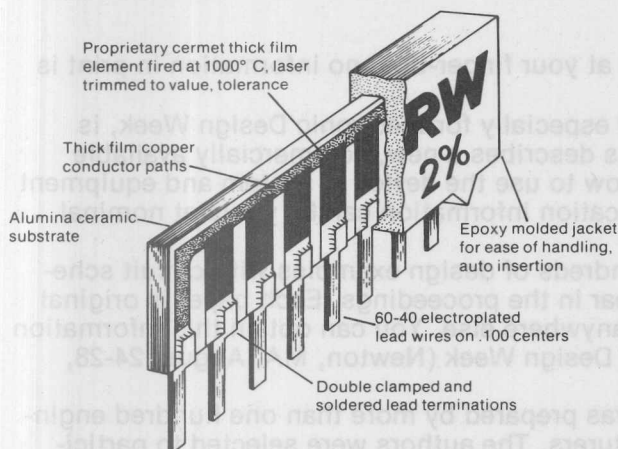


CIRCUIT 3



PART NUMBERS: 6 Pin: 806-1, 806-3; 8 Pin: 808-1, 808-3; 10 Pin: 810-1, 810-3.

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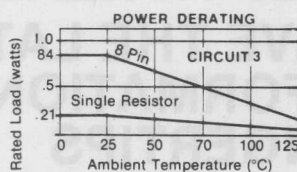
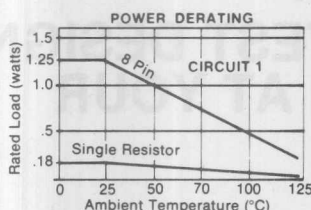
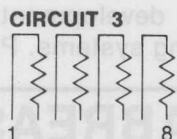
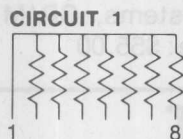
STANDARD RESISTANCE VALUES (OHMS)

33	150	680	3.3K	15K	68K
39	180	820	3.9K	18K	82K
47	220	1.0K	4.7K	22K	100K
56	270	1.2K	5.6K	27K	120K
68	330	1.5K	6.8K	33K	150K
82	390	1.8K	8.2K	39K	—
100	470	2.2K	10K	47K	—
120	560	2.7K	12K	56K	—

ELECTRICAL SPECIFICATIONS

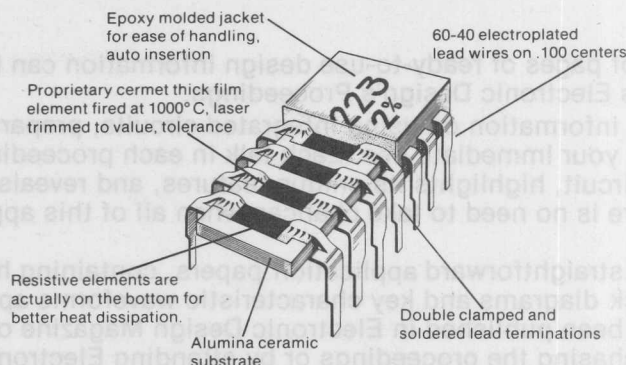
Resistance Range: 33 ohms to 150K
 Resistance Tolerance: $\pm 2\%$, $\pm 5\%$
 Temperature Coefficient: ± 200 ppm/ $^{\circ}\text{C}$
 TC Tracking: 50 ppm/ $^{\circ}\text{C}$ typical
 Power Rating at 25 $^{\circ}\text{C}$: (see derating curve)
 Circuit 1, total package - 8 Pin, 1.25W;
 single resistor - 8 Pin, .18W
 Circuit 3 total package - 8 Pin, .84W;
 single resistor - 8 Pin, .21W
 (Rating at 70 $^{\circ}\text{C}$ is 67% of 25 $^{\circ}\text{C}$ rating)
 Maximum Continuous Working Voltage: 50V
 Operating Temperature: -55 $^{\circ}\text{C}$ to +125 $^{\circ}\text{C}$

STANDARD CIRCUITS



PART NUMBERS: 8 Pin: 608-1, 608-3.

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STANDARD RESISTANCE VALUES (OHMS)

33*	100*	330*	1.0K*	3.3K*	10K*	33K*	100K*	330K*
39	120	390	1.2K	3.9K	12K	39K	120K	390K
47*	150*	470*	1.5K*	4.7K*	15K*	47K*	150K*	470K*
56	180	560	1.8K	5.6K	18K	56K	180K	560K
68*	220*	680*	2.2K*	6.8K*	22K*	68K*	220K*	680K*
82	270	820	2.7K	8.2K	27K	82K	270K	820K

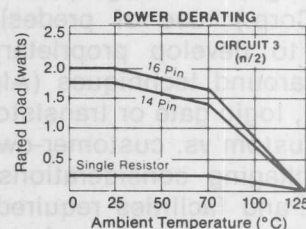
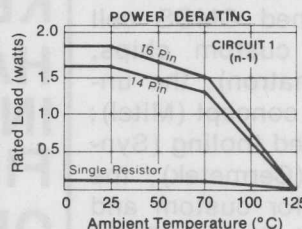
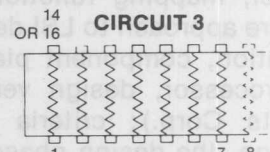
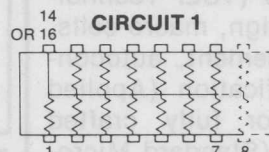
* Preferred Value

1 MEG *

ELECTRICAL SPECIFICATIONS

Resistance Range: 33 Ω to 1 Meg
 Resistance Tolerance: $\pm 2\%$ and $\pm 5\%$
 Temperature Coefficient: ± 200 ppm/ $^{\circ}\text{C}$
 TC Tracking: 50 ppm/ $^{\circ}\text{C}$ typical
 Power Rating 25 $^{\circ}\text{C}$: (see derating curve)
 Circuit 1
 Total package 14 Pin 1.625W 1.875W
 Single resistor .125W .125W
 Circuit 3
 Total package 1.75W 2.00W
 Single resistor .25W .25W
 (Rating @ 70 $^{\circ}\text{C}$ is 80% of 25 $^{\circ}\text{C}$ rating)
 Maximum Continuous Working Voltage: 100V
 Operating Temperature: -55 $^{\circ}\text{C}$ to +125 $^{\circ}\text{C}$

STANDARD CIRCUITS (Resistors all same value)



PART NUMBERS: 14 Pin: 514-1, 514-3; 16 Pin: 516-1, 516-3.

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SPEECH SYNTHESIS AND SOFTWARE ENGINEERING PROCEEDINGS [1981] S1

Nine conference talks are presented in this conference proceedings covering speech voice output integrated circuits and the role of software engineering in engineering design. Papers included are—

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LINEAR IC PROCEEDINGS [1981] L3

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MICROPROCESSOR/DIGITAL [INCLUDING TELECOMMUNICATIONS] PROCEEDINGS [1981] M4

Twenty-three papers are presented in this 477-page proceedings. Every paper was prepared especially for this conference and has not been published elsewhere. The following devices are covered—

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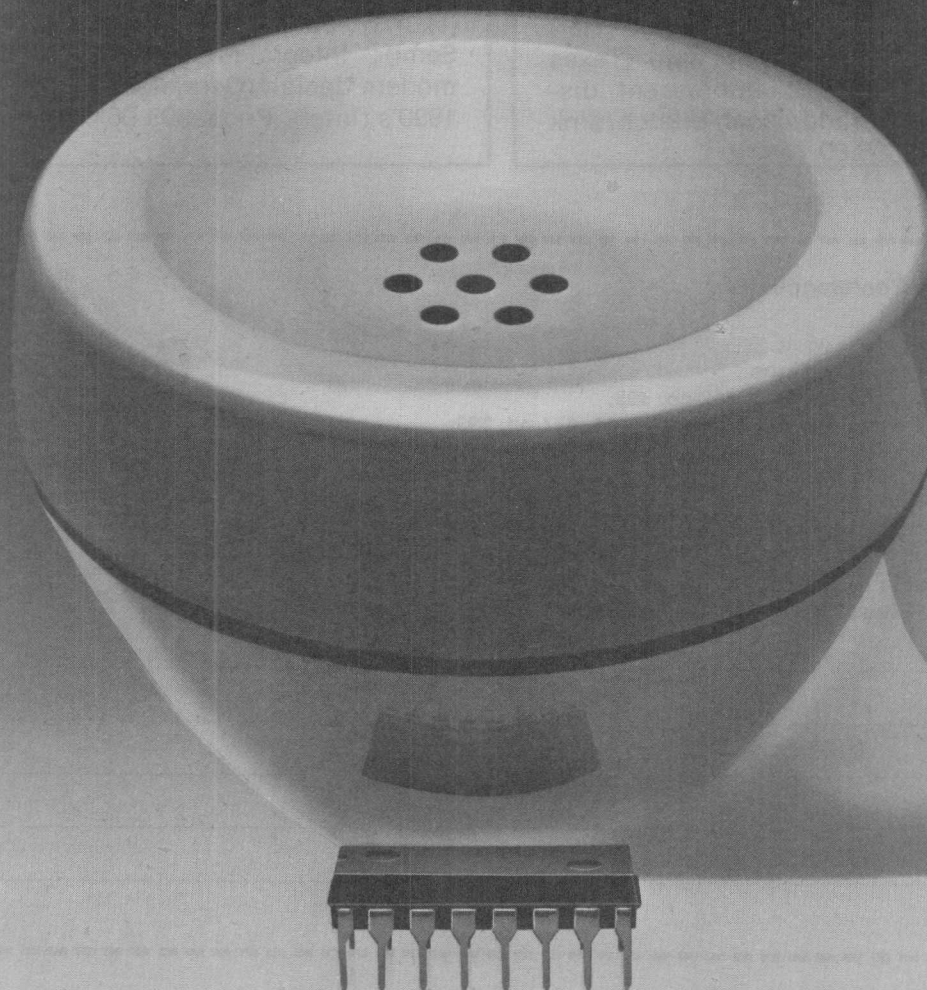
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With a cost potentially one-tenth that of magnetic tape as an attraction, optical disks are being groomed to supplant tape for read-only archival storage. But erasable optical-disks remain in research.

Optical disks loom as replacement for tape

The promise of optical disks—data storage at higher density and much lower cost than magnetic tape—appears destined to become a widespread reality in the next five years. New efforts by researchers are aimed at improving both the storage medium and the read/write lasers of the emerging system. As this work succeeds—and major laboratories are confident that it will—optical disk data storage will find a waiting market.

Consider this: The federal government alone is using about 27 million reels of computer tape, according to a projection by the National Archives (the agency concluded in 1975 that there were then nine million reels and that use was growing at an annual rate of 5%). Add to this the millions of reels used in banking, insurance, and other industries of the United States, and the savings with optical disks could be enormous. One study by an independent research group, Strategic Inc. (San Jose, CA), puts the cost of magnetic tape at \$0.02/Mbyte, against the \$0.002/Mbyte that is expected for a fully developed optical disk storage system.

The present storage medium for an optical system is typically a 12-in. disk coated with a thin film of tellurium. Data are stored in the form of micron-sized holes burned permanently with a laser into the disk's highly reflective metal surface (Fig. 1). To retrieve the information, a lower-power laser detects these holes as points of nonreflectivity on the surface.

There are several prob-

lems with this system that call for improvements. The major ones are these:

- The disk is a write-once medium; it cannot be erased.
- The thin layer of tellurium is unstable; it oxidizes and becomes useless in about 10 years.
- The error rate of the optical medium exceeds that of present storage methods.
- The gas lasers available today—argon for the write head and helium-neon (HeNe) for the read head—are costly. In addition, argon lasers are big and must be water-cooled.

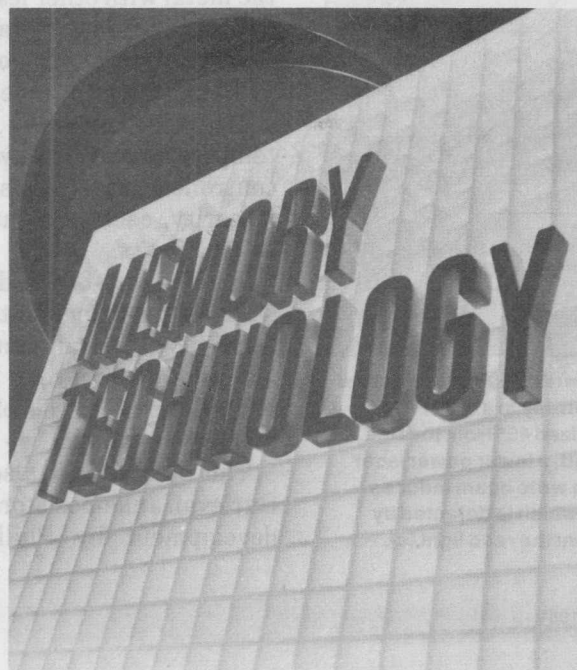
In general, the research efforts are aimed at getting more durable medium than tellurium and at developing smaller and cheaper semiconductor lasers.

Reaching for erasability

To address the problem of erasability, potential medium suppliers are attempting to develop alternative methods of storage to the burning of holes but that would still use lasers to read and write information. Two companies with programs in this area are Corning Glass Works (Corning, NY) and Energy Conversion Devices (Troy, MI).

According to a report on optical storage media by Strategic Inc., Corning is using a silver-halide film, while ECD uses a thin layer of amorphous semiconductors (noncrystalline glass).

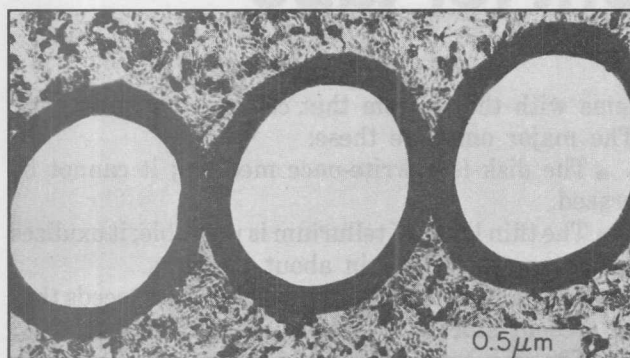
In Corning's approach, a linearly polarized helium-neon laser is used to write and erase; reading is done by a lower-powered gallium-



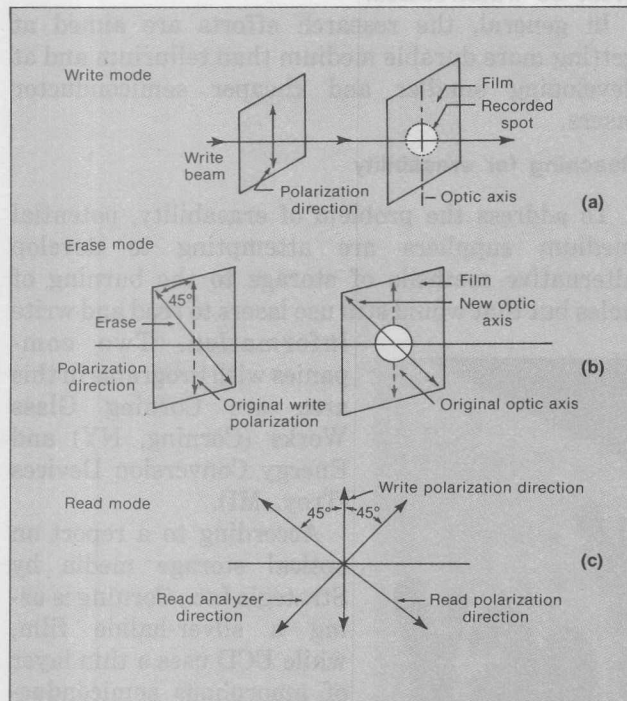
Memory Technology: Optical disks

arsenide semiconductor laser. Writing occurs when a polarized laser beam induces optical anisotropy in a spot on the medium (Fig 2). The bit is erased when the erase laser is rotated 45° from the polarization direction of the write laser.

During a read operation, the read laser, which has insufficient power to change the polarization of the spot on the halide film, applies its read beam to the spot. Like the erase beam, the read beam is rotated 45° from the polarization of the original write beam. The anisotropic spot reflects the beam with a birefringent effect (the refraction of light in two slightly



1. Submicron-size holes store the data in a Philips Labs' experimental optical disk system in a metal disk media.



2. With Corning's erasable media, a write beam (a) polarized in one direction induces optical anisotropy in a spot on the media. To erase, another beam polarized 45° from the first removes the anisotropy (b). During read, a lower power laser producing light polarized 45° from the write beam induces a birefringence in the recorded spot, which is detected by an analyzer crossed at a 90° angle from the read light (c).

different directions to form two rays), and the written bit is detected through an analyzer that is crossed at a 90° angle to the read polarization.

The lure of nonerasability

While erasability is desirable in many applications, there are others where a nonerasable medium might be preferred. For archival applications, for example, there is no real need for erasable media. Similarly, in the banking industry, it is a benefit to have a write-once storage element, like the optical disk, for auditing and security reasons. (Gone would be the days of a clever programmer loading some bogus account with electronically stolen funds. Now there would be a trail of transactions leading back to the thief.)

In transactions using a write-once storage system, a file could be written one day and updated sometime later. To accomplish the update, the entire file could be rewritten at another location on the optical disk. Then, a pointer could be in the out-of-date file directing the way to the current file. In this way not only would the computer system find the current file, but it would also have a complete audit trail with visibility back to the original file.

While this looks good on paper, there is one significant hitch: the software to implement this data-base management system. Current systems are structured around erasable files. To support a system that could keep track of every discarded file, while allowing rapid access to current files, would mean an entirely new systems approach.

The pros and cons of tellurium

In the volatility of its present medium, tellurium, the optical disk is also impeded. For archival storage users want up to 100-year storage lifetimes. Several solutions have been proposed, ranging from mixing the metal with other less-volatile substances to using entirely different storage mediums. At first glance, tellurium does not look that bad when stacked against magnetic tape.

The tape must be maintained at a moderate temperature in an environment where humidity is controlled (tape loves water). To maintain data integrity, each tape must be rewritten every three to five years.

A tellurium-based disk, on the other hand, can stand large swings in temperature, is unaffected by humidity, and can last up to 10 years before data are lost. Moreover, each disk can accept the equivalent of 40 reels of magnetic tape, a volumetric storage advantage.

The optical disk also lends itself to faster data retrieval. Juke-box storage systems, like those under development by Philips Laboratories (Briarcliff

Table 1. Comparing optical memory disks

Media type	Company	Erasable	Pregrooving, preformatting, prerecording	Use with semiconductor laser	Manufacture without vacuum system
Silver halide	Many	No	No	No	Yes
Tellurium	Many	No	Yes	Yes	No
Drexon media	Drexler	No	Yes	Yes	Yes
Bismuth	Many	No	Yes	Perhaps	No
Rhodium	OMEX	No	Yes	No	No
Titanium trilayer	RCA	No	Not likely	Yes	No
Thermodegradable/metal film	Thomson-CSF	No	Not likely	Yes	No
Solvent-coated	Kodak	No	Not likely	Unknown	No
Photodichroic	Corning	Yes	Not likely	Unknown	Unknown

Source: Drexler Technology

Manor, NY) and RCA Advanced Technology Laboratories (Camden, NJ), can store 25-million Mbytes of information, with access to any information in less than a minute. In addition, the information on any one optical disk is available by random access, unlike tape, whose stored information must be accessed sequentially.

Extending the medium's life

Researchers can build longer-lived tellurium-based disks by mixing the volatile metal with some alloy, as well as by sealing the surface with overcoats to prevent atmospheric elements from encouraging oxidation. Overcoats typically tested so far have included silicon dioxide and polymethyl metacrylate (PMMA). In addition, tellurium could be replaced with other metals or organic material. (For a partial list of alternatives, see Table 1.)

In seeking substitutes for tellurium, researchers are looking for media that would require low writing energy, be easy to read, be inexpensive to manufacture, and have a high signal-to-noise ratio with low readout error rates—all of this and long archival life, too.

Several alternatives that meet these criteria hold promise. They include a bubble-forming medium from 3M (Minneapolis, MN), Drexon from Drexler Technology (Palo Alto, CA), and a number of disks that use organic dyes instead of metal to hold the information.

In the bubble-forming disk, information is stored as well-defined submicron-sized bubbles, or blisters, in the top layer of a trilayered disk. The bubble-forming layer is made up of a thin, tough film of nonvolatile refractory material that absorbs light

easily. Beneath this is an optical spacer, and below that is a reflective metal layer. All rest atop a substrate of glass, polymer, or metal.

In operation, an argon laser with a 488-nm wavelength impacts the top film which absorbs the energy, which, in turn, produces heat. The heat prompts outgassing at that point on the layer, and this causes the film to bulge into a bubble. As the bubble forms, the spot grows reflective, thus producing a highly reflective spot on the disk surface, where before the spot was light-absorbing. The reflective spot can be read as a data site.

The reflective spot also self-limits the laser's effect. Since it no longer absorbs the light, the gassing resulting from the acquired heat stops, thus forming a uniform bubble of a specific size. To read the mark, a lower-powered, longer-wavelength (830-nm) diode laser is used to detect the high optical contrast between bubbled and unexposed areas of the disk.

The advantages to this medium are numerous. It needs only low writing power (4 mW), has a high carrier/noise ratio (50 dB), and appears to offer long life, since the bubbles, once formed, should remain raised for many years. 3M has tested the bubbles by mechanically attempting to cause them to deflate, and it reports they have survived these attempts. The temperature and humidity resistance of the bubble-forming medium are comparable to that of tellurium or better.

Drexon, another possible substitute for tellurium, is commercially available. It has a top layer, or crust, an underlayer beneath that, and a substrate layer below that (Fig. 3). In the crust, two types of submicron-sized metal particles are suspended and

Memory Technology: Optical disks

evenly distributed in an organic colloid (gelatinous substance).

One type of particle is a spherical reflective crystal used to achieve a high level of reflectivity. Like a tellurium disk, the surface resembles a mirror. The second particle is a black filamentary silver that absorbs heat readily. In operation, a laser beam hits the disk surface and heats the black particles quickly, thus causing the colloid to melt away at that point. This creates a spot of nonreflectivity in a highly reflective surrounding field.

Neither of the two particles is subject to oxidation; hence, there would be unlimited storage life. And the black particles heat so readily that little writing power would be required.

Using dyes for data storage

Dyes also are under consideration as data storage media, and they offer distinct advantages over metals. First, they can be made more cheaply. Then, the manufacturing process should also be less hazardous—tellurium manufacture involves handling toxic materials, which can create problems for workers, not to mention the added cost of safety precautions. Dyes are not subject to this problem.

Dyes should also require lower write power, thus making it possible to use less expensive and smaller semiconductor lasers when they become available in volume. The one drawback to dyes could be their lifetime under heavy data accessing, but little is now known about dye lifetimes.

Among the media that use dye/binder materials, two look very promising. One is from Kodak Research Laboratories (Rochester, NY) and the other from IBM (San Jose, CA).

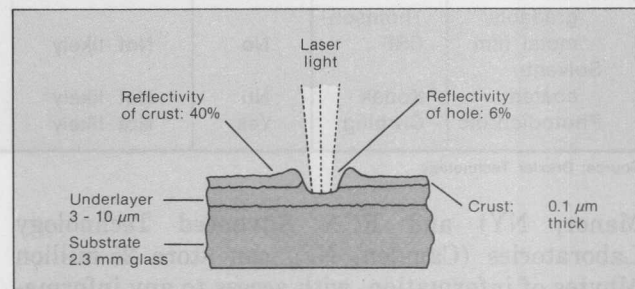
Kodak's medium, according to the Strategic report, uses a 130-nm-thick layer of organic dye/binder as its storage medium. The recorded spot does not extend through the organic coating. Instead, it forms a flat-bottomed depression that is light-absorbing at one wavelength and transparent at another. According to the report, the thickness and melting characteristics of the dye/binder can be varied to maximize absorption and reflection. To write a bit of data requires a low-power pulse of between 10 and 20 mW for 25 ns. Thus, this medium is well-suited for high-speed data storage.

IBM's dye/binder material is hydroxy squarylium (OHSq). When a spot is burned on the media, there is a change in reflectivity that can be detected as data, during the read operation. According to the study, IBM has found that the material has strong optical absorption at wavelengths of 800 nm and below, thus making it possible to operate in the infrared spectrum. It also has been found to have excellent thermal and optical stability. Its write and

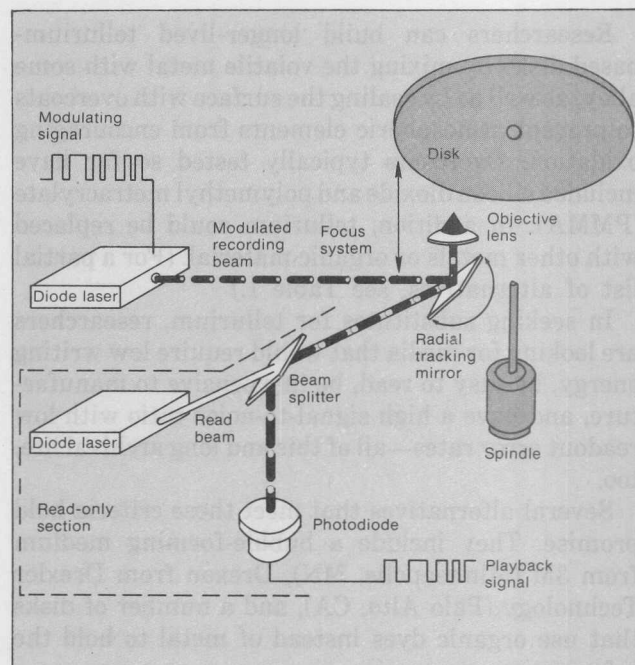
read characteristics are said to be comparable to those of tellurium, and it is relatively easy to manufacture.

Zeroing in on errors

Turning to yet another desirable characteristic being sought in an optical storage medium—improved error rate—most authorities agree that a corrected error rate of 10^{-12} is required before optical disks can hope to replace magnetic data storage on a wide scale. Typical error rates reported at present by most vendors in the field indicate a raw rate of 1 per 10^{-5} or 10^{-6} bits. The rate for the Drexler Technology disk is said to be 10^{-7} , an order of



3. Drexler Technology's Drexon media consists of an upper crust containing silver grains of filamentary and spherical shapes suspended in a colloidal binder; the former heats easily, the latter provides high reflectivity. To write, a laser burns away the binder, leaving a spot of low reflectivity, which can be detected by a read laser.



4. Vernier positioning of a read/write head over the disk in this Storage Technology Corp. simplified block diagram of a storage system is accomplished with a radial tracking mirror, while a focus system compensates for undulations of the disk surface that can cause the light beam to be out of focus.

magnitude better than other metal-based media.

With magnetic disks, the platter is error-corrected before it ever reaches the customer. Skips are inserted in the drive to avoid those spots on the disk where magnetic properties are insufficient to retain data.

According to Juan Rodriguez, vice president for research and technology, Storage Technology Corp. (Louisville, CO), error-detection and recovery techniques will become integral parts of optical disks used for data storage. In effect, these techniques will be used to eliminate errors in real time.

Getting at the data

Another element of the optical disk drive that demands improvement is the mechanism for locating, reading and writing information on the disk medium. Three elements perform this function: the heads used to write and read information, the mechanical positioner, and the optics that ensure that the read-write beam is focused properly.

While the mechanism to move the read/write element over the optical storage medium is similar to that of a magnetic disk storage system, significant enhancement of accuracy is needed in an optical system. Magnetic drives store information in circular tracks on the disk at a density below 1000. Optical systems would begin with a density somewhere around 4000 to 5000 tracks/in. That calls for a much-improved positioning mechanism to resolve such densely packed track spacing.

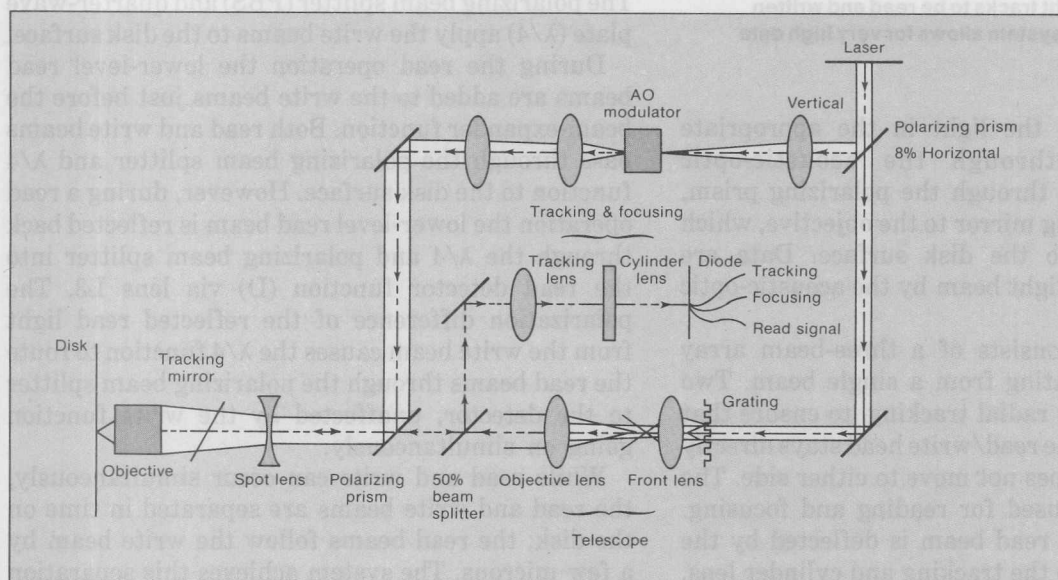
In a typical magnetic disk drive, a voice coil moves an actuator with read/write heads horizontally across the disk surface, perpendicular to the axis of

rotation of the disk. A closed-loop servo ensures accurate positioning of the heads over the appropriate track. In an optical disk system, such a servo loop would provide coarse positioning of the heads. Thereafter, another servo positioner would be needed to control vernier location of a specific track within a group.

A simplified diagram of a vernier positioning system by Storage Technology System is shown in Fig. 4. The galvanometer is a lightweight motor that alters the angle of the radial tracking mirror. If the mirror angle is bent, the beam position can be moved very accurately on the disk surface to locate the appropriate track. Moreover, the actual positioning can occur very rapidly—five to 10 times faster than the mechanical actuator.

Other more esoteric solutions might serve this application as well. Frank Sardello, vice president of the Recording Technology Center at Memorex (Santa Clara, CA), describes one as a method demonstrated by Zenith some 10 years ago. It consists of a lens that could deflect a beam of light without mechanical motion. To effect the deflection, the crystal structure of the lens is altered electrically. This in turn changes the index of refraction. Ten years ago there were no takers for this novelty; however, with the advent of optical storage systems, such a beam-steering device might find new applications.

Another servo within the Storage Technology head-positioning mechanism controls focusing of the laser beam used for either read or write operation. This is shown in Fig. 4 as the focus system. A beam of light directed at the disk surface is reflected back



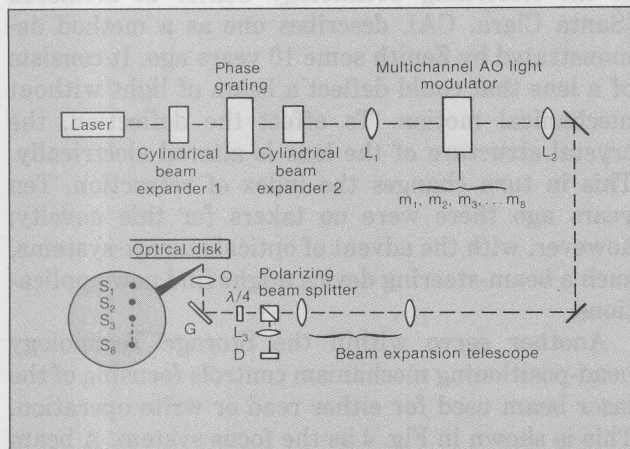
5. In the Philips Labs' optical system, the write beam passes through the acousto-optic modulator where data is added to the beam. The read beam passes through the grating, is split into three beams, which are reflected from the disk surface, and is deflected by the beam splitter to the diode where data is extracted.

Memory Technology: Optical disks

into the servo system, indicating any surface undulations on the disk. Such undulations are critical, since the focus of the read/write beam must be within a micron of vertical space. Using the reflected focusing beam, a voice coil moves the objective lens directing the read/write light onto the disk surface, up or down, to focus the beam very precisely on the disk surface.

Another optical positioning method under development (Fig. 5) is part of an experimental digital optical recorder by Philips Laboratories (Briarcliff, NY).

According to Philips' George C. Kenney, group director for electronic and optic systems, light from one of two lasers is directed in either of two directions, depending on whether the light is used for a read or write operation. Light from the lasers is polarized in one direction for read and in another for write. The polarizing prism at the laser and at



6. The RCA Advanced Technology Labs optical system shown above allows eight tracks to be read and written simultaneously. Such a system allows for very high data transfer rates.

the objective direct the light in the appropriate direction. Light through the acoustic-optic modulator is routed through the polarizing prism, spot lens and tracking mirror to the objective, which directs the beam to the disk surface. Data are modulated onto the light beam by the acoustic-optic modulator.

The read beam consists of a three-beam array produced by the grating from a single beam. Two of these are used for radial tracking, to ensure that as the disk rotates, the read/write head stays directly over the track and does not move to either side. The remaining beam is used for reading and focusing. During focusing the read beam is deflected by the 50% beam splitter to the tracking and cylinder lens. If the disk surface undulates upward or downward, the beam in the cylinder lens becomes elliptical in one direction or the other.

This anomaly is detected by a photo diode, and a correction signal causes the objective to be moved closer or farther from the disk surface to compensate. Read data are extracted from the read beam by electronics beyond the diode. To effect read-after-write operation, the record and read beam are angularly separated along the track, with a 10-to-20 bit delay between the two.

The performance of this system of optics is a minimum 5 Mbits/s transfer rate using a single beam and writing one beam at a time.

Improved optics boost data rate

Another design intended for faster data-transfer rates achieves a speed of 400 Mbits/s. This system was developed by RCA Advanced Technology Laboratories (Camden, NJ). According to RCA's G.J. Ammon, unit manager in the Applied Physics Lab, the increased speed is achieved through the optics of the system (Fig. 6).

In this scheme, the laser write beam passes through a cylindrical beam expander (CBX₁) and a phase grating function (PG). The light is split by the phase grating into eight distinct beams. The beams move to another cylindrical beam expander and then to a multichannel acousto-optic light modulator (MCAOLM), which is a single-crystal acousto-optic cell with eight closely spaced transducers, which individually modulate the eight input beams. Each modulates at 50 Mbits/s, thus eight channels with a total 400 Mbit/s data rate.

The remainder of the RCA optical system is similar to a single-beam system. The beam expander provides the magnification to fill the objective lens. The polarizing beam splitter (PBS) and quarter-wave plate ($\lambda/4$) apply the write beams to the disk surface.

During the read operation the lower-level read beams are added to the write beams just before the beam-expander function. Both read and write beams pass through the polarizing beam splitter and $\lambda/4$ function to the disk surface. However, during a read operation the lower-level read beam is reflected back through the $\lambda/4$ and polarizing beam splitter into the read detector function (D) via lens L3. The polarization difference of the reflected read light from the write beam causes the $\lambda/4$ function to route the read beams through the polarizing beam splitter to the detector, unaffected by the write function going on simultaneously.

While read and write can occur simultaneously, the read and write beams are separated in time on the disk; the read beams follow the write beam by a few microns. The system achieves this separation by angling the read beam slightly behind the write beam on the disk surface.

Providing the beam that writes on and reads from

the disk is the job of lasers. Up to now, gas lasers have done the job, the two most favored being the argon and HeNe. But that is beginning to change with the advent of semiconductor lasers, which can do the job better.

Lasers that read and write

Argon lasers can produce power levels over a watt, while HeNe come in between 20 and 50 mW. The wavelengths on these devices are very short—4880 and 6328 angstroms, respectively. The argon laser is typically used for writing and the HeNe for reading.

For writing, the high power and narrow wavelength of the argon laser can produce very small submicron dot sizes and very fast writing speeds. Thus the information can be packed very densely on the disk and at high data-transfer rates. The lower-powered HeNe laser offers lower cost and smaller size over the argon laser; hence it is used for reading typically.

But while gas lasers offer these advantages, they also have drawbacks. Argon lasers are big, some versions being six feet long. Because of their high power, argon lasers must also be cooled with water, and as might be expected, they're not cheap.

In addition, the argons operate continuously during a writing operation; the beam is always on. The laser tends to wear out more quickly than it would under intermittent operation. To write, the output beam is modulated, requiring external electronics and optics. Finally, there is a warm-up time of several minutes needed for the unit to stabilize after it is turned on.

Enter the semiconductor laser, which seems likely to do to gas-tube lasers what the semiconductor transistor did to the vacuum tube. Diode lasers are smaller, will cost much less and last longer than gas units, and they will not require external modulation electronics and optics.

Because of its small size, a diode laser can be mounted right on an optical disk actuator, much like the present setup in magnetic disk drives (Fig. 7). In effect, the read/write laser can be moved across the disk surface to perform its function. The cost will be less because, like any semiconductor product, the lasers can be mass-produced with conventional technology.

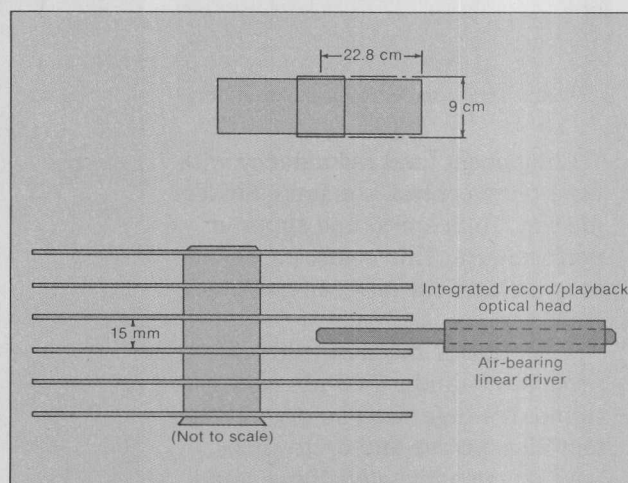
Diode lasers are expected to last longer, not only because they are semiconductors, but also because of the way they operate. Unlike gas units, diodes can be modulated by an input sign turning the laser on and off; hence the diode is not on continuously.

Still, there are potential problems with diode lasers that will have to be solved. They have low output power and longer wavelengths than gas

lasers, and they do not produce light in a highly directed beam, as do the gas lasers. The output power is typically under 20 mW, which affects data-transfer rates. With a 40-mW gas laser, a 60-Mbit/s transfer rate is possible, while a more realistic level for a diode laser would be below 20 Mbits/s. Using a faster transfer rate with lower-power lasers would result in spots that blurred together indistinguishably.

Finally, diode lasers would encounter difficulty in producing a highly directed beam. In most diode lasers the light is emitted in dispersed multimode fashion, rather than in a directed (single-mode) manner. One solution has been to use optics to focus the light into a beam at the output of the laser. However, more recently strides have been in producing one coherent beam of light from a diode.

To achieve this, a waveguide is fabricated into the



7. In the Philips' simplified actuator assembly shown above with semiconductor lasers, the read/write head becomes part of the actuator that slides across the disk surface much like a magnetic disk.

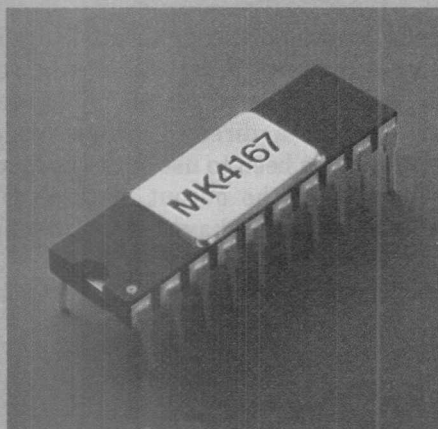
laser during its manufacture.

One version from Optical Information Systems (Elmsford, NY) uses a buried heterojunction large optical cavity structure to produce a laser capable of 20 mW of continuous output power, with a pulse power of 40 mW. RCA (Princeton, NJ) is also confident of having a diode laser capable of 40-mW pulse power. The laser it is developing uses a constricted junction double-heterojunction optical cavity to produce a very directional output beam of light.

According to Mike Ettenberg, head of the Optoelectronics Systems lab at RCA (Princeton, NJ), the RCA laser has undergone 10,000 hours of evaluation, and the company is confident that it will be able to manufacture it soon.

Another company said to have laser diodes capable of 20 to 25 mW output is Hitachi (Chicago, IL). □

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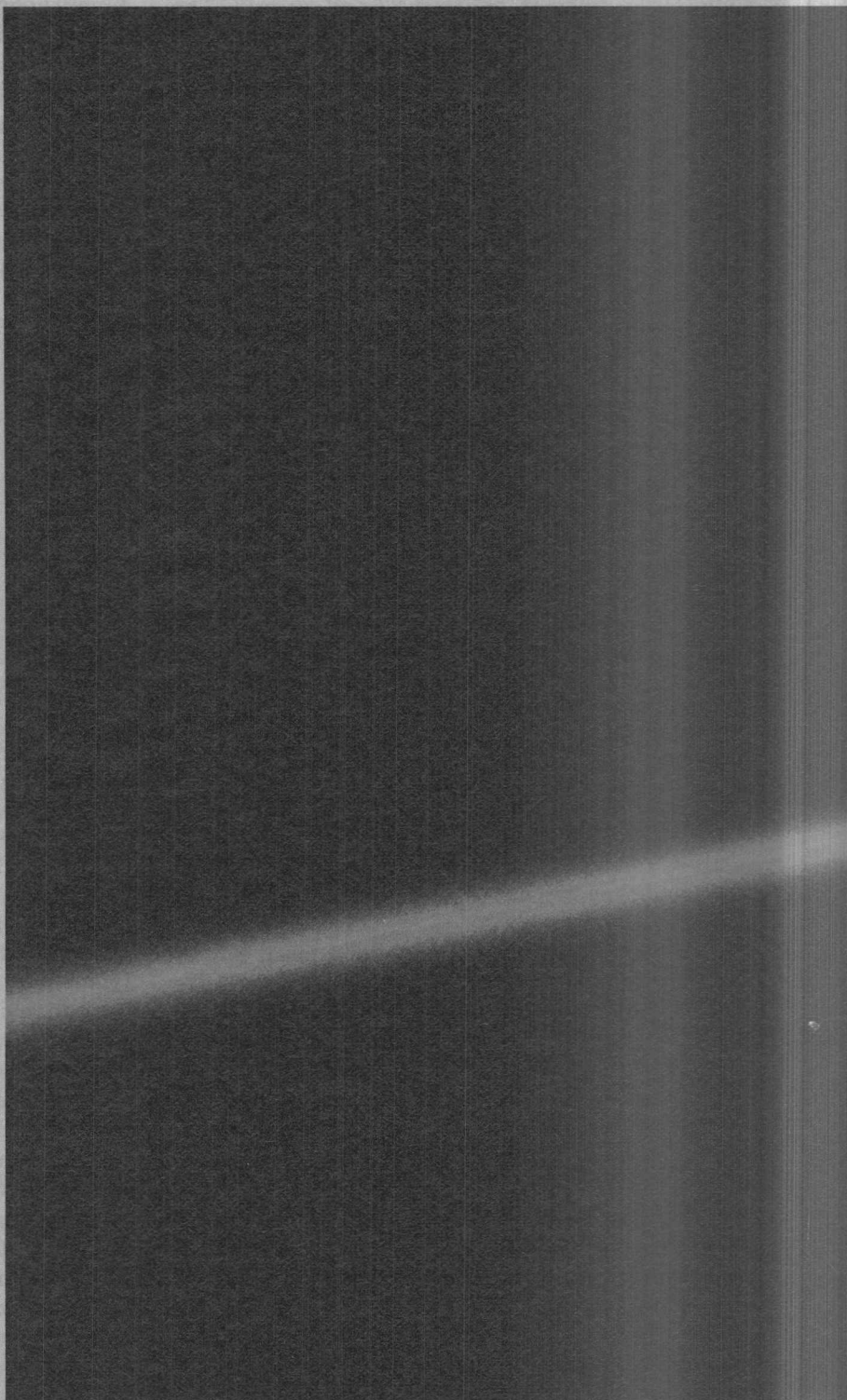
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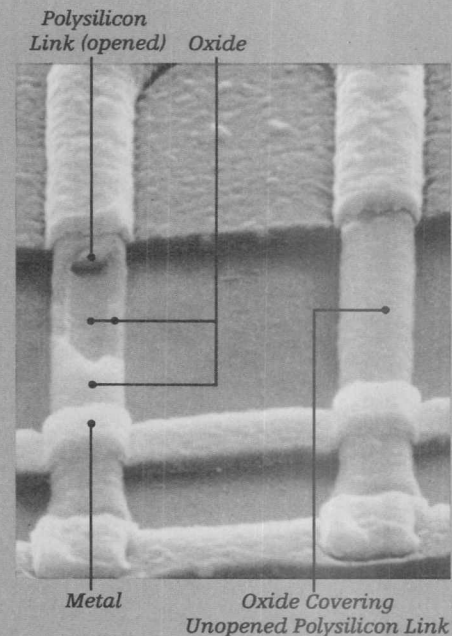


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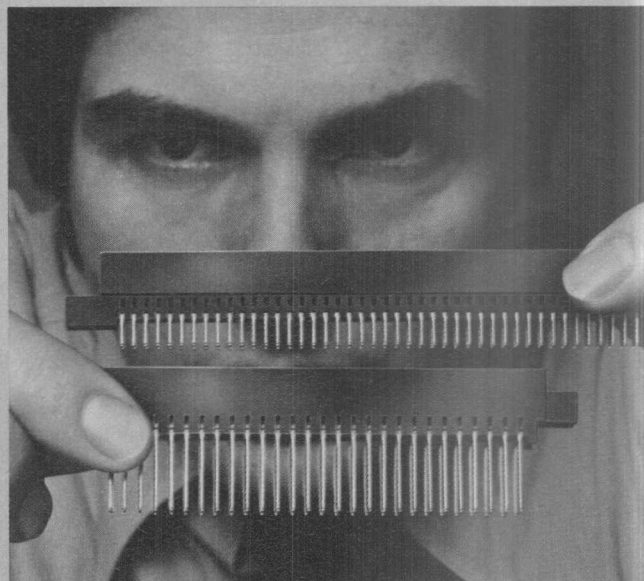
Scanning Electron Micrograph of a polysilicon link which has been opened to select a redundant column. The link was vaporized by a precision laser pulse.

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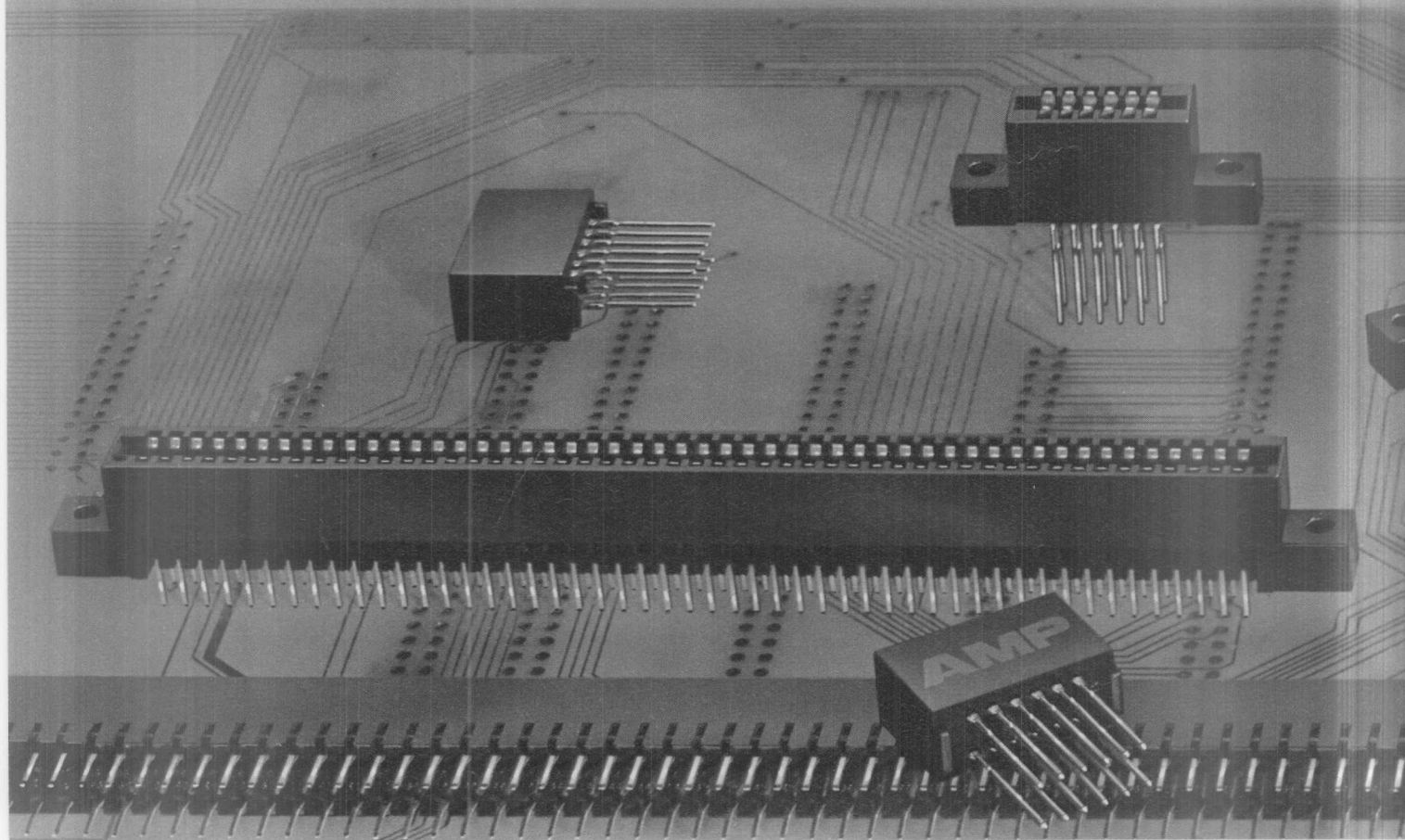
Another part is Accu-plate, the exclusive plating process that precisely plates different metals on the same contact—without waste. Nickel underplate, gold only where it's needed and tin lead on the legs for easy solderability.

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AMP Facts

Sizes and Dimensions: 6 to 50 positions on .100" centers (.200" row-to-row) and .125" centers (.250" row-to-row). Height—0.610". Card slot depth 0.295". Card extender version also available.

Current Rating: 3 amperes.

Resistance: 12 milliohms.

Voltage Capability: 1000 VAC at sea level

Operating Temperature: -55°C to +105°C.

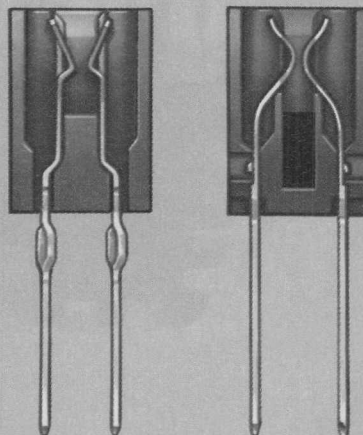
Insulation Resistance: 5000 megohms (minimum after humidity test).

Vibration Test: 10 to 500 cycles per second (10 G's peak).

Engagement Forces: 8.0 ounces typical for .062" board.

Humidity Test: 90-95% for 96 hours.

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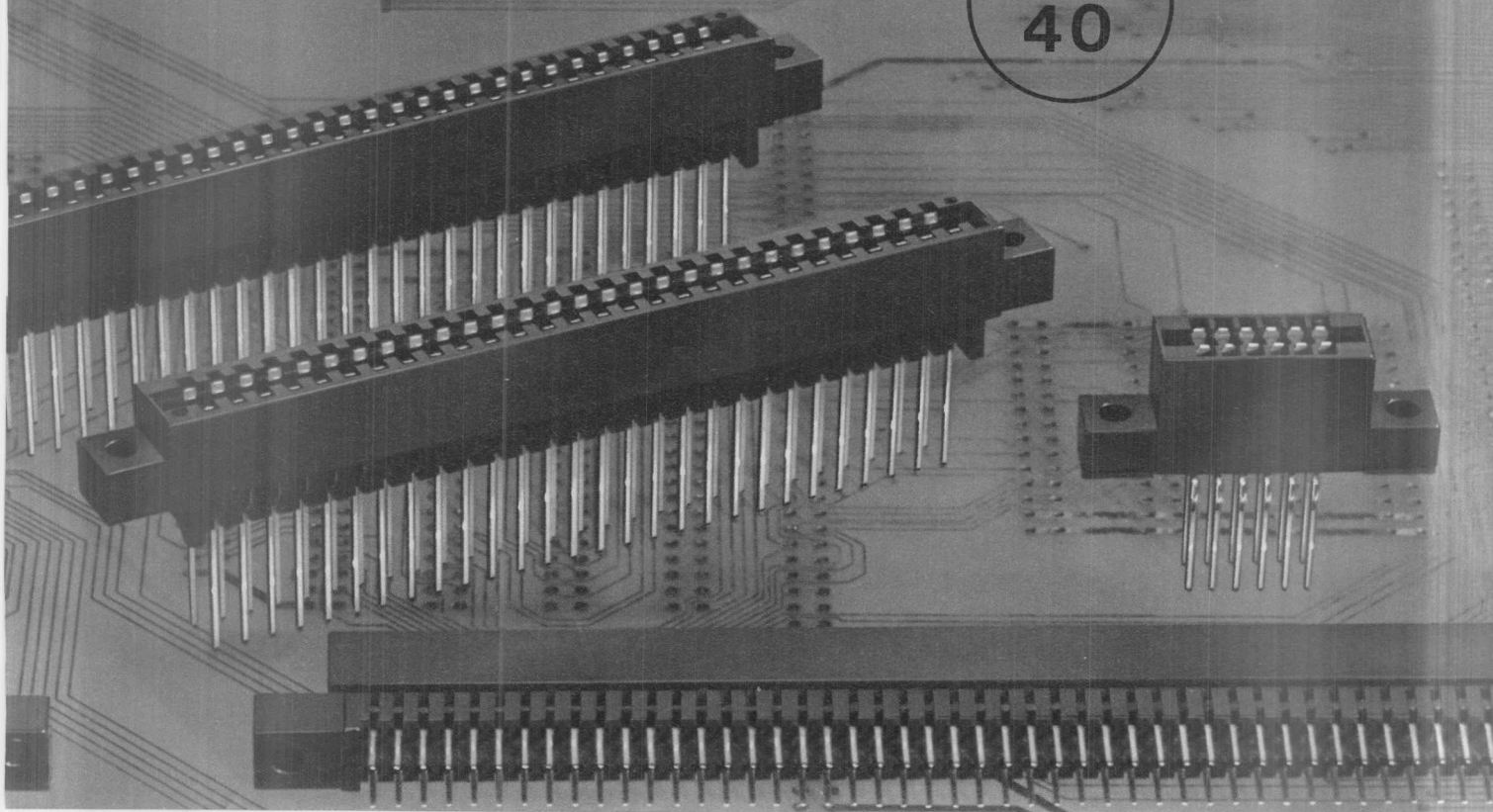
For a free sample, call the AMP Standard Edge Connector Information Desk at (717) 780-8400.

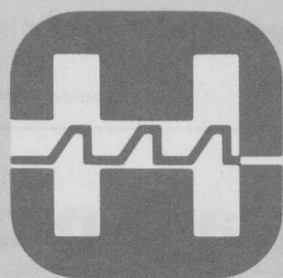
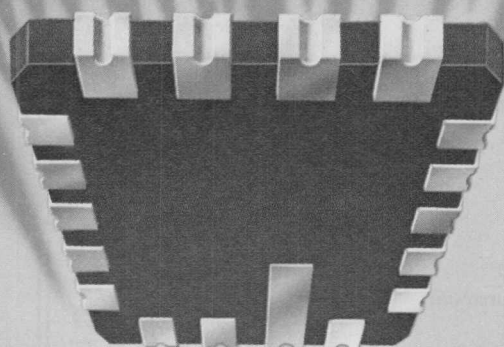
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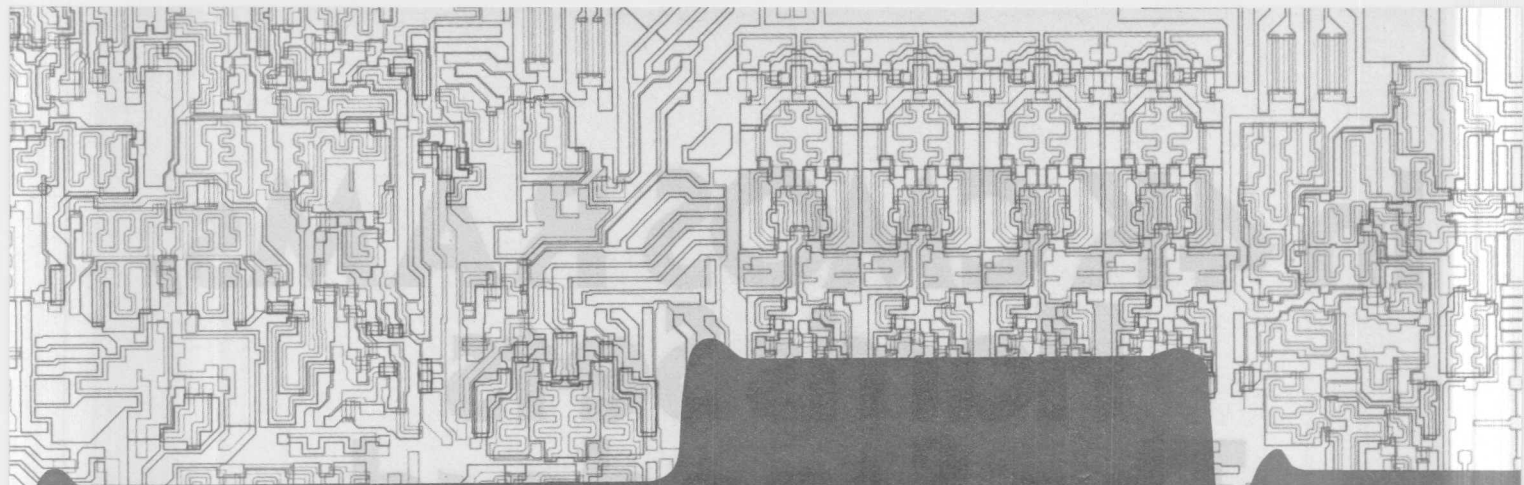
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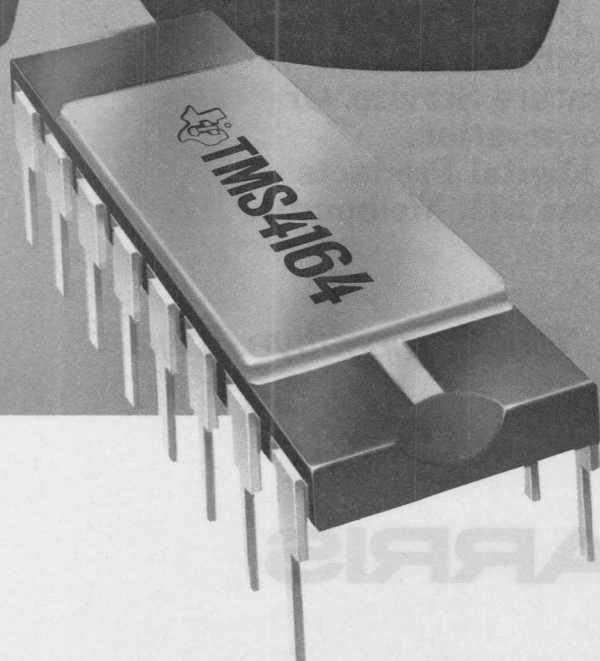
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40 mA

20 mA

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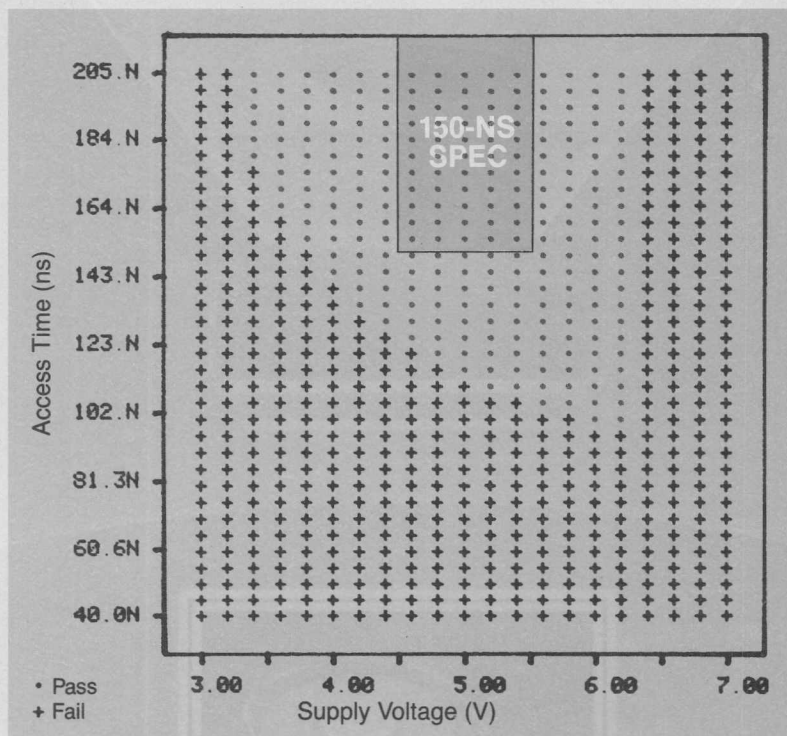
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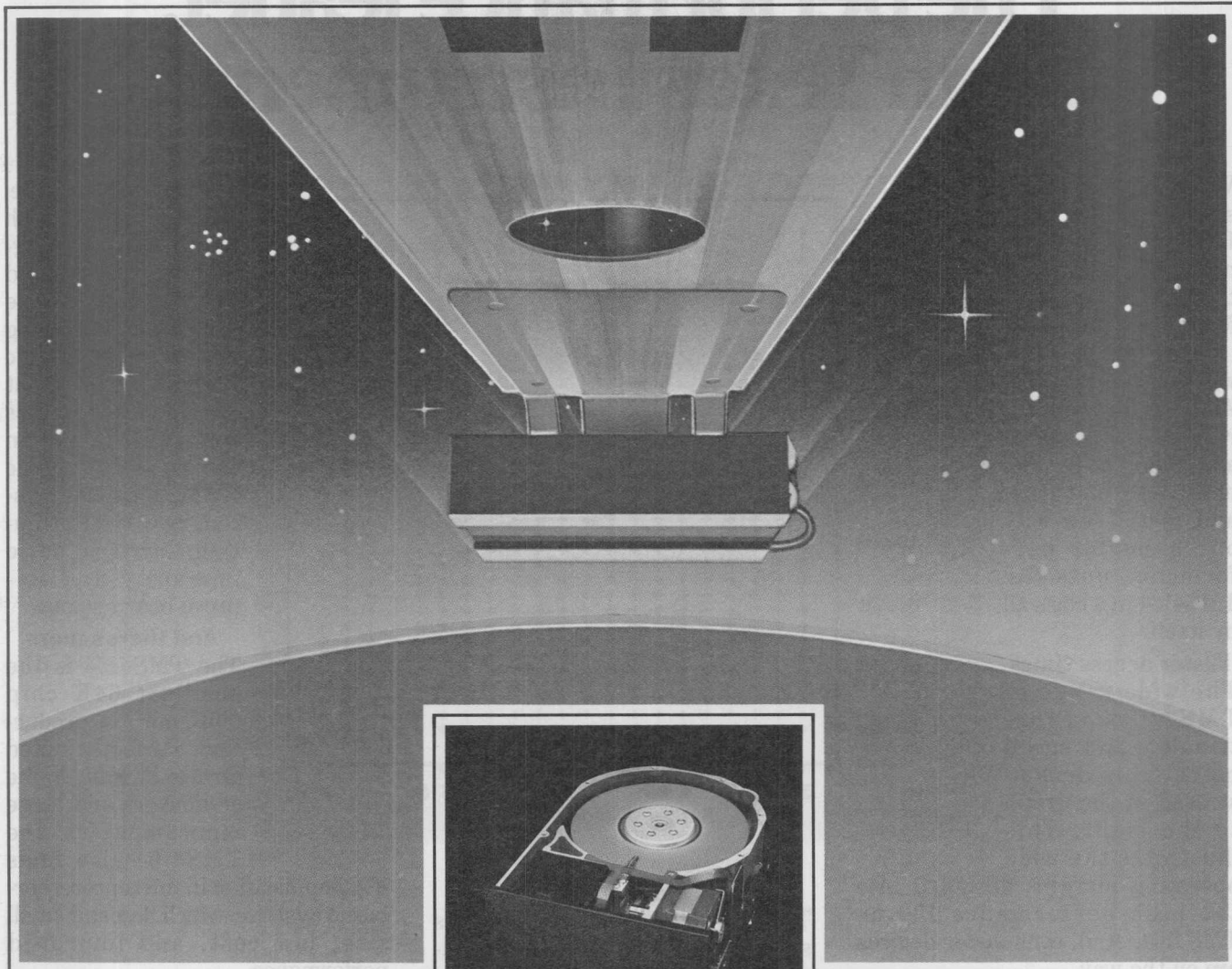
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CIRCLE 50

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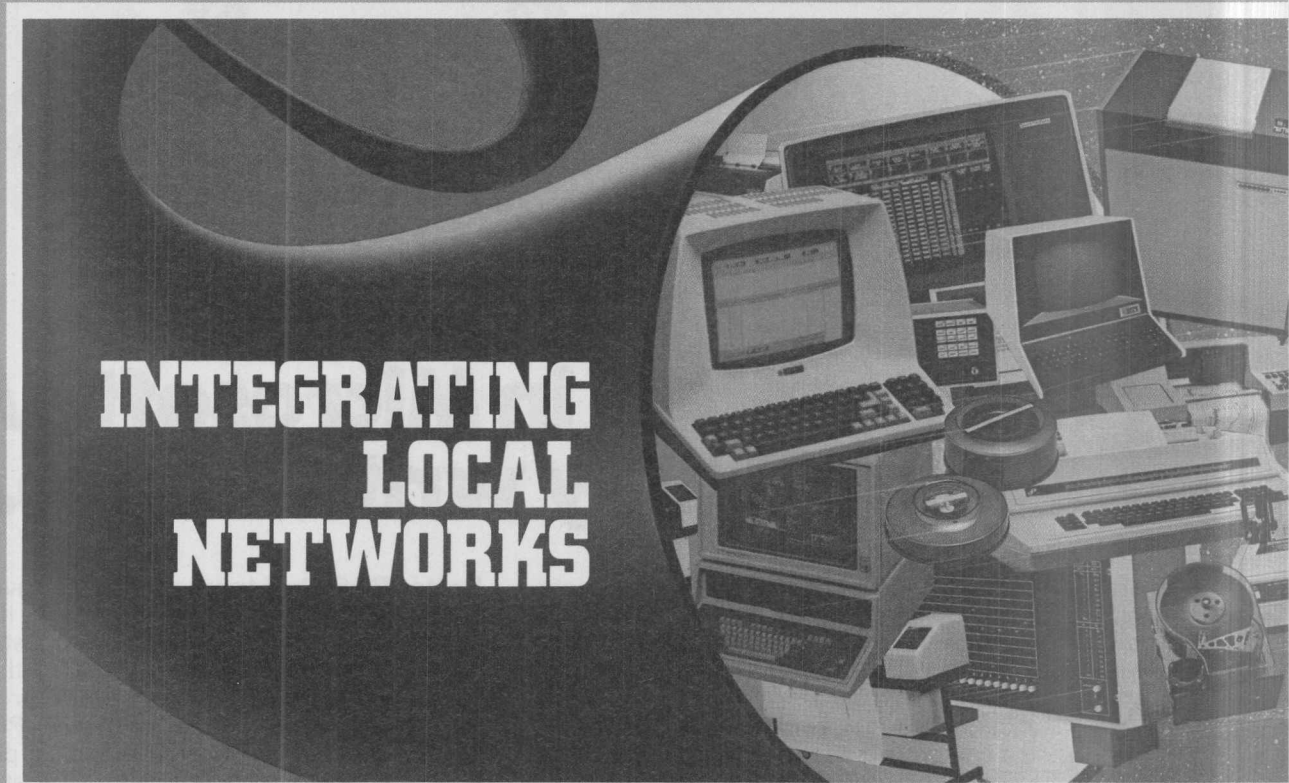
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SYSTEMS & SOFTWARE

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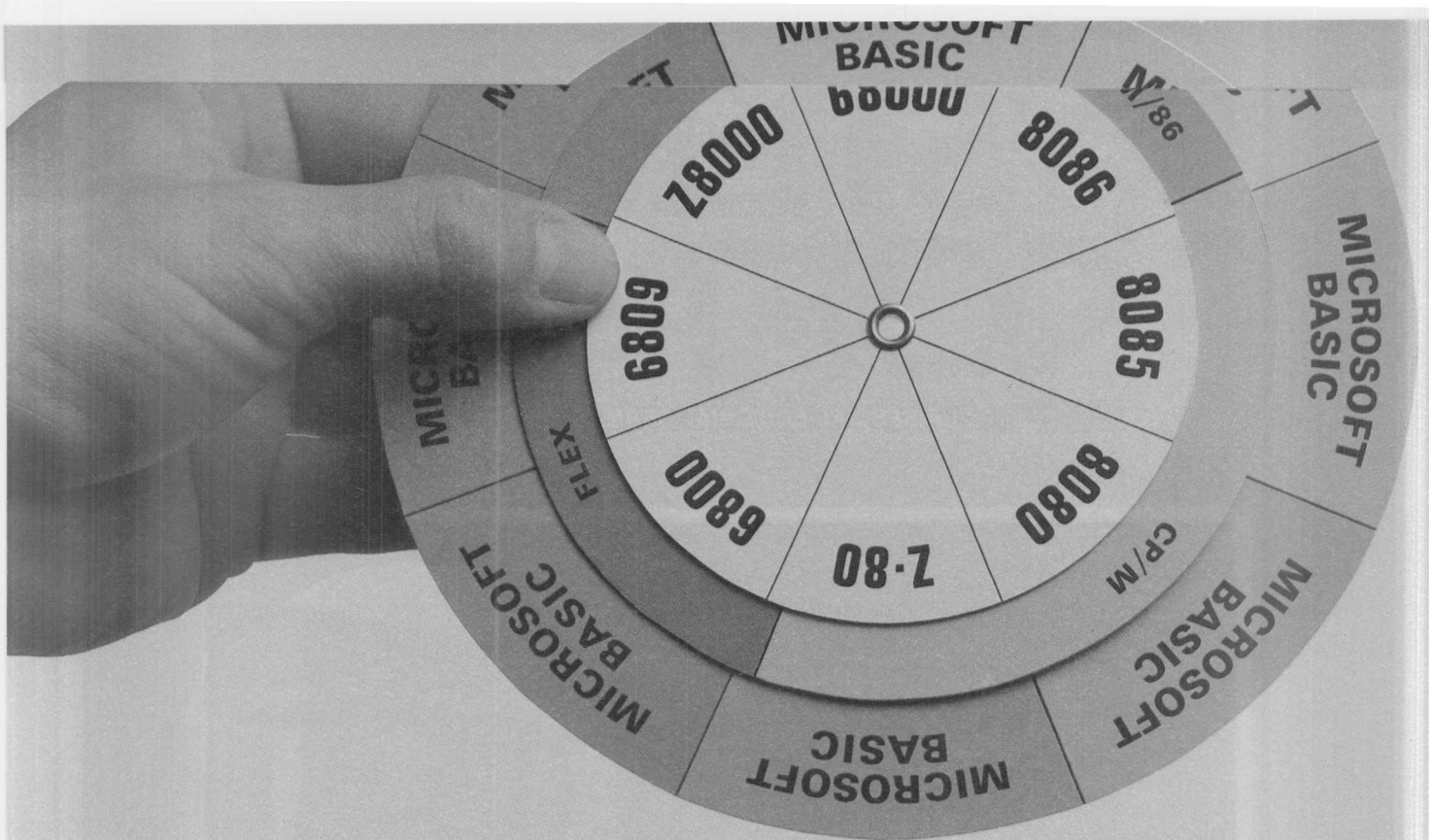
INTEGRATING LOCAL NETWORKS

The ins and outs of networking architectures

Assessing the standards controversy

What the trade-offs are in selecting hardware

How software manages the network



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Introducing a new editorial series for systems integrators

Today's systems integrators face not only a steadily quickening pace of technological improvements from the component level up to the system level, but also, thanks to VLSI technology, a narrowing gap between the two. Yesterday's subsystems have evolved into today's single-chip components. VLSI chips have rendered obsolete major portions of systems that once consumed year-long efforts in design, assembly, and testing.

VLSI is also the prime mover behind the proliferation of small computers carrying price tags within the reach of any manager in business or industry. Such computers are, in fact, becoming as indispensable a tool for managers as, say, the typewriter has been for the secretary, or the VOM for the service technician. Such rapid-fire hardware improvements mean little, however, without companion improvements in software, which has long been the stumbling block in designing efficient systems. But the availability of low-cost small computers for users who have little training in programming has brought renewed efforts in automatic software production. Thus, systems integrators must broaden their horizons to encompass VLSI-based microcomputer hardware. At the same time, they are finding a rich lode of software developments that can be transferred upward to larger systems.

Systems integrators are also feeling the impact of steadily improving storage-device performance at ever lower prices. The floppy disk, developed by IBM as a read-only microprogram memory, has become virtually a universal means of mass

storage for small computers and has opened the way for more reliable, higher-capacity mini and micro-Winchester-disk drives. Such shifts in the price-performance criteria have further complicated the dynamics of systems planning.

The growing interest in local-area networks is also placing new challenges before systems integrators. The concepts involved in data communications and distributed processing are hardly new, but now the systems integrator must respond to a growing customer demand for small-computer networks that allow many users access to system resources. Here, too, new approaches are required—specifically to meld architecture, software, and hardware into one efficient system.

Indeed, faced with changing tools, changing subsystems, and changing applications, today's systems integrators must change their basic approaches to systems design. Timeliness is becoming a critical element—a successful product must ride the crest of one technology well before a new wave can erode its underpinnings and capture the market.

ELECTRONIC DESIGN's Systems & Software series will present the authoritative, practical information today's systems integrators require as they prepare to tackle the problems raised by local networks, software automation, computer graphics, office automation, manufacturing, and scientific and engineering applications. Each installment in the Systems & Software series will present several articles examining principal topics from every angle. No other publication has focused its energies to such an extent on the critical issues facing the systems integrator.

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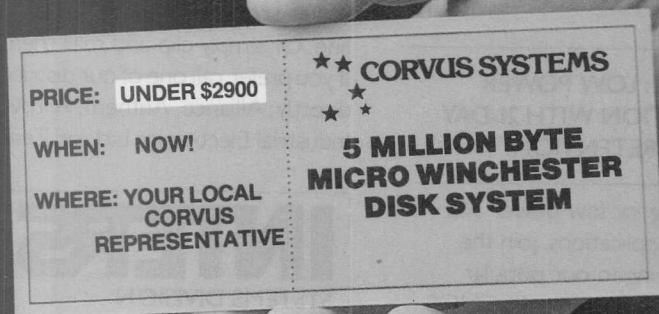
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Local networks mushroom to increase productivity

Local-area networks—high data-rate communications systems that interconnect multiple processors and shared peripheral devices—have been used for years in random applications in office buildings, plants, laboratories, and other small geographical areas. Over the past few years, however, this scattergun approach has been giving way to a concrete perspective. Economies offered by large-scale integrated circuits have spurred intense development of networks that will support office, factory, and laboratory-of-the-future concepts—specifically, an intelligent workstation on every desk, linked to such shared resources as data bases, printers, and telecommunications facilities.

The driving force behind this effort is the need for greater productivity in nonmanufacturing activities. According to Dataquest, Inc. (Menlo Park, CA), business organizations would have to install a trillion dollars' worth of new equipment by the year 2000—\$11-billion a year—to match industry's investment per worker in automation.

Leading-edge users of office-automation systems—mostly large corporations—plan to make their investments rapidly, but the needs of smaller organizations will remain unfilled for decades to come. By 1990, only a few percent of potential LAN applications will be filled (Strategic Business Services,

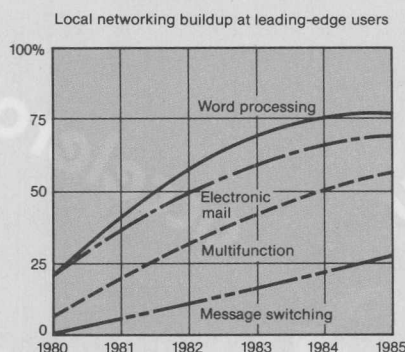
Inc., San Jose, CA).

LANs are being installed today as EDP systems with intraoffice extensions, using newly designed terminals that easily interface to a network, and as PBX systems with data sets. There are also a growing number of hybrid approaches: EDP-based networks with attached digital PBX systems, general-purpose microcomputer systems bundled with nets and software, and

simple disk-storage systems designed to serve a cluster of microcomputers.

There are no hard and fast standards for LANs yet; therefore, as in the microcomputer startup era a decade ago, the potential for innovative applications is enormous.

The future, then, belongs to the system integrator who can tailor hardware and software to his own customer's needs. The following series of articles aims at helping the systems integrator do just that, with discussions devoted to choosing an architecture; assessing the ongoing efforts to establish LAN standards; developing software, a process that is now the longest part of the learning curve; and selecting the hardware with careful cost evaluations to implement the scheme.



Potential LAN applications (millions of line terminations)

	1980	1985	1990
Office *	3.12	6.20	14.50
Operations *	1.40	2.60	6.00
Facilities †	0.13	0.25	0.50
Totals	4.65	9.05	21.00

Estimated attainable LAN installations (millions of line terminations)

	1980	1985	1990
PBX-based control	—	0.07	0.21
EDP-based control	—	0.05	0.14
Stand-alone LAN	—	0.03	0.10
Intelligent LAN terminals	—	0.02	0.25
Totals	NA ‡	0.17	0.70

* KSR/video, telephones, key systems/PABX, printers, microcomputers, minicomputers.

† Analog controllers, microcomputers, minicomputers.

‡ Not analyzed.

Source: Strategic Business Services Inc.



UDS technology

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The accelerating growth in modem technology at Universal Data Systems has now produced the Company's first 9600 bps unit on a super-compact OEM board. Occupying about 100 square inches of PCB space, this microprocessor LSI modem offers dramatic space savings for designers who wish to package data sets internally in microcomputers, minicomputers or interactive terminals. The traditional UDS economy and reliability are inherent in the new 9600 bps modem.

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CIRCLE 104

Created by Dayner/Hall, Inc., Winter Park, Florida

Network architectures offer performance variety

A broad range of LAN architectures have been developed for many applications; choosing one requires study of topology, protocol, and media.

Most LANs have one of five basic topologies: star, loop, ring, common-bus, and broadband-bus systems. The topology generally goes hand-in-hand with the control architecture, which may be centralized, as in a PBX or time-shared computer or in an IBM business loop. Or the architecture may be partly decentralized, as in a new PBX with microprocessor-based subsystems on each floor of an office building and some newer loops. It may be fully distributed in rings and buses, but a measure of central control may be added to handle priority traffic and a variety of services.

Distributed control and protocols for implementing buses are coming to the fore because they are more compatible with LSI technology. Microprocessors and new interface chips placed in each node avoid the need for a large, complex central controller and allow a network to expand at incremental costs per node. Also, they help assure graceful degradation of the network instead of catastrophic failure.

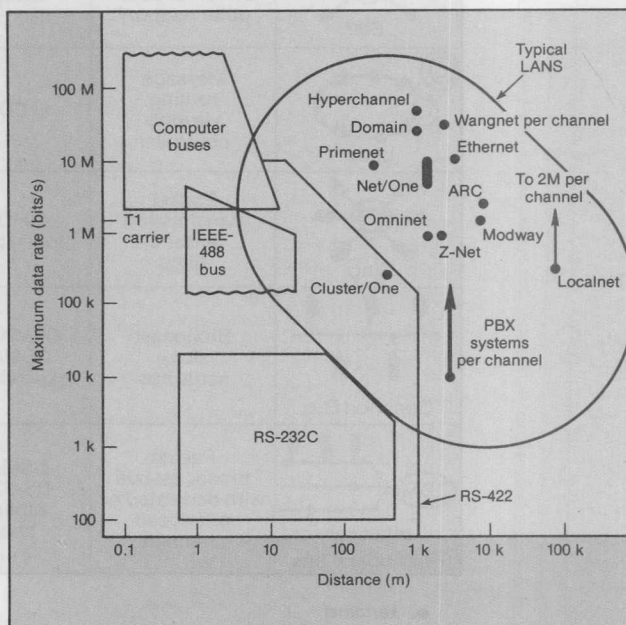
It is now practical to install a miniature counterpart of a nationwide packet-switching network within an office. Equipment manufacturers are beginning to design into their products LSI counterparts of packet-switching minicomputer nodes. The chips shrink the interfaces from several boards to a single board, so that new networks will be competitive with traditional point-to-point links. Moreover, the local data rates go very high—megabits per second instead of kilobits.

Eventually the popularity of particular chip sets may lead to a few standard LAN designs for high-volume applications. For the moment, there is what one vendor calls "almost total confusion" in the marketplace about which LANs are best for which applications. It is not possible today to compare LANs on the basis of a few specifications, such as transmis-

sion rate and distance—the plots prove only that LANs have a broad range of applications (Fig. 1).

Starting at the top of the per-channel performance range, one can pick from networks like these:

- HYPERchannel, for connecting mainframes, large minicomputers and memories at computer centers (Network Systems Corp., Minneapolis, MN).
- WangNet, an office-oriented multichannel system for data, voice, and video communications (Wang Laboratories, Inc., Lowell, MA).
- Ethernet, an office-oriented system for data and—in the future—voice (Xerox, Digital Equipment Corp., and Intel—Fig. 2).
- Domain, an expandable minicomputer-based network (Apollo Computer Inc., North Billerica, MA).
- PrimerNet, bundled with proprietary computer systems (Prime Computer Inc., Framingham, MA).
- Net/One (Fig. 3), a general-purpose system for interconnecting normally incompatible equipment (Ungermann-Bass Inc., Santa Clara, CA).



1. Local area networks (LANs) are filling the vacuum in the data-communications market between computer buses and the long-haul networks. Their data rates and transmission distances vary widely, because they are usually aimed at particular segments of the overall LAN market.

George Sideris, Contributing Editor

Systems & Software: LAN architectures

■ ARC, bundled with proprietary computer systems with office extensions and digital PBX (Datapoint Corp., San Antonio, TX).

■ Localnet, a multichannel, general-purpose, data network (Sytek Inc., Sunnyvale, CA).

■ Modway, a flexible-architecture system for industrial applications (Modcon Div. of Gould Inc., Andover, MA).

■ Z-Net, an office-oriented system for local data communications (Zilog Inc., Cupertino, CA).

■ Omninet (Fig. 4), a shared-disk system for personal computers (Corvus Systems Inc., San Jose, CA).

■ Cluster/One, a flexible-architecture system for personal computers (Nestar Inc., Palo Alto, CA).

■ Digital PBX systems, for voice and data communications (such as systems from Rolm Inc., Santa Clara, CA and Northern Telecom Inc., Minnetonka, MN).

Data rates are deceiving because they may have nothing to do with the system's traffic-carrying capacity and, hence, the number and variety of nodes on the network. Despite their relatively low data rates, for example, PBX systems can interconnect thousands of

users. So can seemingly slow multichannel systems.

To arrive at the cost/performance tradeoffs that make sense in any particular market area, LAN vendors must choose from several different options at each level of network design: architecture, protocol, and media (Tables 1 and 2).

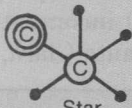
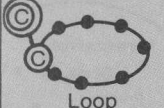
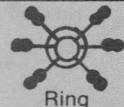
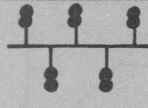
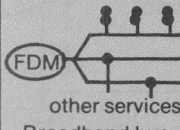
A look at topologies

Of the five basic LAN topologies, the star arrangements are most like those used in time-sharing of central computers. Today, data and text processors only occasionally share resources.

The newer loop configurations are often microcomputer systems, with any microcomputer capable of acting as the loop controller should the one designated as the loop master fail. All can operate as stand-alone systems until one requires access to a shared resource.

These systems are usually bundled with networking software. They are popular in departments of large corporations and in smaller businesses that prefer to create their own local data base rather than depend continuously on services offered by time-shared systems.

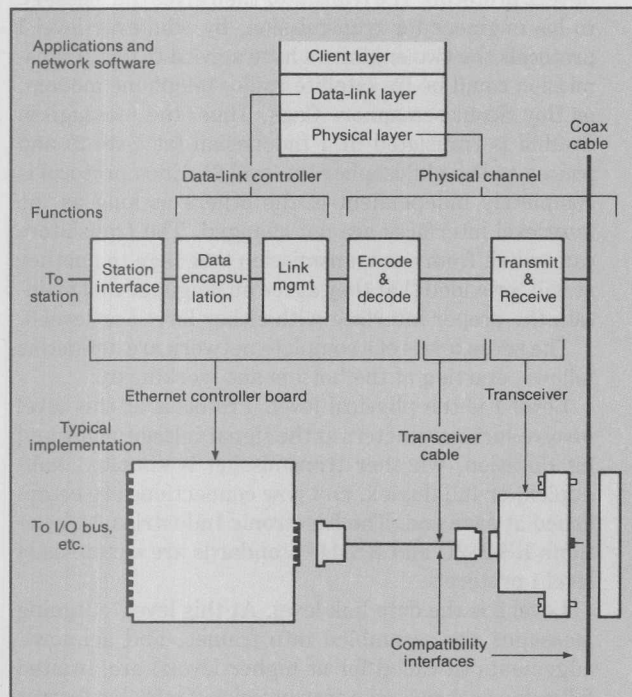
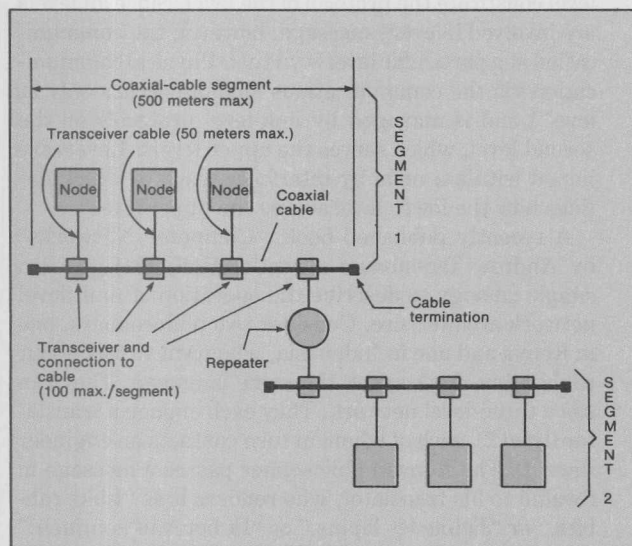
Table 1. Basic local-network architectures

Topology	Transmission mode	Typical protocols	Typical No. of nodes	Advantages	Typical systems
 Star	Point-to-point via channel switch or computer memory	RS-232C or computer	Tens	Well-known, large base of users	PABX, computer μ C clusters
 Loop	Message routing via loop controller	SDLC	Tens	Well-known, large base of users	IBM 3600/3700, μ C clusters
 Ring	Packet transmission around rings	HDLC (token passing)	Tens to hundreds per channel	Distributed control, no contention, popular for computer nets	Primenet, Domain, Omnilink μ C clusters
 Common Bus	Broadcast along serial bus	CSMA/CD or CSMA with acknowledgment	Tens to hundreds per segment	Distributed control, popular for office networks & computer nets	Ethernet, Net/One, Omninet, Z-Net μ C clusters
 other services Broadband bus	Packet broadcast bus with dedicated or prioritized channels	CSMA/CD RS-232C & others per channel	Two to hundreds per channel	Distributed control, large variety of users and services	Wangnet, Localnet M/A-COM

- Terminal
- Terminal with distributed controllers and/or multivendor interfaces
- Local controller
- Hierarchical network
- FDM Frequency division multiplex

The ring setups come in three basic classes: those that connect minicomputers into mainframe-class systems; those designed for distributed processing; and lower-performance rings for the office environment. In high-performance systems the cabling may be routed through a central point for network management and control. In office systems, control is usually fully distributed. Simple rings circulate packets of data and bus grants from node to node. The delay times usually limit the number of nodes to tens. However, this is not an inherent limitation.

Most common-bus systems allow any station to



2. Ethernet is a baseband, common-bus system (top). To use it, a system integrator adds a controller board to a work station (bottom).

broadcast a packet to all other stations. The addressee receives the packet, while all others reject it. Access to transmit on the bus is usually gained through a contention mechanism (some pass control or are prioritized).

Office-oriented systems, such as Ethernet and Z-Net, depend upon traffic being bursty at the link level to avoid a continuous state of contention. Ethernet has a high rate so it can grow to a thousand nodes, while Z-Net is designed as an inexpensive system for tens of small microcomputers.

To further boost traffic or node capacities, multi-channel systems divide broadband media into over a hundred channels. Localnet, for one, can handle up to 256 nodes on each of 120 channels. This allows the number of contenders per channel to be kept in balance by an increase in channels—an expansion in frequency rather than length.

Wangnet is a broadband system designed to integrate a wide range of data communications (from RS-232-C to contention bus and Wang proprietary), with the ability to provide voice and video services on the same cable. It also expands on a per-channel basis.

Most new LANs provide some means of interfacing existing computer hardware and software systems with the local network. It has been estimated that some 75 percent of users will want to preserve existing investments in data-communications facilities for at least a decade. So LANs come with user-transparent interface units, gateways to other nets, conventional communications ports or some combination of these interfaces.

The protocols

Some LANs use such protocols as RS-232C, HDLC (international high-level data link control) and SDLC (IBM's synchronous data link control). Some are based on the Multibus, IEEE-488 bus and other standard bus structures. However, new protocols—both "official" and de facto—are coming into use with the newer

Table 2. Media for local networks

Cable	Typical aggregate data rate	Typical number of nodes	Typical Applications
Shielded twisted pair	1 Mbit/s	Tens	μ C cluster
Baseband coaxial cable	10 Mbits/s	Tens to hundreds	Office equipment
Broadband coaxial cable	300 Mbits/s	To hundreds per channel	Office, computer center
Fiber-optic	50 Mbits/s	Two	Trunk, Hi-rel link

ring and bus topologies to support distributed-control approaches.

On contention buses or on contention channels of broadband buses, a node that wants to transmit listens to see if the media is free: carrier sense multiple access (CSMA) with acknowledgement of delivery, or CSMA/CD (CSMA with collision detection for auto-

matic restart of CSMA after a random delay). Ring systems either pass logical bus grants from node to node (token passing) or use time slots. All are forms of time-division multiplexing.

In the U.S. an IEEE committee is developing standards for CSMA/CD and token passing. However, the only de facto standard, the Ethernet CSMA/CD, var-

Seven-level architecture formalizes network protocols

In computer networks, just as in building, architecture is a concept that forces itself upon a practitioner. You can build a house without retaining a professional architect. However, you might find that it's not a very comfortable house. If you build many houses, one after the other, you want to make them similar but not identical, without encountering major construction problems with each new version. Likewise, in large computer networks and in local-area networks, a professionally constructed architecture is a must to achieve satisfactory operation and application flexibility.

For computer networks, the International Standards Organization has proposed a seven-level architecture called the Reference Model of Open Systems Interconnection—the palindromic acronym ISO-OSI (see Fig.).

Often, the architectural levels were not recognized as such in early networks, but they did exist in some form. Even in newer networks, the architectural levels may not look the same as in the ISO-OSI model, which is a set of guidelines, not a well-defined standard. This is particularly true of local nets, which might even separate the lowest levels and lump all the higher levels together.

Eventually, as the use of networks expands, particularly at the local level, the need to standardize at all seven levels will arise. At present, no such seven-level standardization for LANs exists. However, the Institute of Electrical and Electronic Engineers has a draft standard at levels 1 and 2, the U.S. Department of Defense has standardized higher level protocols, and the National Bureau of Standards is also working at the higher levels.

Some network vendors recognize the existence of all seven ISO-OSI levels in their systems, and implement each level in a way that seems to serve their applications adequately. Proprietary versions become a standard. Hewlett-Packard's HP-IB was slightly modified, for example, to become the IEEE-488 general-purpose interface bus (GPIB). Originally, the GPIB interconnected electronic instrumentation systems. Now, 488 is often used in local networks that contain no instruments (in the usual sense) at all—it is one of the popular architectures for local-area networks, in effect.

On each level of the ISO-OSI reference model, a given

node in a network communicates with another node; all communication is supposed to remain at a particular level at all times. Rules and conventions used at this level constitute the protocol of the level. Since all levels are involved in every message, however, the communication at a particular level is virtual. Physical communication via the communications medium occurs only at level 1 and is managed by link-level protocols on the second level, which serves the upper levels. Levels are joined within a node by interfaces, each of which defines how the lower level serves the upper level.

A recently published book, "Computer Networks" by Andrew Tanenbaum (Prentice-Hall, 1981), uses a simple analogy to describe the operation of multilevel network architecture. Consider two philosophers, one in Kenya and one in Indonesia, who want to talk about rabbits but don't speak the same language. They can use a three-level network. They each engage a translator (level 2), each of whom in turn contacts an engineer (level 1). The Kenyan philosopher passes a message in Swahili to his translator, who renders it as "I like rabbits," or "J'aime les lapins," or "Ik hou van konijnen," depending on the common language of the translators (level 2 protocol). The translator then gives the message to his engineer for transmission, by whatever level 1 protocols the two engineers have agreed to use. Transmission could be by satellite radio, telephone modem, or Boy Scout semaphore flags. Thus, the message in Swahili is translated into Indonesian (at level 2) and passed to the philosopher (at level 3). Each protocol is completely independent of the others as long as the interlevel interfaces are not changed. The translators can switch from one transmission language to another at will, provided that they agree on language and maintain the proper interface with either level 1 or level 3.

The seven levels of a complete network are defined as follows, starting at the bottom and working up:

Level 1 is the physical level. Protocols at this level involve such parameters as the signal voltage swing and bit duration, whether transmission is simplex, half-duplex, or full duplex, and how connections are established at each end. The Electronic Industries Association's RS-232C and RS-449 standards are examples of level 1 protocols.

Level 2 is the data link level. At this level, outgoing messages are assembled into frames, and acknowledgements (if called for at higher levels) are awaited following each message transmission. Outgoing frames include a destination address at the link level, and, if the higher levels require it, a source address as well—plus a

ies considerably from the IEEE draft.

CSMA/CD, because it is a contention protocol, will generally be used in applications where processors on a network use only shared resources or engage in distributed processing. This doesn't rule out prioritizing, as evidenced by HYPERchannel. Since the latter is designed to interface mainframes in heavy traffic

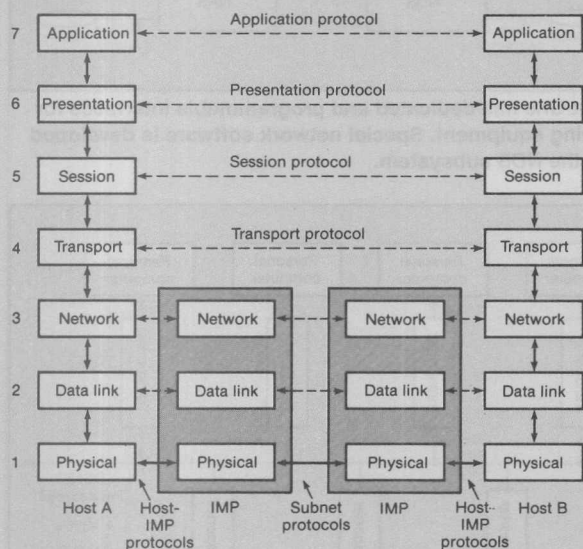
applications, it reverts to a priority mode after each transmission is completed. Token passing is used on some buses to guarantee access.

Also, token-passing rings are not necessarily slow and small. The Domain system has a data rate of 12 Mbits/s, expands to hundreds of nodes and could theoretically have billions of nodes. Token passing may be

trailer containing an error-detecting or error-correcting code. The data portion of the frame is whatever comes down to this level from level 3, without reference to its significance. Correct operation at this level assures reliable transmission of each message.

ISO HDLC (high-level data link control) and IBM SDLC (synchronous data link control) are examples of level 2 protocols; HDLC is incorporated into X.25 (CCITT standard generally used for data-packet communications) at this level. In some local nets, only error detection occurs at level 2 and correction is left to higher levels.

Level 3 is the network level. At this level, outgoing messages are divided into packets. Incoming packets are assembled into messages for the higher levels, and routing of outgoing packets is determined. A packet header defines the destination of the packet and indi-



cates the order of transmission. (The packets are not necessarily received in the same order in which they were sent when a packet network is used.) The header usually includes a source address. Level 2 constructs the frame containing the packet's data and header.

These first three levels are also involved when messages pass through intervening nodes en route. One well-known implementation is the interface message processors (IMPs) of the Arpanet, and another is the X.25 protocols. At level 2, X.25 calls for HDLC—the CCITT version of IBM's SDLC. The IMP concept has

spread from the Arpanet to other networks (notably GTE Telenet).

Level 4 is the transport level. This may be the busiest of all the architectural levels. Its protocol establishes network connections for a given transmission—for example, whether several parallel paths will be required for high throughput, whether several paths can be multiplexed onto a single connection to reduce the cost of transmission, or whether the transmission should be broadcast. This is the lowest level of strictly end-to-end communication, where the involvement or even the existence of intervening nodes is ignored.

Level 5 is the session level, at which the user establishes the system-to-system connection. It controls logging on and off, user identification and billing, and session management. For example, in a data base management system, a failure of a transmitting node during a transaction would be calamitous, because it would leave the data base in an inconsistent state. Level 5 organizes message transmissions in such a way as to minimize the probability of such a mishap—perhaps by buffering the user's inputs and sending them all in a group, more quickly than they could be under control of a higher level. Level 5 is not present in the Arpanet, and is rather restricted in IBM's System Network Architecture (SNA), in which levels 3, 4, and 5 are defined somewhat differently than in the ISO-OSI model.

Level 6 is the presentation level. It controls functions that the user requests often, and that therefore warrant general treatment. Such functions include library routines, encryption, and code conversion.

Level 7, the topmost level, is the application level, the one seen by individual users. At this level network transparency is maintained, hiding the physical distribution of resources from the human user, partitioning a problem among several machines in distributed-processing applications, and providing access to distributed data bases that seem, to the user, to be concentrated in his CRT terminal. In SNA, level 7 is represented by access methods, such as VTAM and TCAM. Levels 6 and 7 are combined in Digital Equipment Corp.'s DECnet.

These seven levels formalize the functions required at each level. By adhering to such a network design plan, a local-area network designer can ensure that all the required functions are performed. At the same time, the designer can simplify any future changes that may be needed, and help assure compatibility at the higher levels with other networks—local or long-haul.

Wallace B. Riley

Systems & Software: LAN architectures

the future standard of the plug-compatible computer industry—it is being backed for standardization by IBM and other mainframe computer manufacturers because of its architectural flexibility, as well as its easier compatibility with existing computer network architectures.

Media may dictate cost

None of the topology-control-protocol combinations preclude other combinations. Likewise none dictate the choice of media. In fact, it is often the other way around, with the media choices representing the major tradeoff.

In some cases a medium such as telephone wire or AC power wiring is chosen to avoid rewiring costs. PBX-based systems are designed around the premise that it is most economical to use the same wiring system for voice and data.

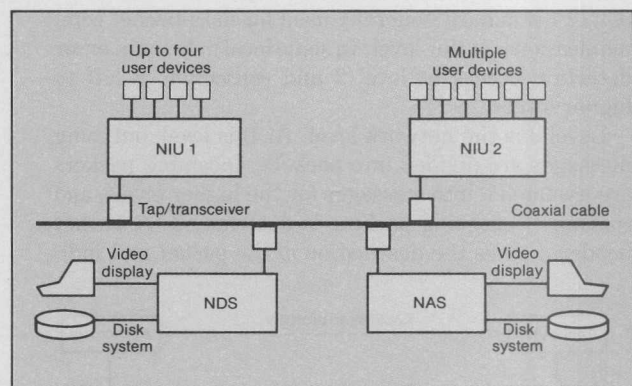
Media choice heavily influences the costs of interface units. Costly ECL logic assemblies are required to fully exploit the data rates achievable with base-band cable, while frequency-agile modems and other subsystems are needed to divide broadband cable into channels. Very-high-performance LSI devices will be used to reduce Ethernet interfaces to fit onto a single board.

Meanwhile many smaller networks have been installed to serve relatively limited numbers of microcomputers. These typically use telephone cabling with modem eliminators, twisted pair with conventional protocols or coaxial cable at a fraction of its

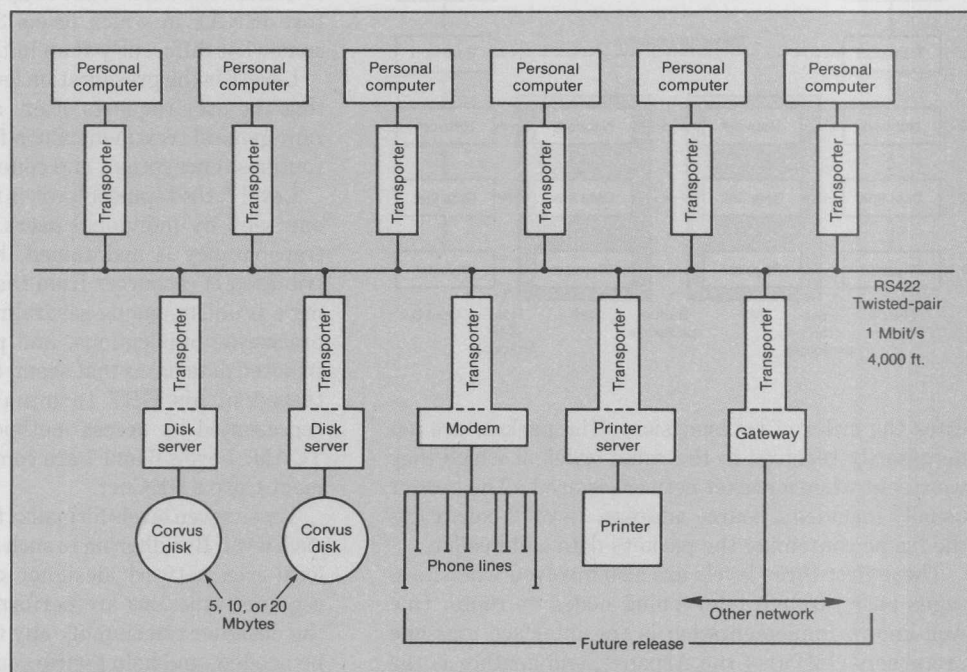
traffic capacity to reduce interface costs. In general, these are star or loop configurations, but some are ring and common-bus.

Fiber optics offers extremely high data rates. However, because low-cost components are available only for point-to-point connections, the topologies are limited. The major applications are in star systems that require links with high noise immunity and trunk lines. In most cases the systems operate at only a small fraction of the potential data rates so low-cost data sets can be used.

Increasingly the choice of media and architecture will be made by users and their building architects. New office, industrial and research centers are being built with cabling intended to form the backbone of local data networks. □

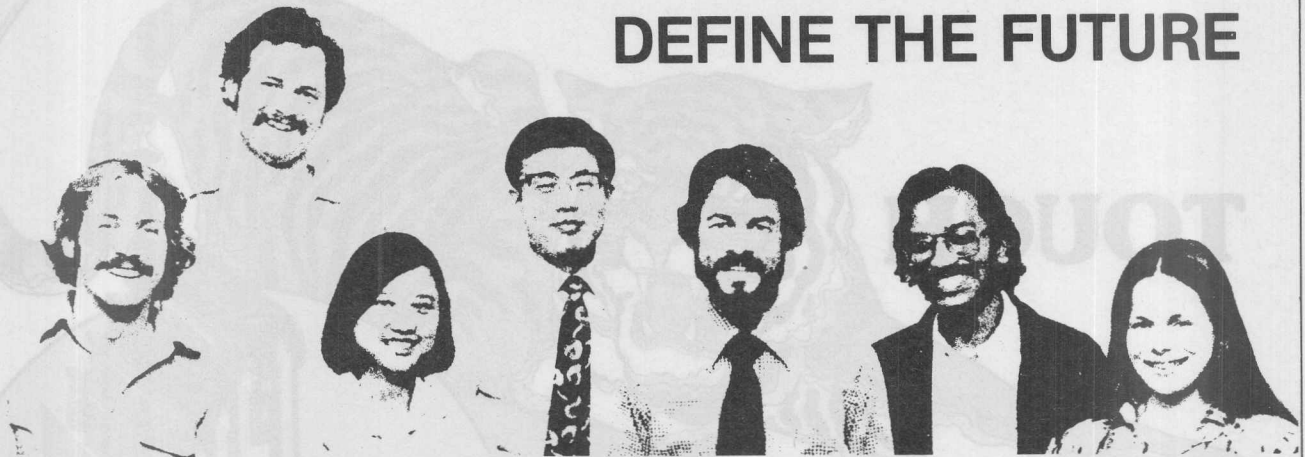


3. Net/One has dedicated and programmable interfaces for existing equipment. Special network software is developed with the NDS subsystem.



4. One of many local bus systems designed to interconnect microcomputers with shared resources is Omninet. The bus consists of RS-422 links, with carrier sense for multiple access.

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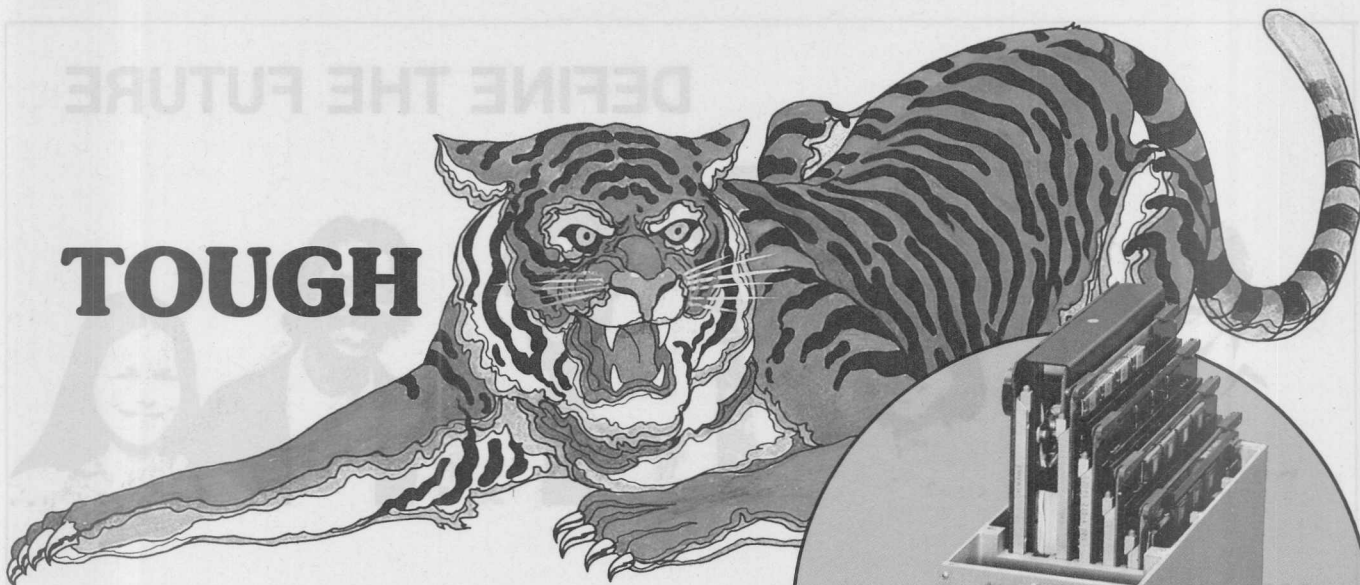
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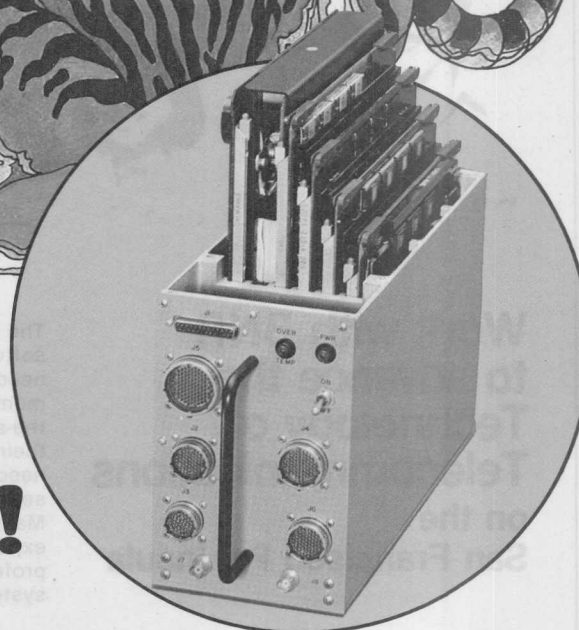
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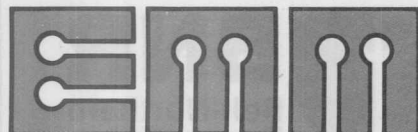
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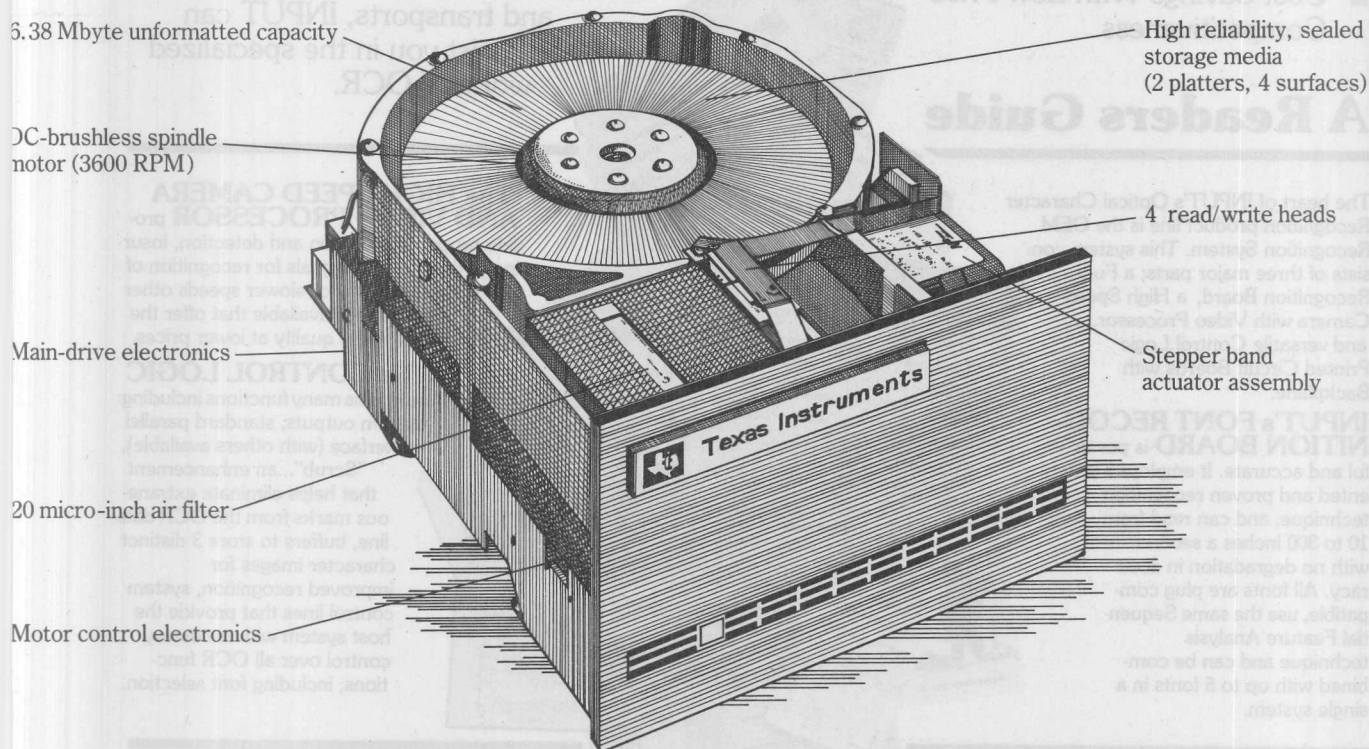


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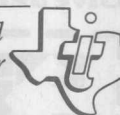
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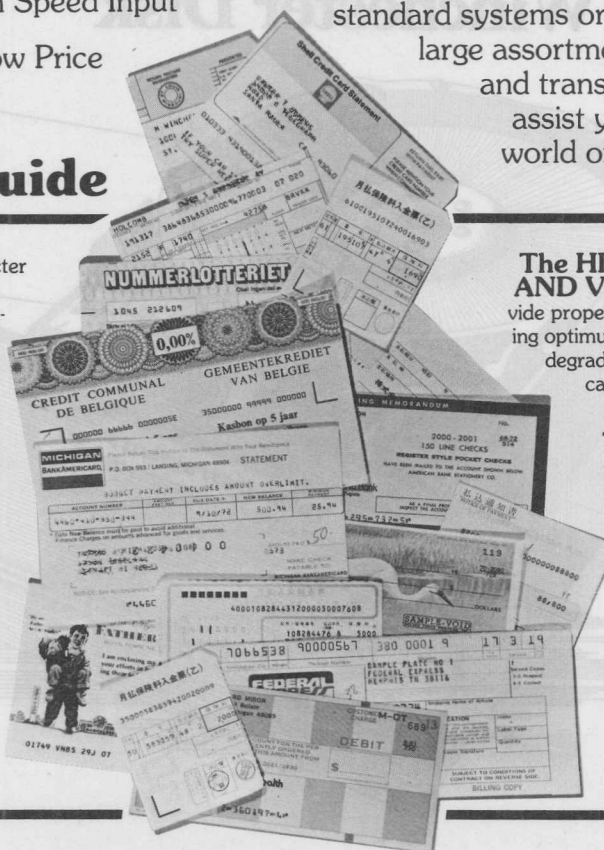
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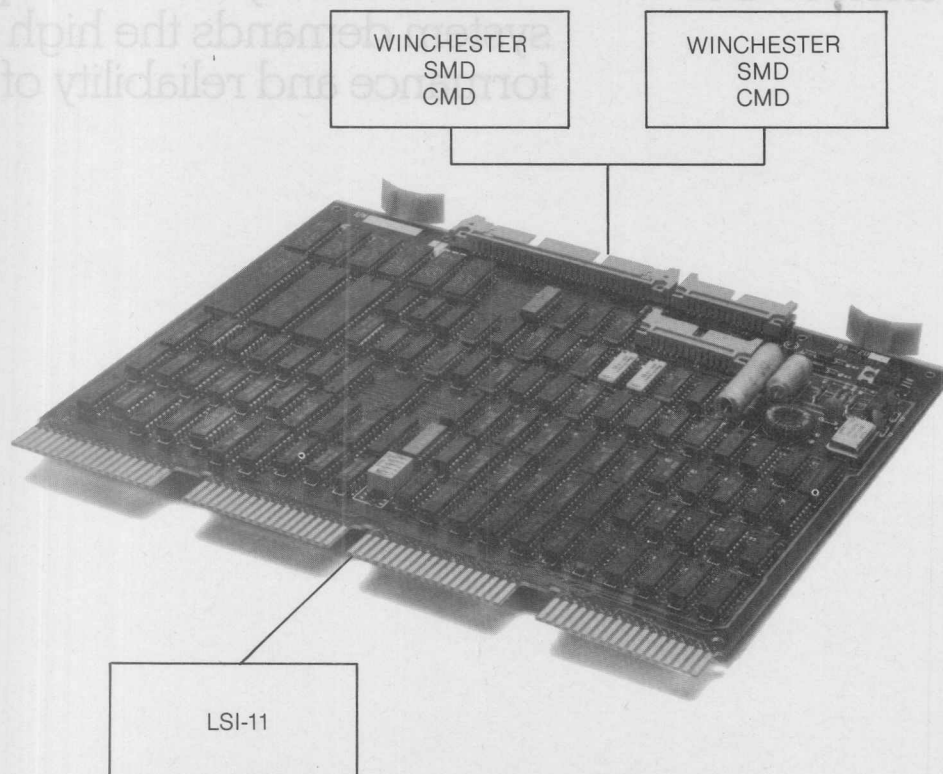
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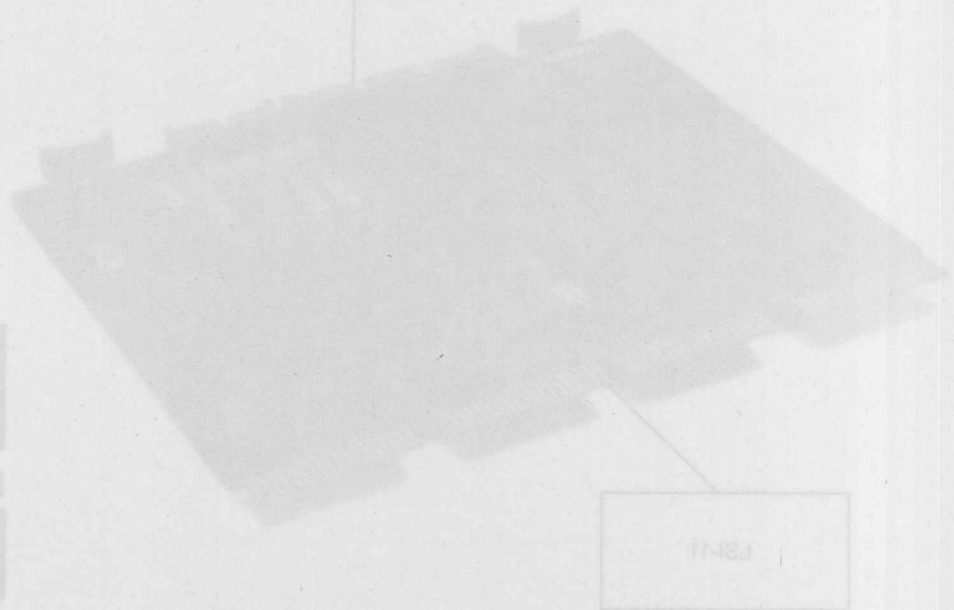
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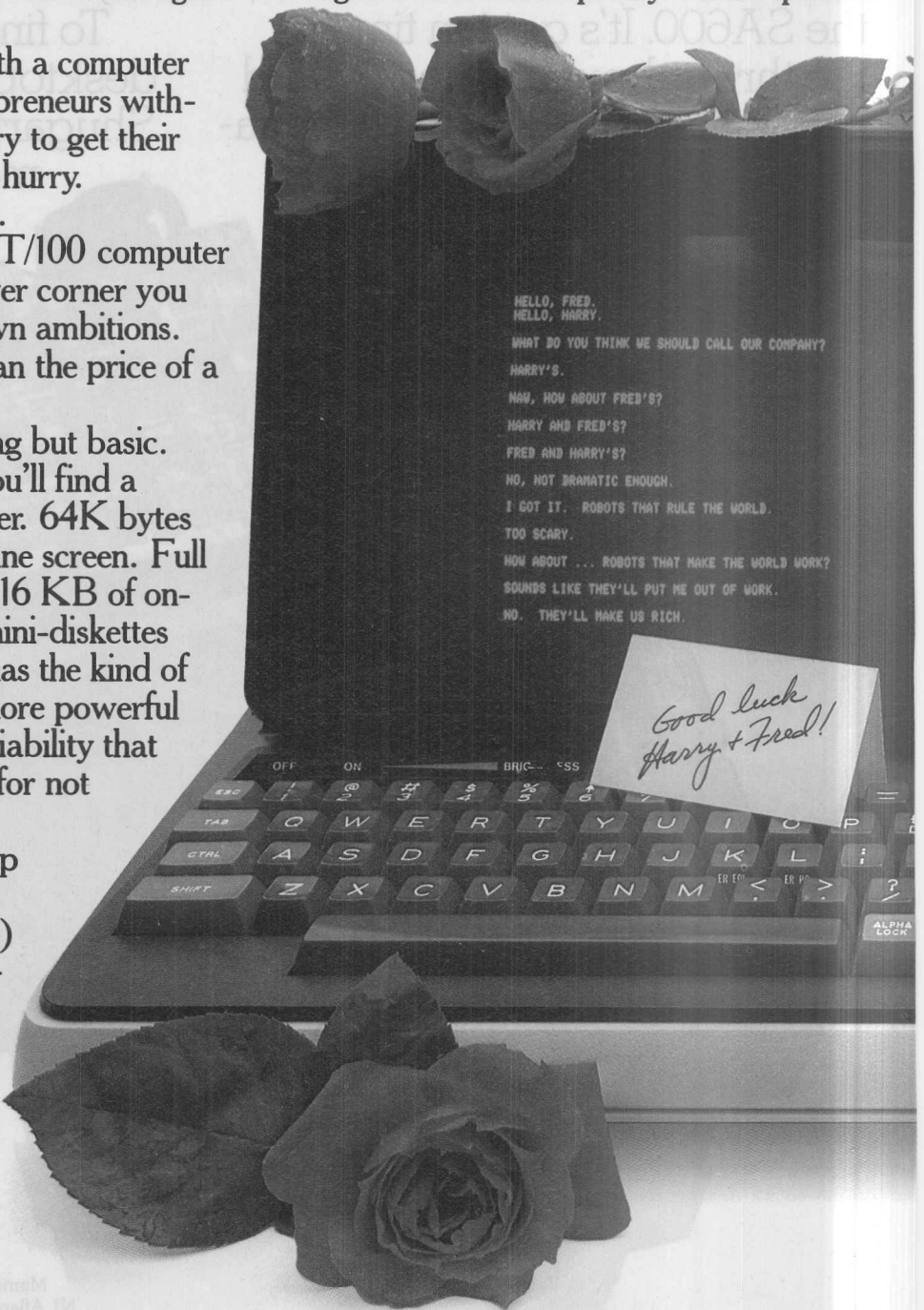
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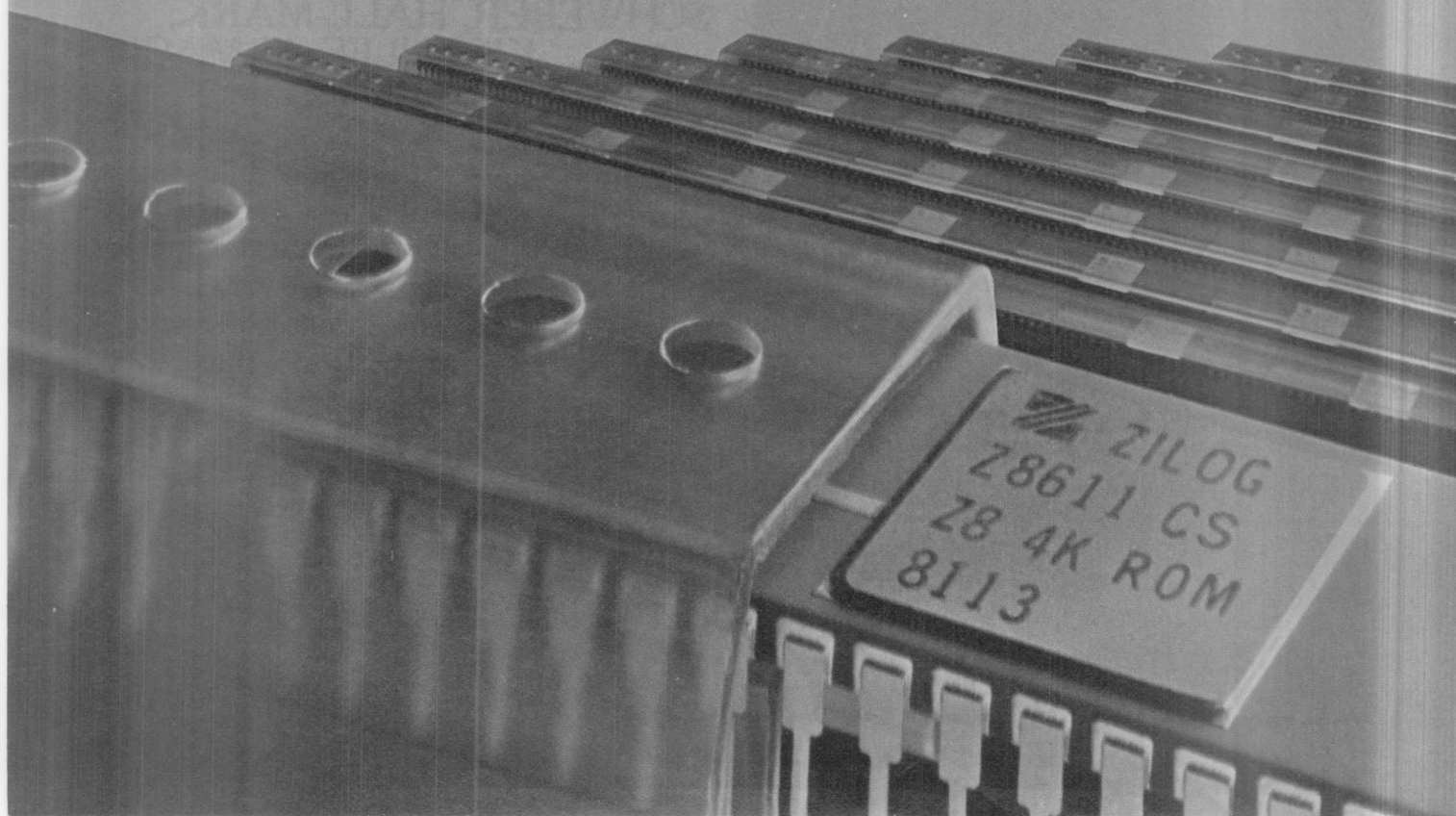
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CIRCLE 112



LAN standards controversy looms: Ethernet vs IEEE-802

Defining communications rules within local-area networks becomes a problem when a protocol standard must be selected.

Designers of local-area networks face a common challenge: defining the rules for intranet communications. One big problem is there are too many "standards" to choose from: *de facto* standards like IBM's System Network Architecture (SNA) and proprietary standards developed by other companies. And now, an "industry standard" called IEEE-802 is in the works. Though it will probably attain formal status by the end of 1982—after the originating committee and several layers of reviewers evaluate and approve it—even then, it will have to contend with an architecture like Ethernet—a proprietary standard with enough support to become a *de facto* standard.

SNA is attractive simply because it comes from IBM. It offers a plug-compatible market, and is a complete, multilevel system. But SNA is also a complex protocol, not really suited for LANs (see "The IBM Alternative").

IEEE-802 and Ethernet share enough common ground to square off naturally. For one thing, Ethernet, developed by Xerox and supported by Intel Corp. and Digital Equipment Corp., provides an access method called CSMA/CD (carrier-sense, multi-access with collision detection). So does IEEE-802. But the differences between the two are significant.

Physically, at least, they look alike. Both systems consist of one or more segments of coaxial cable, up to 500 meters long and terminated in 50 ohms at each end. Each segment contains up to 100 transceivers, separated by multiples of 2.5 m—a distance chosen to minimize interference from reflections caused by impedance mismatches at the transceivers. Each station can be up to 50 m from its transceiver. Repeaters are used between segments and count as one transceiver.

No two stations can be more than 1500 m apart, but this distance can be extended to 2500 m by using a point-to-point link of up to 1000 m that is logically part

of a single repeater. Such a point-to-point link would be used primarily between segments in adjacent buildings. Repeaters with or without the point-to-point link can be connected anywhere along the segment, subject to the 2.5-m spacing requirement for transceivers. This gives the network a tree structure, but without a "root" or central controller.

Ethernet specifies a maximum of 1024 stations. IEEE-802 does not specify a maximum number of stations, but it does give the same separations. However, the committee's original objectives included "at least" 200 devices along "at least" 2 km.

In both networks (the baseband part of 802), the cable and interface specification are quite rigid to ensure compatibility between products of different manufacturers. However, the transceiver-cable specification is looser, offering terminal designers some leeway in trading off parameters.

Defining levels 1 and 2

Both systems take into account the two lowest levels of the seven-level ISO architecture. "Dealing with only those two levels is itself a pretty big job," says Maris Graube, chairman of the 802 committee and manager for corporate interface engineering at Tektronix, Inc. (Beaverton, OR). The principal objective is to allow interface chips to be designed by different manufacturers with different approaches, while remaining functionally compatible. Meanwhile, standardization at the higher levels is being undertaken by the National Bureau of Standards; proposals at levels 3, 4, and 5 are out now or will be by the end of 1981. Levels 6 and 7 are targeted for 1982.

For outgoing messages, data transferred from level 3 are supplied with addresses and a frame check sequence at the data-link level (level 2). The information is then forwarded to the physical level (level 1), which places a synchronizing preamble on the coaxial cable, serializes the frame, and transmits it.

An incoming frame is preceded by a preamble, which is used by level 1 to adjust its circuits, and then discarded. The remainder of the frame, after conversion to parallel form, is sent up to level 2, which inspects the destination address and discards the frame if the address is not recognized. If the address

Systems & Software: LAN standards

is recognized, the source address and the data field are sent to level 3. (The source address is processed at a higher level, not defined in either Ethernet or 802, but space for it is reserved in the frame, defined at level 2). The frame-check sequence, following the data field, is used for error detection at level 2, but correction or other consequential action is reserved for higher levels.

What's more, neither the Ethernet specification nor the 802 draft is concerned with real-time processes. Both systems leave real-time processing as well as encryption and other high-security measures to higher levels.

On the other side of the coin, one major difference between Ethernet and 802 is their treatment of options. Ethernet has a tightly drawn set of specifications with no options, to ensure that every Ethernet system is compatible with every other, anywhere. Its protocols have also been reduced to firmware. IEEE-802, on the other hand, allows several optional features, which permit a network or a terminal to be tailored to a particular application. As a result, when 802 becomes final, the mere existence of two or more networks adhering to it will not ensure their compatibility; nor will any manufacturer be able to advertise an "802-compatible" product without specifying which options the product incorporates. (The same situation arose with the IEEE-488 general-purpose interface bus standard, and is now slowly being resolved by *de facto* implementations of the standard.)

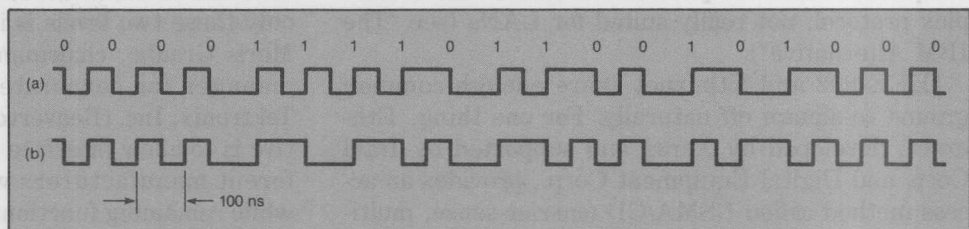
The transceiver cable, which connects the transceiver to the station, is defined differently in Ethernet

and 802. In Ethernet, the cable contains four shielded twisted-pair conductors carrying receive and collision-detect signals to the station, and transmit signal and power to the transceiver. In 802, the cable contains five shielded twisted pairs, carrying no fewer than ten logical signals, including an idle state. Because these signals are logical rather than physical, some of them are no more than the absence of a prescribed waveform on the corresponding pair. As in Ethernet, one pair carries power from the terminal to the transceiver.

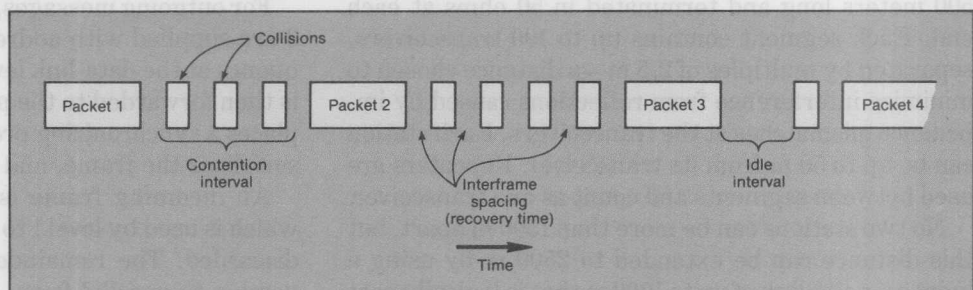
Every Ethernet system has a 47-bit address, with one extra bit that specifies whether a given address identifies a single station or a group of stations. Addresses are assigned by Xerox to the station manufacturer. Thus, any Ethernet station can be used on a particular Ethernet.

IEEE-802, on the other hand, allows addresses of one to seven bytes. One bit of the first byte of a destination address indicates whether the address is of an individual station or of a group of stations. The corresponding bit in a source address indicates whether the frame constitutes a command or a response. Another bit of each byte in both destination and source addresses indicates whether another address byte follows the current one.

For data and control signals, Ethernet uses straight Manchester phase encoding, while differential Manchester phase encoding is specified for 802 (Fig. 1). The two encoding methods have similar waveforms and spectra, but the differential form reportedly has advantages in error monitoring.



1. Straight Manchester phase encoding is distinguished from (a) differential Manchester (b) by how the center transition represents a bit. In the straight form, a ZERO is a negative transition and a ONE is positive. In the differential form a ZERO is in the same direction as the preceding bit, and a ONE is in the opposite direction—regardless of the value of the preceding bit.



2. Contention-based access allows any station to use the bus at any time provided it first checks to see that the bus is not in use. Collisions occur when two stations try to start at the same time.

Feature	Ethernet	IEEE-802
Data rate (Mbps/s)	10	1-20
Max. nodes	1024	—
Max. nodes per segment	100	100
Max repeaters per segment	2	2
Max station separation	2.5 km	2.5 km
Max segment length	500 m	500 m
Medium	Shielded coax, baseband signal	Shielded coax baseband or broadband
Encoding	Manchester phase	Diff. Manchester phase
Topology	Nonrooted tree	Nonrooted tree
Access	CSMA-CD	CSMA-CD or token passing
Levels	1 and 2	1 and 2
Frame organization		
Synchronization (bits)	64	64
Address (bits)	47	6 to 42
Type or control field (bits)	16 (T)	8 (C)
Data (bytes)	46-1500	46-1500
Frame check (bits)	32	32
Frame spacing	9.6 μ s	Depends on data rate

Both Ethernet and 802 divide messages into frames, which are similar but not identical. Ethernet has a type designation of 2 bytes, while 802 has a 1-byte control field—in both cases immediately following the two address fields. The type and control fields are used at higher levels in the ISO architecture, but are included in the frame definition at level 2 to establish a convention permitting multiple higher-level protocols to use the level-1 and 2 network. Both systems then allow a data field that can range from 46 to 1500 bytes (or octets), and finally a frame check sequence of 4 bytes.

A synchronizing preamble of 64 alternate ONES and ZEROS precedes the frame in Ethernet. IEEE-802 specifies a more complex bit pattern in its preamble; should an error crop up in the preamble, the 802 scheme is less likely to begin frame transmission prematurely.

Ethernet transmits at 10 Mbps/s, whereas 802 allows 1, 5, 10, or 20 Mbps/s. In the case of broadband transmission under 802, video and audio signals can be added to any of these rates.

Question of access

Access to the transmission medium (coaxial cable) differs sharply in Ethernet and 802. In Ethernet, any station can transmit to any other station when the bus is not in use. Conflicts that arise when two or more stations try to begin transmission simultaneously are

copied almost word for word from the Ethernet specification. However, 802 also offers an alternative called token passing.

IEEE-802 recommends both contention-based and token-passing access methods—incompatible but recommended “to keep everybody happy,” says committee chairman Graube. The committee, Graube says, was split about 50-50 over the two methods. Since approval of one or the other requires a 75% consensus, recommending both allowed a draft to be produced.

One reason for the split is that several computer manufacturers are already using token-passing ring and bus networks in proprietary products, and others plan to use it. Several large minicomputer systems are actually a group of minicomputers linked by token-passing networks. Also, token passing is more suitable for systems that must allow for priority access, such as large computer networks. In its purest form, token passing is used in a ring topology, in which all nodes are equal, and in which (generally) there are two paths from any node to any other node, going clockwise or counterclockwise around the ring.

In token passing, as in CSMA/CD, only one station in the network can transmit at a time, but no conflicts can arise (at least theoretically) because only one station can possess the token that permits it to transmit. (A third option is also available in 802, that of broadband transmission, allowing several terminals to use the medium simultaneously. Their messages are frequency-multiplexed on the cable).

Being contention-based, CSMA/CD allows a station to take over the network for message transmission at any time, provided it first listens to make sure no other station is transmitting. However, two or more stations could simultaneously listen, hear nothing, begin transmission, and “collide.” They would then back off, each for a random time, and try again. In Ethernet, the collision generates a detection signal. In 802, a similar signal indicates the *absence* of a collision; a dc level indicates a collision.

If a collision occurs in less than the total network propagation time, a jamming signal is transmitted in both Ethernet and 802 to make sure all stations know that a collision has occurred. Following the jam, each would-be user waits for a random time—a few tens of microseconds—and tries again. (The waiting time is unlikely to be the same for both contenders). Because the waiting time is random, the probability of a second collision is less than on the first try. Sooner or later, a station should manage to seize the line.

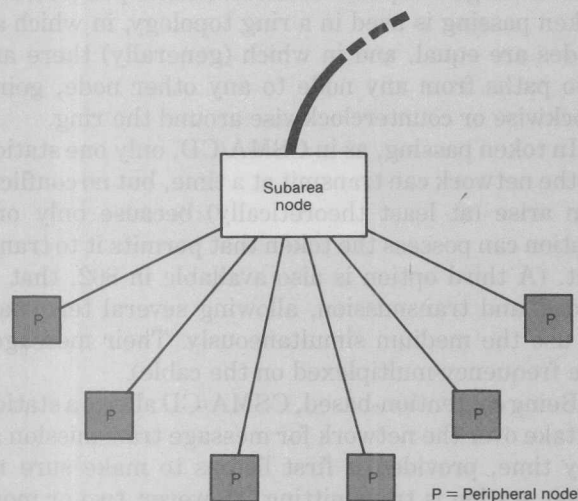
Ethernet and 802 both give up after 16 attempts (one original attempt and 15 retries), at which point level 2 reports “excessive collision error” to higher levels of the network.

CSMA/CD is well known and easy to put on a single

The IBM alternative

Although it can be used in local-area networks, System Network Architecture is much more suitable for large computer networks with terminals great distances apart. But since large networks often contain clusters of terminals close together, SNA provides for "subareas," each of which might be considered a local network. These subareas can be interconnected via shared communication links. However, a subarea is a logical rather than physical entity—it could cover an entire state.

In IBM parlance, each subarea contains one "subarea node" and a number of "peripheral nodes" (see Fig.). Connections between a subarea node and its local peripheral nodes can be hard-wired or they can be switched, nonswitched, or multipoint common-carrier lines that use the SDLC protocol. There are no maximum separations between stations or specified communications media, such as coaxial cable. Also, there is



no maximum number of peripheral nodes per subarea node, but since the area has a star or loop topology, the number is limited by the physical and logical number of connections that the subarea node can handle.

The star topology is an important distinction between SNA and most local-network architectures. Local networks usually contain many autonomous stations, each handling its share of network control. This autonomous behavior requires a prescribed technique for gaining control of the communication line before beginning to transmit.

No such technique is prescribed in SNA; the star topology implies the presence of a central controlling node, which polls the subsidiary stations or responds to interrupts from the other stations. The controlling node may be another station that is "more equal" than the others, or it may be a large central computer. Data may move from one node to another within a subarea independent of polling. That is, once the central controller has started communication between two nodes, they handle the transaction themselves.

integrated-circuit chip, permitting simple implementation in a host's interface circuitry. However, it becomes inefficient when traffic is heavy—more than about 30% of channel capacity. (However, an experimental Ethernet, in use for several years at the Xerox Palo Alto Research Center with many kinds of stations, has rarely exceeded 3%.)

What's more, under such a scheme, bus length, data rate, and frame length are closely interrelated:

$$2t_p = L/R$$

where t_p is the propagation time in seconds, L is the length of the main cable in terms of the number of bits that can be simultaneously in transit, and R is the data rate in bits per second. Twice the propagation time must be less than the time required for a station to put an entire frame on the cable. This protects two stations, A and B, at opposite extremes of the network, from garbling each other's messages.

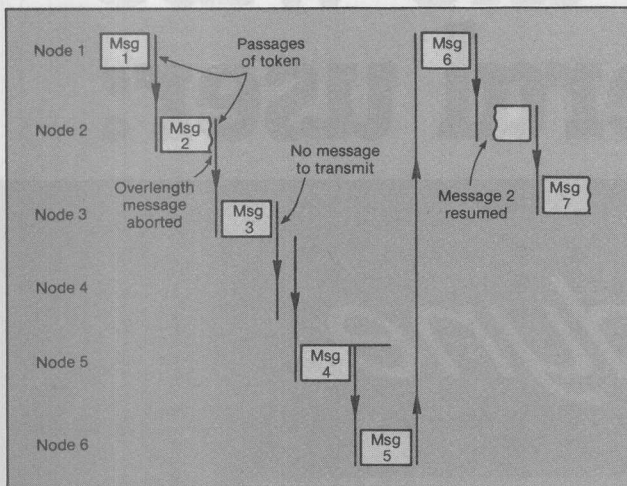
However, any change in one of these three parameters affects the others. This problem can be serious in a network serving a growing company, which may find that it cannot expand its network operations without a major restructuring. Nevertheless, within those limits, adding a station to a network with contention-based access involves merely plugging it in.

Token-passing access permits a station to transmit only at stated times, when it possesses a "token" allowing it to use the network (Fig. 3). When a node completes a transmission, or when an allotted maximum time elapses, it transmits a signal to the next node in a prescribed sequence. This signal says, in effect, "Go ahead, it's your turn now."

Token passing can be used either in a ring or on a straight bus. In a ring, the logical order for passing the token is usually, though not necessarily, the same as the physical order. Data frames or tokens transmitted by any station go only to the next station on the ring; that station either accepts the frame or repeats it for further propagation along the ring. If the originating station gets the frame back, it knows that nobody wanted it or that the station to which it was addressed is inactive. If the frame does not come back, either the addressee has it or the ring is broken; the originating station does not know which unless it asks the addressee for an acknowledgment.

In a bus, the logical order for passing the token need not, and usually does not, have any relation to the physical order of the stations. Data frames or tokens transmitted by any station always go to all other stations, and—unless they were addressed specifically to all stations—only one station accepts them. Here, too, the originating station does not know the fate of the frame unless it asks for an acknowledgment.

With either topology, a node that receives the token but does not need the network at that moment imme-



3. Token-passing access gives a station access to the bus only in its turn. A "token" representing the privilege of transmitting is handed around in a prescribed order to permit all stations to transmit.

diately retransmits the token to the next station in logical sequence.

Token passing is not subject to random and unpredictable delays caused by contention—only to fairly predictable delays. Moreover, the three parameters that are interlinked under CSMA/CD—bus length,

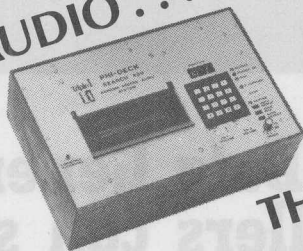
frame size, and data rate—are independent.

However, the token sender must be able to recognize that the token receiver actually received the token. The latter might, for example, have suffered a power failure or other breakdown. This could cause the token to be lost completely, and keep the entire network down until the token can be regenerated. Practical ring networks have generally solved the problem by having a main channel that transmits clockwise around the ring and a counterclockwise channel serving as backup. But such methods are of little value at the moment of failure, since they work after the fact and cannot help locate the lost token.

Adding a station to a token-passing network requires the preceding station in the token-passing order to be informed. Or, allowances must be made in the addressing structure. (Since this can involve software changes at higher levels, it is not as easy as it looks.)

Such considerations make token passing a more complex process at the local-net level than the contention-based access method. But several computer companies prefer its architectural flexibility as well as its ability to fit into hierarchical networks. Some, in fact, use a combination of token passing and HDLC for compatibility with international networks. □

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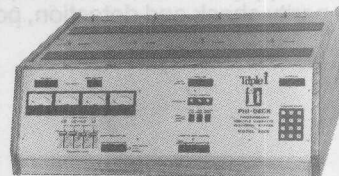
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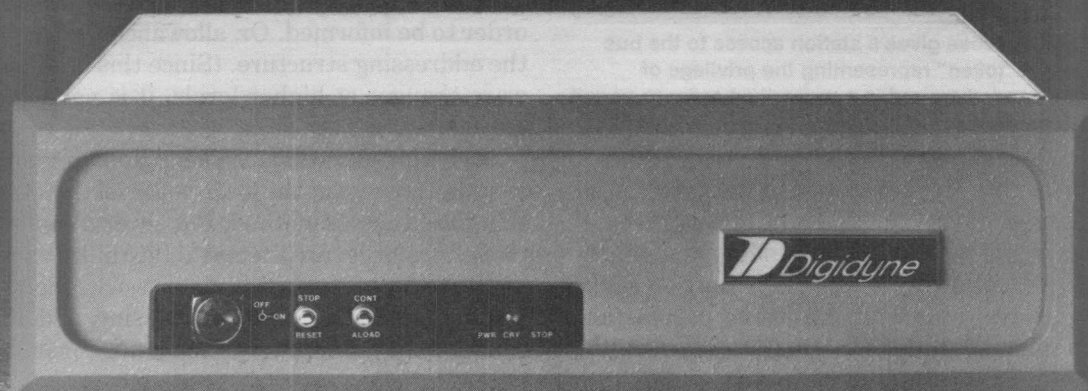
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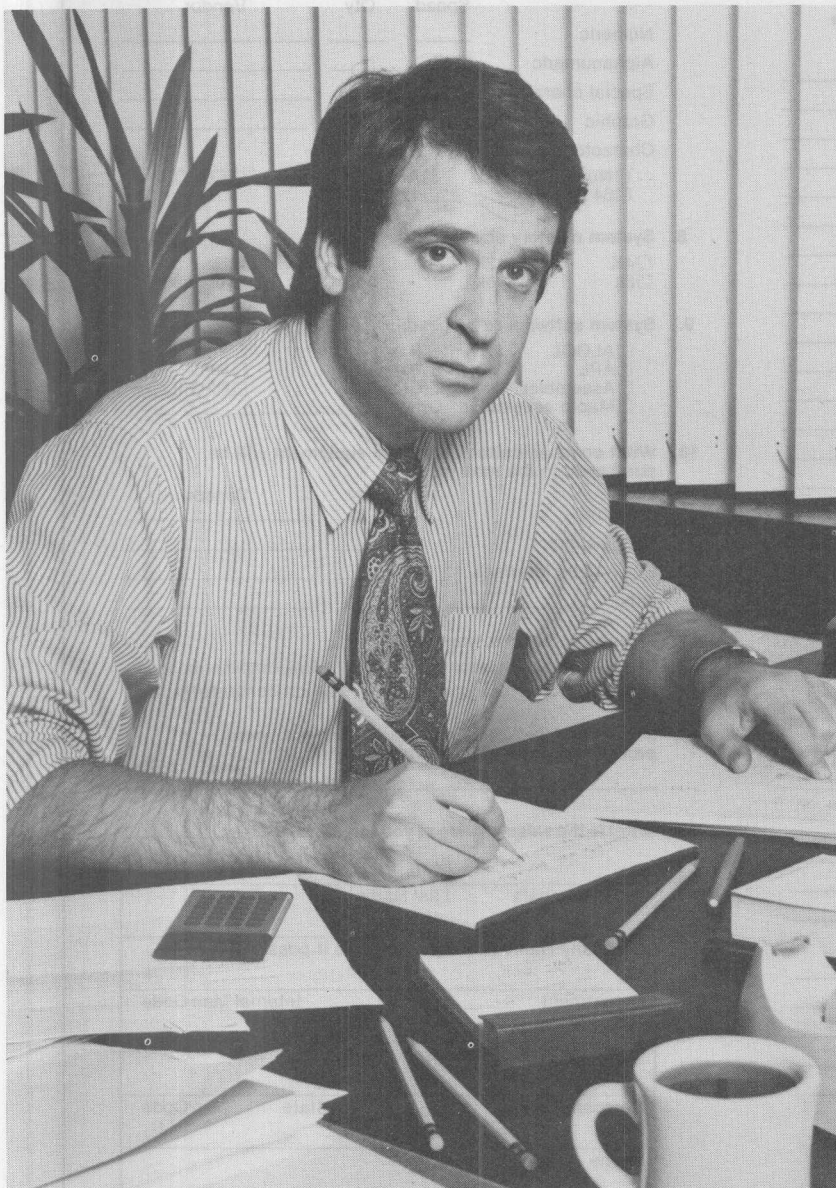
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3. Which CPUs are you considering for your computer-based design:

1 _____ 3 _____
2 _____ 4 _____

4. Please specify the new peripherals to be purchased in the next year.

	Qty	Vendor
CRT displays	_____	_____
Intelligent terminals	_____	_____
Line printers	_____	_____
Serial printers	_____	_____
Nonimpact printers	_____	_____
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Remote-batch terminals	_____	_____
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Other	_____	_____

5. What types of CRT terminals are you designing into your system?

Type	Qty	Vendor
Intelligent	_____	_____
Dumb	_____	_____
Graphic	_____	_____
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Character Set		
Numeric only	_____	_____
64 ASCII	_____	_____
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Size _____ Capacity _____

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Application _____

7. Please indicate your company's plans for printer purchases in the next year.

	Speed	Qty	Vendor
Numeric	_____	_____	_____
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☐ APL ☐ Pascal ☐ RPG
☐ Assembler ☐ COBOL ☐ RPG II
☐ Macro assembler Other _____

10. What communications interface equipment will be purchased in the next year?

	Qty	Vendor
Modems	_____	_____
Multiplexers	_____	_____
Fiber-optic interface	_____	_____
Other	_____	_____

11. Please characterize your system:

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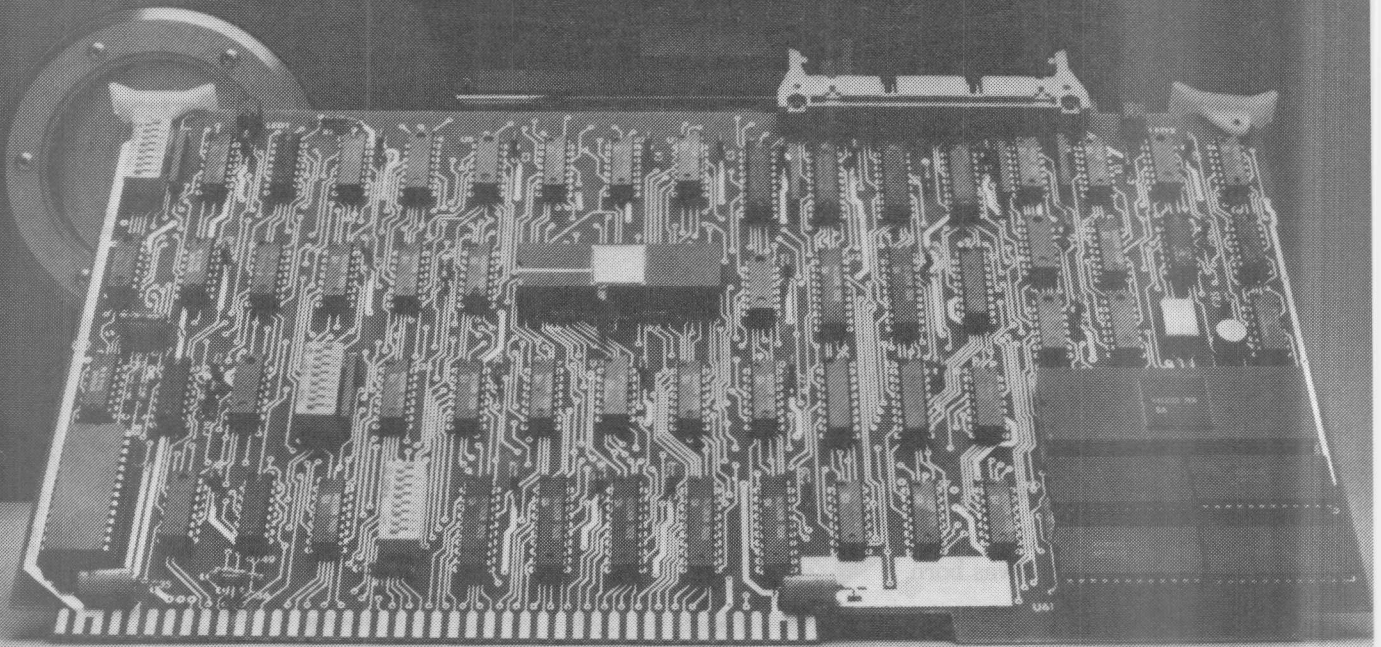
12. Indicate the nature of your application (i.e., word processing, industrial control, scientific, etc.)

13. What is the sales volume of your organization?

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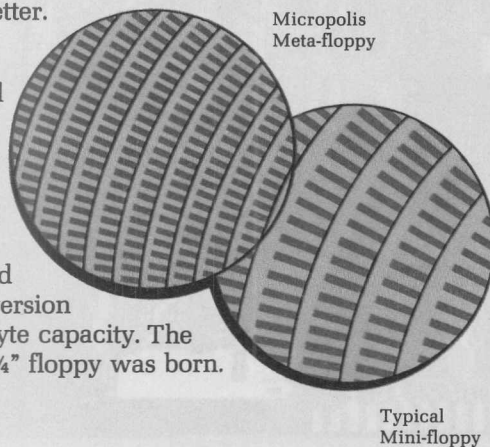
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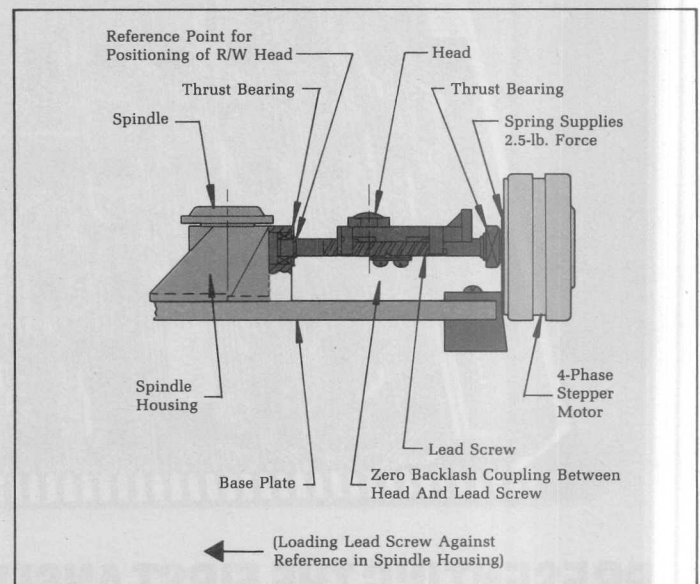


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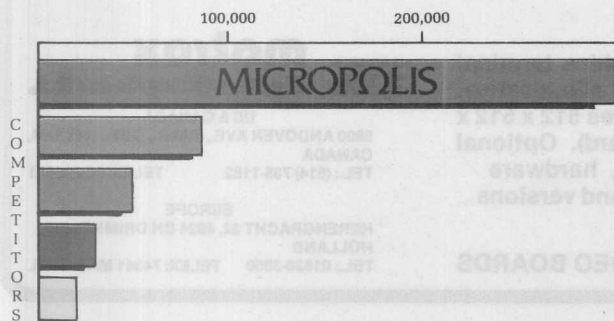
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facts about 5 $\frac{1}{4}$ " floppies

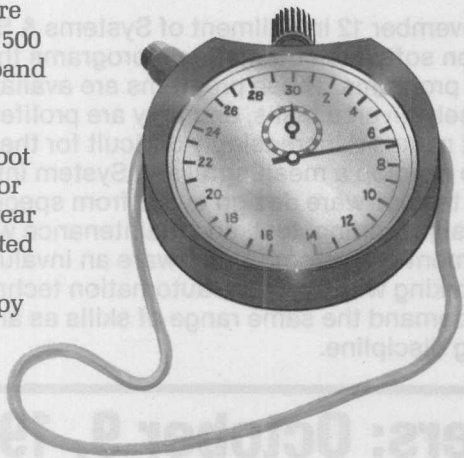
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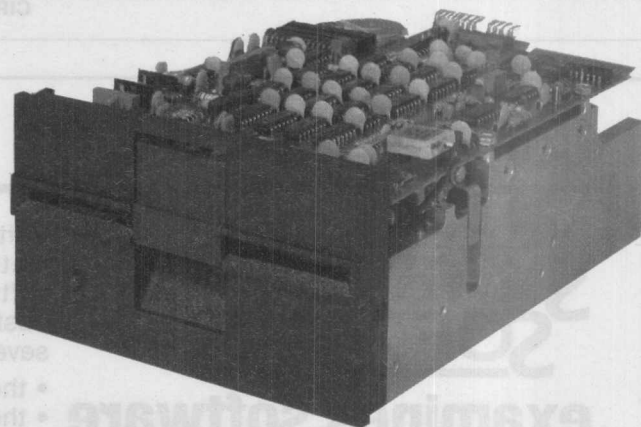
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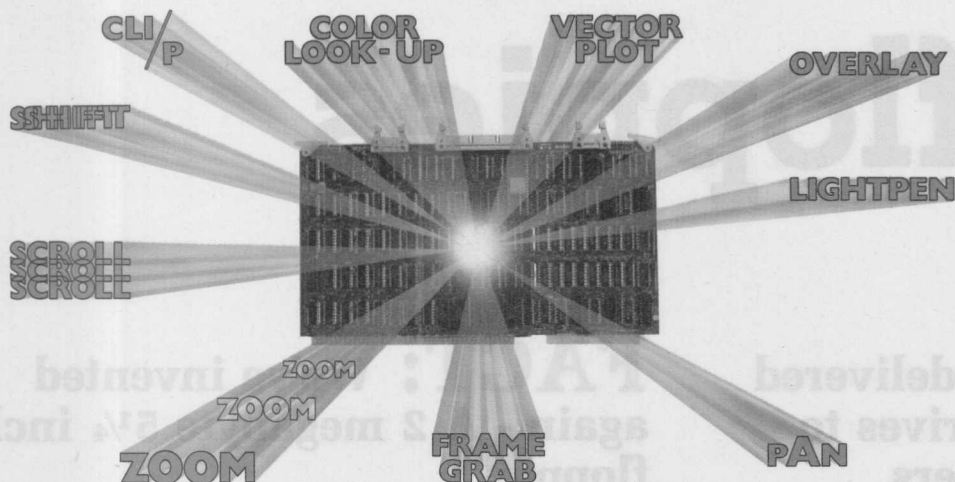
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CIRCLE 117

Coming November 12

ElectronicDesign

SYSTEMS & SOFTWARE

examines software automation—techniques for the development and management of computer software

Software now accounts for 80% of a computer system's lifetime cost, and will approach 90% by 1990. Whether software is to be a major contributor—or the biggest obstacle—to industry growth depends on this trend and several other factors, including:

- the availability and quality of programmers,
- the contributions of high-level languages and software components,
- and current trends in software tools.

The November 12 installment of Systems & Software will focus on software automation—programs that help write other programs. These programs are available today for immensely diverse tasks, and they are proliferating at a pace that makes it increasingly difficult for the software engineer to develop a meaningful set. System integrators involved in the software design cycle, from specification through design, coding, test, and maintenance will find this installment of Systems & Software an invaluable guide to working with software-automation techniques, which will demand the same range of skills as any other engineering discipline.

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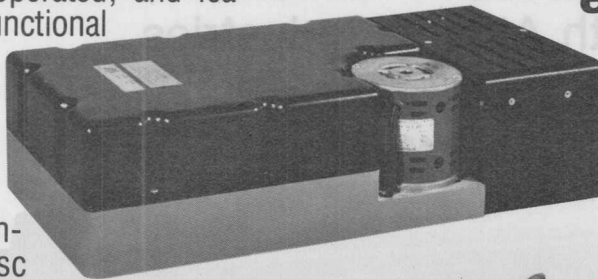
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CIRCLE 119



Software helps networks grow with compatibility

LAN software, to set up reliable communications between growing user software processes, will help maintain orderly transitions to future applications.

Productivity, productivity, and more productivity—that's the local-area-network challenge to software developers. The pressure is on to make a transition from resource sharing, a popular initial application that reduces the cost per user of data bases, document bases, and expensive equipment, to new forms of distributed data processing and database management that will improve productivity. Major investments in new software hang in the balance. Fortunately, major trends in local-network support are aimed at cutting the problem down to size—and at providing an orderly transition to future applications.

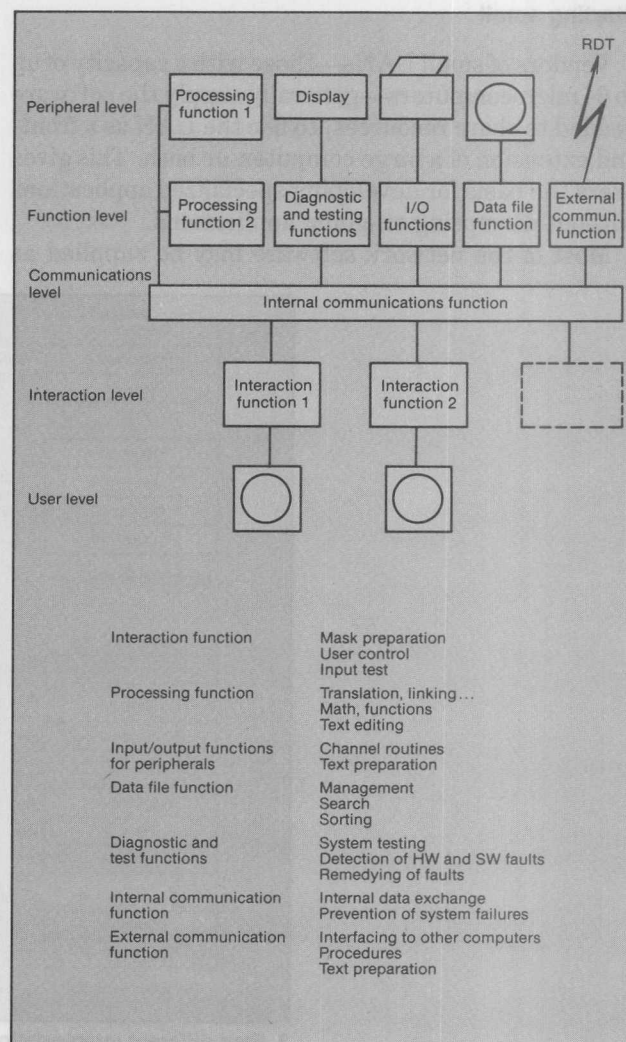
Most existing applications software will remain usable because of efforts made, on the one hand, by computer manufacturers and LAN vendors to keep new links compatible and, on the other hand, by operating system vendors to provide compatibility with new protocols. In between, agreement is growing on the intermediate protocols for the newer packet-switching systems.

Since the Arpanet fathered packet communications for distributed processing, Arpanet protocols are coming to the fore in Ethernet and similar systems. The X.25 protocols (which include HDLC) are also in use locally, as well as in gateways to public packet networks. Since X.25 can be a common ground, CSMA/CD systems with X.25 gateways are becoming available.

This adds up to incentives for LSI manufacturers to develop more LSI protocol chips and less software. Meanwhile, researchers are also working on new architectures for host software. For example, Siemens AG Research Labs (Munich, Germany) has been studying the decomposition of functions for multiprocessor office computers (Fig. 1). The experiments are part of a project to develop a fiber-optic broadcast bus that uses X.25 protocols.

George Sideris, Contributing Editor

The common objective in LAN software design is to establish reliable communications between user software processes. Three basic forms are used in packet-switching systems: reliable datagrams (the receiver acknowledges transmission of undamaged packets), messages (the LAN software or firmware multiplexes and demultiplexes the packets of the data block being transferred), and virtual circuits (seemingly continu-



1. Both the microprocessors of future office computers and the system software could be distributed along a local network. The software system would be decomposed for allocation to hardware modules.

Systems & Software: LAN software

ous, end-to-end connections).

Even though the packets are only about 512 bytes to a few kbytes long, these techniques can handle transfers up to hundreds of kbytes with better response time, as a rule, than if the data were being accessed on a floppy disk at the workstation.

Layered system architectures allow the communications functions to be added "under" existing system software, so the LANs mate well with existing applications and user business procedures. As a result, the layering approach has proved irresistible, even though few designers follow the ISO-OSI model religiously (Fig. 2).

Typically, the first application is cost reduction—the LAN allows a hard-disk system to be shared by several microcomputer users, along with a printer and telecommunications port. File sharing, electronic mailing, and other productivity-improving applications are then added on.

Starting small

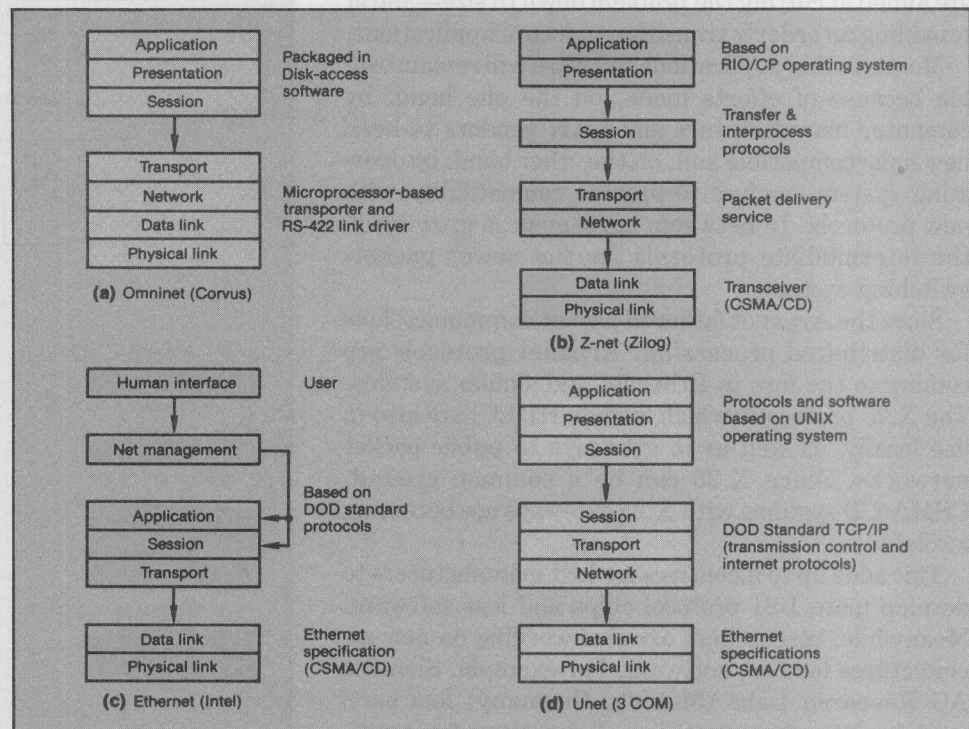
Vendors of small LANs—those with a capacity of up to 64 microcomputers—generally supply the software needed to share resources, to use the LAN as a front-end extension of a large computer, or both. This gives users the basis for developing specialized applications without disrupting on-going applications.

Most of the network software may be supplied as

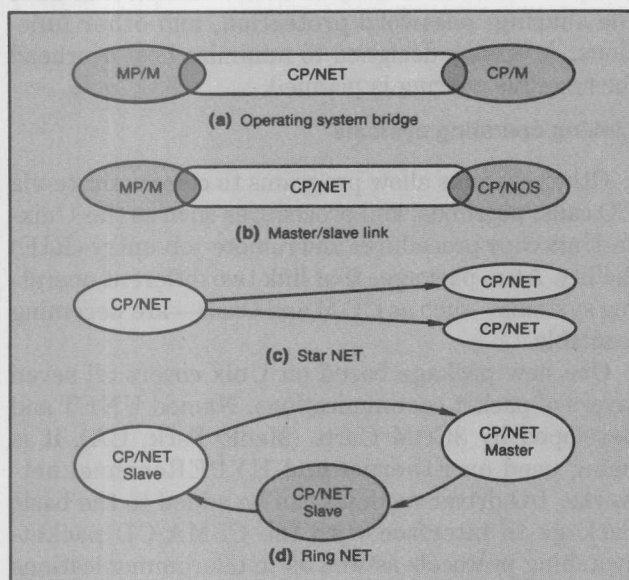
firmware on an interface card for each microcomputer. For example, Cluster/One cards provide all layers required for message transmission. Hardware handles bus allocation, contention resolution, address recognition, and byte transmission, while ROM-based firmware takes care of packet transmission, error detection and retransmission, and grouping of packets into messages. Although essentially a CSMA contention system with variable topology, the link includes a control line that allows a node to maintain access until extensive file transfers have been completed.

At the process-to-process level, host software creates the virtual channels and commands the server operations. The server—a microcomputer that can also be a client of other servers—interprets control blocks of the client's operating system (typically, Apple DOS). It also controls process synchronization and rights to access the resource. These basic services can be extended from file access to data-base management and other services.

In the Omninet system, firmware on a "transporter" card delivers reliable datagrams, leaving messaging and flow control to host software. Each transporter is a CSMA bus contender with RS-422 transceivers. A microprocessor system, Omninet can be modified to couple to the bus of various computers (Apple and LSI-11, initially). Also, it is designed to



2. Four different interpretations of the ISO-OSI architectural model illustrate a split between packaged hardware and software (a), use of software at all levels above the data link (b), addition of standard protocols to proprietary operating systems (c), and the use of standard protocols with a standard operating system (d).



3. Operating systems can be linked with a software bridge like CP/NET into a variety of LANs via point-to-point connections. Data rates over 100 kbit/s can be obtained with conventional protocols and I/O drivers.

operate independently of the host operating systems. Datagrams are simply delivered to sockets (memory areas assigned by the hosts), so a variety of operating systems can be used.

The direct-memory-access (DMA) transfer can be split. For example, addresses and other network-level information can be deposited in one socket and data in another. Besides making it unnecessary for the host to handle nondata bytes, it allows network-use information to be logged as an aid to net management and administration.

Z-Net represents yet another way to build low-cost networks. It provides a reliable datagram service based on CSMA/CD, but each interface is the same basic microcomputer (MCZ-2) that is used as a workstation, controller, or interface to a larger computer. Its CSMA/CD contention-bus interface is a high-speed, serial I/O channel.

The operating systems handle the process-to-process communications. Each station contains an RIO/CP system, a concurrent-processing upgrade of the RIO remote I/O system. This system's multitasking kernel communicates with its counterparts in other stations while other tasks are also running on the same stations. The software provides sockets for the packet delivery service and for user protocols.

Getting larger

Large, general-purpose systems offer datagram and virtual-circuit services. Although they generally use CSMA/CD and other packet-communications protocols internally, they come with interfaces for industry-standard protocols and computer buses.

A baseband system such as Net/One can interface hundreds of workstations, terminal clusters, and computers. It has a datagram service for brief transmissions such as "Where is the file on Mr. Jones" and three types of virtual circuits: session-oriented circuits created by user commands, semipermanent (bound) circuits set up by system-initialization software, and administrative circuits for network management. The administrative circuits are used, say, to interrogate the network and update an address list so that users (and their processes) can communicate with other users and resources by name rather than by logical address.

Ethernet's software architecture is heading in the same direction. The new iLNA (Intel Local Network Architecture) is the first subset of a larger iNA system. All layers above the link layer are modules that can be stored as firmware on a Multibus-compatible interface board, or mixed in with OEM software.

While the link layer handles packet transmission, the transport layer creates virtual circuits and the session layer binds network addresses to processes. The binding functions are designed to keep all communications location-independent—another way of eliminating addressing problems.

A network-management layer contains operating utilities and diagnostics. For instance, it keeps planning statistics, logs illegal messages, locates the stuck transceiver that is jamming the ether, or locates a wet cable section by monitoring transmissions.

Broadband systems like LocalNet can connect over 20,000 users through virtual circuits. More than 100 channels, with different frequencies, connect hundreds of users. If a channel approaches its traffic capacity, transmission can be selectively forwarded over different channels by a net-management subsystem.

Operating systems fit in

Local-network development can also start with any multiuser operating system, such as the CP/M family from Digital Research Inc. (Pacific Grove, CA), Oasis from Phase Four Systems (Oakland, CA), Unix from Bell Laboratories (Murray Hill, NJ) or derivatives like Xenix from Microsoft (Bellevue, WA). Since they all can be adapted to high-speed I/O channels, and provide facilities for resource sharing, they are being used in many systems with point-to-point links. The links are suitable for master-slave bus networks, stars, loops, and other conventional architectures.

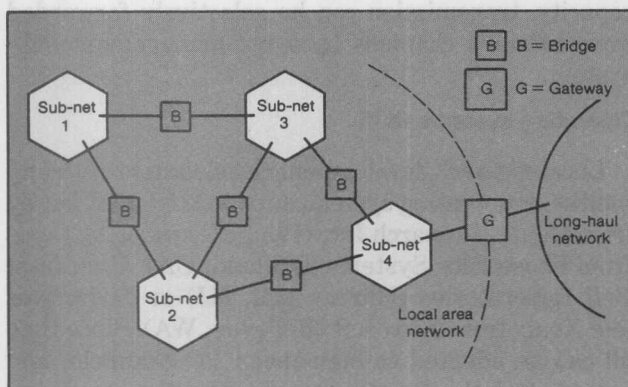
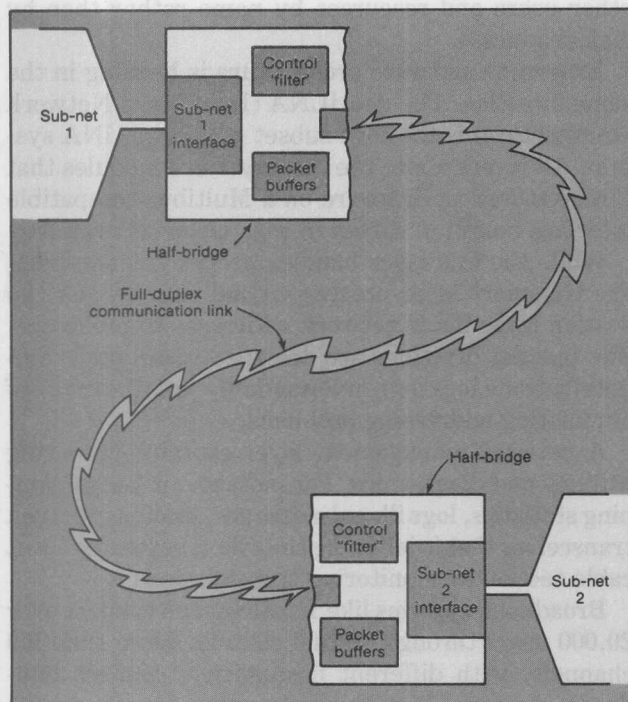
Popular operating systems are being enhanced to cater to OEMs who want to do networking without disturbing existing software. In the CP/M and MP/M family, for example, CP/NET bridges two operating systems (Fig. 3) and CP/NOS provides a slave system

Systems & Software: LAN software

that fits into a 4-kbyte ROM. Current networks run at over 100 kbit/s using RS-232C protocols, but CP/NET is designed to be protocol-independent so custom drivers for new nets can be added.

The networking software intercepts the normal operating-system calls and, if the calls are for a remote system, formats a packet-like message. The receiving host checks the packet for damage during transmission and performs the operation identified by a function code. Addressing is based on identification tables maintained by CP/NET.

Originally released in a disk-sharing version last



4. A trend toward standardizing protocols will simplify bridges needed to interconnect different types of local networks and gateways needed to access long-haul networks.

year, CP/NET now comes in a new version that adds file sharing, password protection, and other functions. A version designed to minimize host overhead for resource sharing is planned.

Linking operating systems

Other systems allow programs to communicate via I/O calls, pipelines, and procedures such as the Unix-to-Unix copy procedures and remote-job-entry (RJE) facility. Also, packages that link two different operating systems—such as CP/M and Oasis—are becoming available.

One new package based on Unix covers all seven layers of packet communications. Named UNET and developed by 3COM Corp. (Menlo Park, CA), it is being used on Ethernet and HYPERchannel networks. I/O driver modules can be added to the basic package to interface with the CSMA/CD packet-switching protocols as well as to telecommunications protocols.

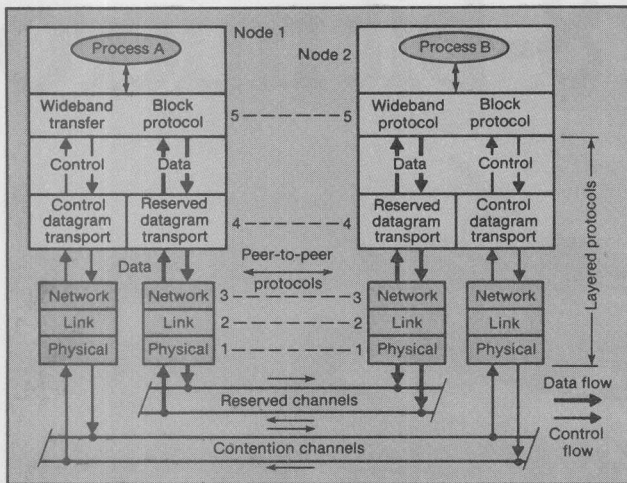
Upper-layer protocols include standard Dept. of Defense TCP (transport control) and IP (internet) protocols along with protocols generally accepted in the telecommunications industry: FTP (file transfer), VTP (virtual terminal) and MTP (mail transfer) protocols. UMTF is compatible with Rand MH and Bell Mail protocols.

At present, most networks are interconnected to other networks—usually telecommunications—through large or small computers operating as communications servers. However, this method is slow, roundabout, and expensive in more ways than one. An interface message processor (IMP) for Arpanet and similar networks is essentially a full-capability mini-computer. An X.25 gateway takes two or three years to develop.

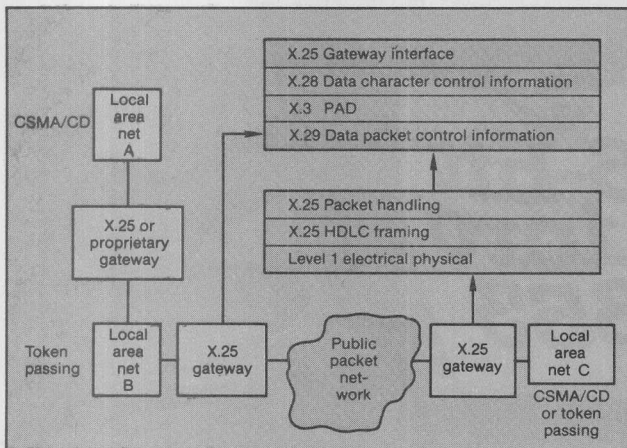
Protocols simplify bridges

Studies conducted at the Massachusetts Institute of Technology and other institutions during the early years of local-network development showed that the software and hardware of internet bridges and gateways would be enormously simplified if higher-level protocols were agreed upon (Fig. 4). The bridge could simply be an interface card that buffers and filters packets (sends them to subnets determined by addresses).

Some LAN developers have backed this concept—particularly those using the CSMA/CD protocol. Ethernet licensees register addresses at the Palo Alto Research Center. Xerox is expected to make the PARC universal protocol (PUP) generally available. PUP is based on Arpanet protocols that led to the current DOD standards and the expected NBS standards. So similar protocols are cropping up in systems like iLNA and UNET (see Fig. 2), and older systems



5. This layered architecture, by using contention, military, and telephone-industry standards for its protocol, combines contention channels for general use and reserved channels for block transfers.



6. X.25 gateways are being added to LANs for telecommunications. Eventually, LSI versions could provide economical interfaces between heterogeneous LANs.

are now starting to add internet bridges.

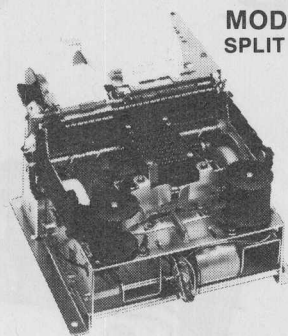
One new architecture for broadband systems, developed by Network Analysis Corp. (Vienna, VA), combines CSMA/CD, TCP, and the telephone industry's CCIS (common-channel interswitch signaling) in its seven layers (Fig. 5). The system provides a series of contention channels, plus reserved channels for high-volume traffic.

The general implication is clear: Semiconductor manufacturers can afford to develop not only HDLC/SDLC, RS-232C, and other conventional protocol controller chips, but also TCP chips. Furthermore, X.25 chips are likely to be in the cards. To this point, a mere handful of equipment manufacturers has been able to develop X.25 gateways acceptable to public packet networks. But several years from now, it could become as economical to plug together local and long-haul packet networks as it is to plug a computer into a local network today (Fig. 6). □

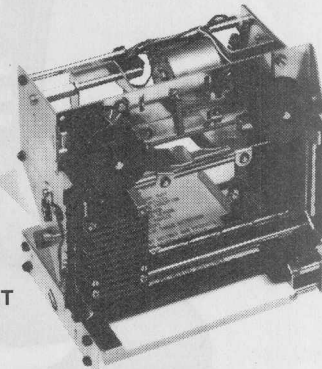
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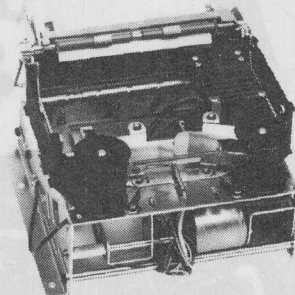
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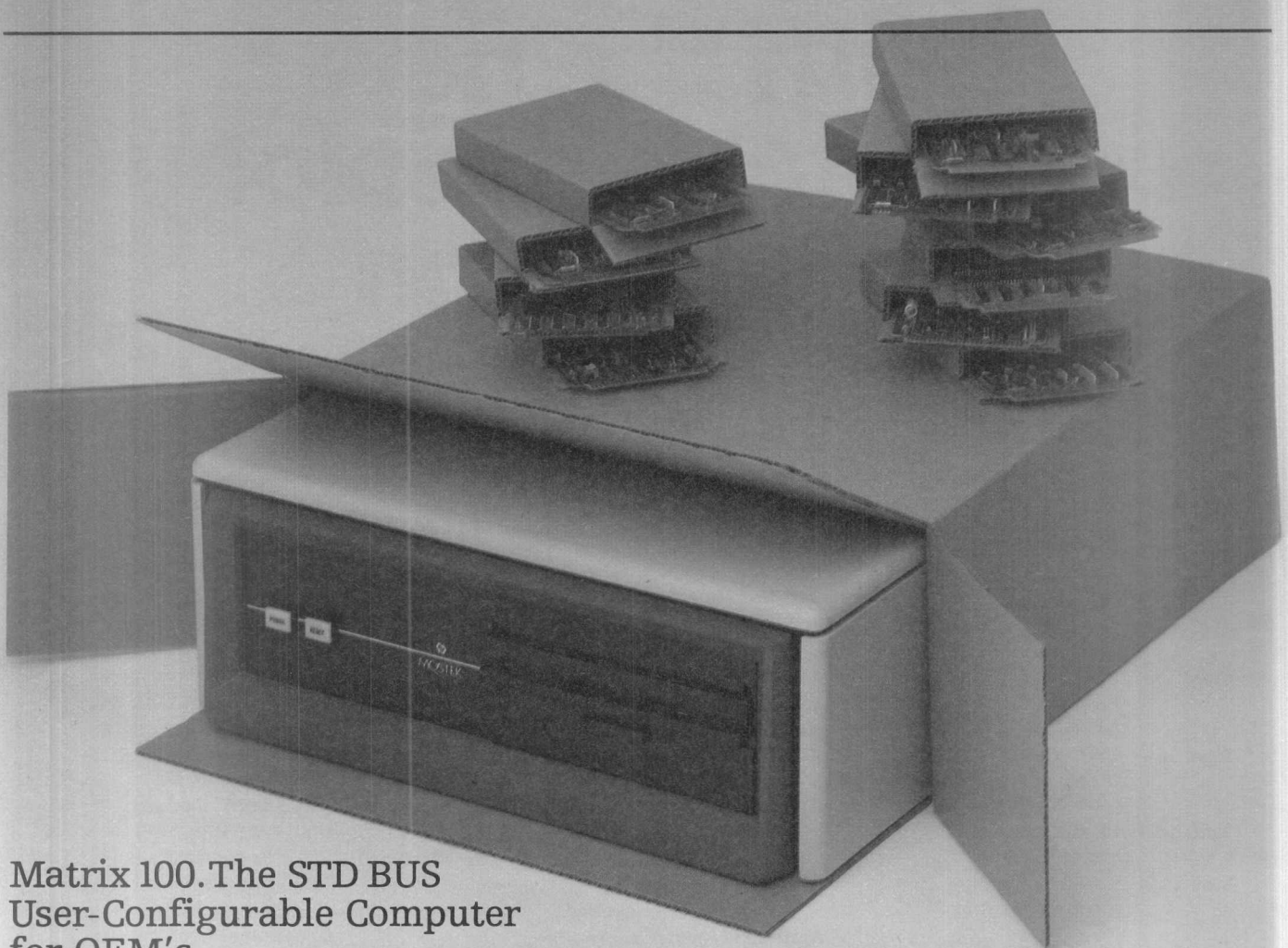
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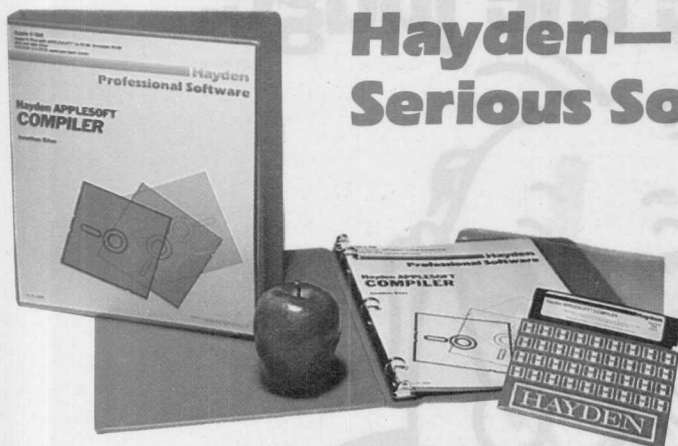
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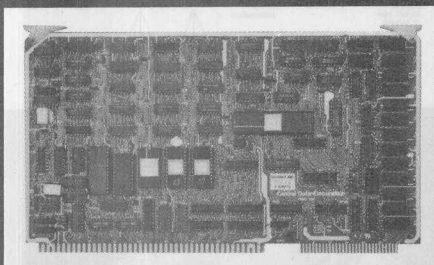
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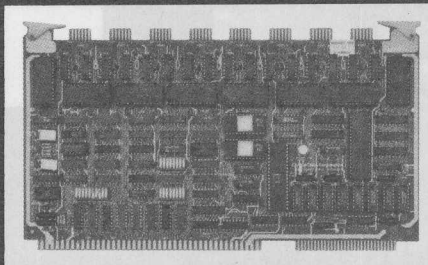
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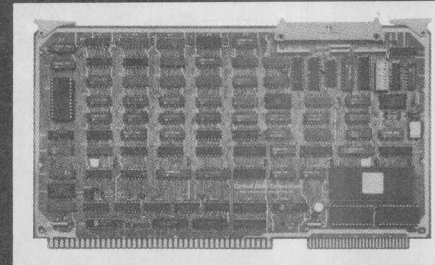
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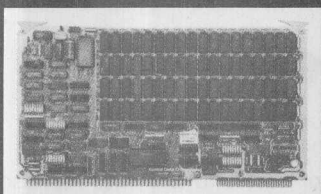
Z8000* Memory Management Processor Board features 4MHz Z8000 running with unique paged/segmented memory management. Includes interrupt controller, interval timers. Can also support PROMs and 9511 APU. Multi-User operating system available. Standard Board \$795
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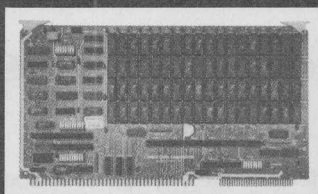
Intelligent Octal I/O Board provides 8: RS-232 ports controlled by on-board 2650 microprocessor. 16K of dual-port RAM allows data transfers with no bus overhead. Includes standard terminal driver program, can hold 4K custom driver program in PROM. \$700.



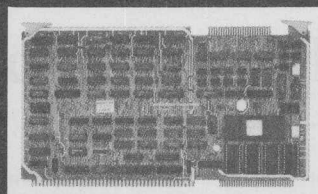
ANSI Winchester Controller fully conforms to the proposed ANSI standard for 8" winchester disk drives. Custom microprogramming available to interface with other disk drive interfaces. Controls up to eight drives. \$550.



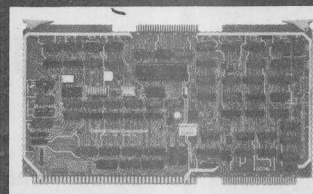
32K-128K Dynamic RAM Board features low power consumption, standard parity checking, and ultra-high reliability.
32K-\$530 96K-\$1080
64K-\$800 128K-\$1350



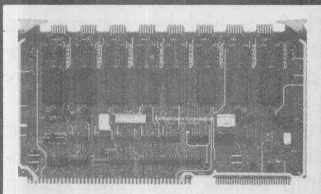
Static Ram Board adds either 16K or 32K of static memory to a Multibus system. 16K — \$620
32K — \$1100



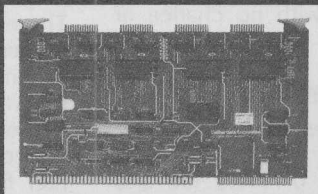
Cartridge Disk Controller Board provides DMA transfers to or from cartridge disk drives with capacities of 10 or 20 Mbytes. \$435



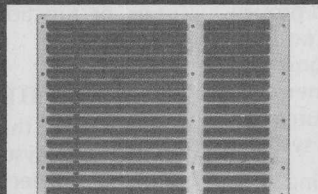
Double Density Floppy Disk Controller adds from one to four double density standard sized floppy disk drives, either single or double-sided. \$315



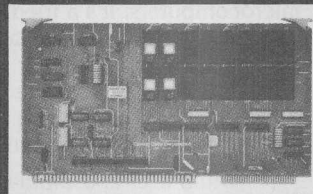
Octal Serial Interface Board allows up to eight EIA RS-232 interfaces. \$330



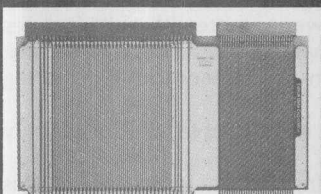
Quad Serial Interface Board hooks up to four EIA RS-232 interfaces to your system. \$280



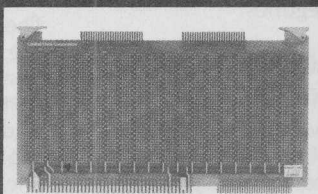
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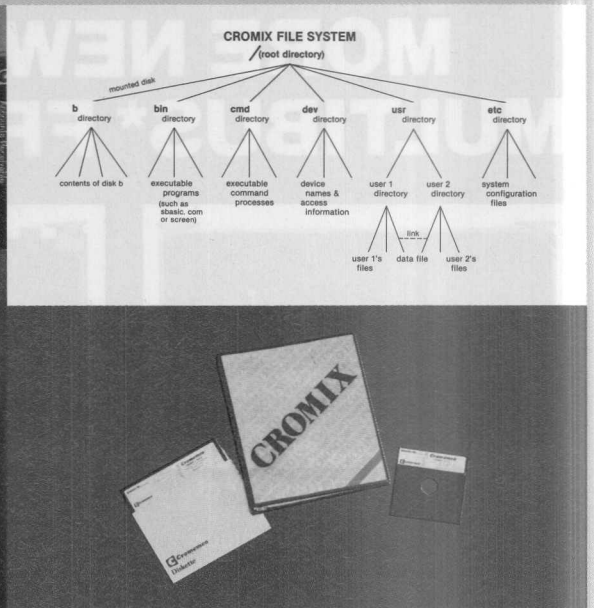
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CROMIX* — Cromemco's outstanding UNIX[†]—like operating system

CROMIX is just the kind of major development you've come to expect from Cromemco. After all, we're already well-known for the most respected software in the microcomputer field.

And now we've come up with the industry's first UNIX-lookalike for microcomputers. It's a tried and proven operating system. It's available on both 5" and 8" diskettes for Cromemco systems with 128K or more of memory.

Here are just some of the features you get in this powerful Cromemco system:

- Multi-user and multi-tasking capability
- Hierarchical directories
- Completely compatible file, device, and interprocess I/O
- Extensive subsystem support

FILE SYSTEM

One of the important features of our CROMIX is its file system comprised of hierarchical directories. It's a tree structure of three types of files: data files,

directories, and device files. File, device, and interprocess I/O are compatible among these file types (input and output may be redirected interchangeably from and to any source or destination).

The tree structure allows different directories to be maintained for different users or functions with no chance of conflict.

PROTECTED FILES

Because of the hierarchical structure of the file system, CROMIX maintains separate ownership of every file and directory. All files can thus be protected from access by other users of the system. In fact, each file is protected by **four separate access privileges** in each of the three user categories.

TREMENDOUS ADDRESS SPACE, FAST ACCESS

The flexible file system and generalized disk structure of CROMIX give a disk address space in excess of one gigabyte per volume — file size is limited only by available disk capacity.

Speed of access to disk files has also been optimized. Average access speeds far surpass any yet implemented on microcomputers.

'C' COMPILER AVAILABLE, TOO

Cromemco offers a wide range of languages that operate under CROMIX. These include a high-level command process language and extensive subsystem support such as COBOL, FORTRAN IV, RATFOR, LISP, and 32K and 16K BASICS.

There is even our highly-acclaimed 'C' compiler which allows a programmer fingertip access to CROMIX system calls.

THE STANDARD O-S FOR THE FUTURE

The power and breadth of its features make CROMIX the standard for the next generation of microcomputer operating systems.

And yet it is available for a surprisingly low \$595.

The thing to do is to get all this capability working for you now. Get in touch with your Cromemco rep today.

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Tomorrow's computers today

Network hardware is key element in connection costs

Host-software burden, sharing, interconnectability, and specialized networking components all must be considered in determining the cost for each network connection.

The most common local-networking rule of thumb is that the cost of adding a work-station should only be a small fraction—say 10% to 20%—of the cost of a stand-alone host. Today's local-area networks easily satisfy that rule, whether the network is a group of small computers with one acting as the net master, a larger number contending for access to a distributed-control bus, or a broadband system designed to connect thousands of users.

The cost per connection hinges on three major considerations:

- Host-software overhead burden determines the work station's cost performance in the sharing mode and is the primary factor in selecting a basic class of LAN: master-slave microcomputer network, low-cost contention bus, general-purpose contention bus, or broadband system.

- Interconnectability, or the number of work stations that can share resources concurrently, determines how much the user can afford to spend on resources such as hard-disk drives, versus using stand-alone computers with their own peripherals.

- The cost of specialized networking components can be averaged over the number of network nodes. These include the master station and the required support in slave stations on a master-slave network, the distributed-control interfaces in a contention or a token-passing system, the costs of frequency multiplexing and channel switching in a broadband system, and the cost of the transmission medium.

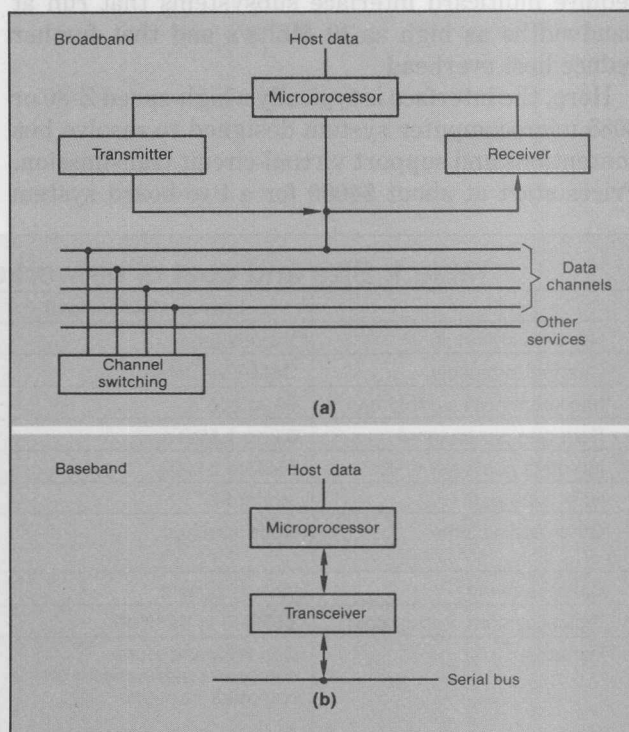
Process-control, military, and other high-reliability networks may require redundant paths, which drive up interconnect hardware and media costs. Also, the need for master command and control prevents full distribution of system control.

The great majority of small computer networks

packaged by OEMs today are hierarchical. Two representative strategies for keeping host overhead down during network growth are to expand a master-slave microcomputer network's bus resources or to expand a star by adding microcomputer-based terminal clusters at the outlying nodes.

The bus approach offers high-speed access to shared disk storage. For three or four slaves to access storage, 128 kbytes of RAM are added to the master. More slaves call for a second CPU, then buffer memory in the disk controller and each microcomputer. As the network grows to 32 users—its limit—the effective cost per connection drops from under \$1000 to under \$500. The star approach competes by using serial links and satellite CPUs with 64-kbyte RAMs to unburden the original CPU. A basic three-CPU star can support 16 users.

Contention systems also grow incrementally in cost. Those designed to connect up to 64 stations



1. Broadband bus systems (a) require multiplexing and channel switching to grow beyond a simple baseband bus (b).

generally have an interface cost of \$500 or less (Table 1), whereas those designed to link up to 256 have interface costs up to around \$1000. Each host's overhead is moderate because distributed control allows each to communicate with the resources.

As the number of users grows, the interconnection costs grow in proportion until they add up to more than the total cost of the microcomputers on a master-slave network. However, large, costly resources can be shared by many more work stations to lower the average cost per user. The resources of these networks range up to mainframe computer systems. The mainframe acts as a data-base server to the microcomputers, and the microcomputers minimize the mainframe's time-sharing and front-end communications-processing load.

These systems cannot operate at high data rates, because each host (or server) has to handle higher-level communications tasks with software. So the bus-interface units (BIUs, also called CIUs, or communications interface units) can be built with standard, low-cost LSI chips, such as serial I/O circuits and single-chip microprocessors, accounting for the low cost involved in such systems.

Mid-range contention

The next cost break comes in systems, such as Net/One and Ethernet, designed to handle hundreds of office computers, terminal clusters, large disk storage systems, laser printers, and even mainframes. They require multicard interface subsystems that run at bandwidths as high as 10 Mbits/s and that further reduce host overhead.

Here, the interface is typically a high-speed Z-80 or 8085 microcomputer system designed to resolve bus contentions and support virtual-circuit transmission. Prices start at about \$4000 for a two-board system

with a computer-bus port, plus \$500 per transceiver card, and range to over \$10,000 for a multiport system with a multiprocessor, user-programmable microcomputer system. The basic Ethernet controller for Multibus-based systems is a \$4000 8085 system, for example. OEMs can minimize host overhead by storing iLNA software modules as firmware, but that also increases the cost per connection.

But again, the rules of thumb hold true. For example, the first Ethernet-compatible product, the Xerox 8010 Star multifunction office computer, costs \$16,595 in a basic configuration, compared with around \$3000 for a low-cost net's personal computers and about \$1000 for a cluster's CRT terminals.

The cost of mid-range interfaces will drop as VLSI begins to replace the microcomputer systems. The target is to compete with office telephone systems (\$600 to \$1100 per line) between 1985 and 1990. Meanwhile, the low-cost systems have made "LAN" an office if not a household word.

At the high end of the common-bus range are high-performance channels designed to connect a relatively small number of mainframes and large memory systems. They cost well above \$10,000 per connection because they are built with emitter-coupled logic (ECL). But the shared resources are far more costly and until recently were I/O-limited.

Broadband systems

Broadband bus networks compete with linear systems across much of the applications range and are also competitive with PBX systems. Like other LANs, they require an intelligent interface. They also require some form of frequency multiplexing and channel switching to grow beyond a simple baseband bus (Fig. 1)

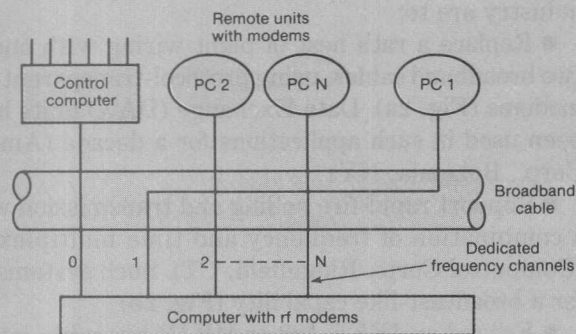
In these systems, computers are connected through

Table 1. Size and cost of networks with contention-access channels

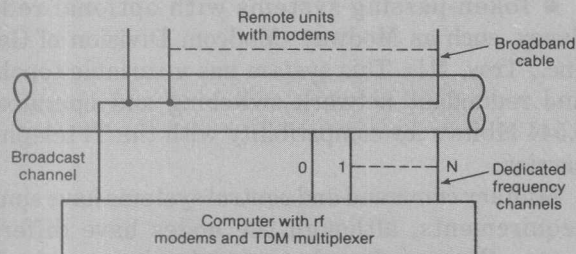
	Low-cost linear bus	Midrange linear bus	Broadband bus system
No. data channels	1 (baseband)	1 (baseband)	2 to over 256
Channel protocols	CSMA or CSMA/CD	CSMA/CD	CSMA/CD or modem
Maximum nodes per channel	64 to 256	256 to 1024	2 to over 256
Data rate per channel	0.2 to 1 Mbit/s	2 to 10 Mbits/s	9.6 baud to 12 Mbits/s
Interface costs per node	\$500 to \$1000	\$5000 to \$10,000 *	\$1,000 to \$10,000 *
Host overhead	Moderate	Low	High to low
Other subsystems	None required	Repeaters or bridges for maximum size	Frequency and channel switching
Cable required	Wire or coaxial	Low-loss coaxial	Cable television
Typical system startup cost	\$10,000 to \$25,000	\$25,000 to \$50,000	\$25,000 to over \$100,000
Remarks †	Can be stand-alone microcomputer network or computer front end	Can be stand-alone microcomputer network or include mainframes and terminal clusters	Can also include dedicated computer and terminal channels and voice and video channels

* High-end interfaces are multiport subsystems; \$1000 is typical price for terminal modem for broadband system.

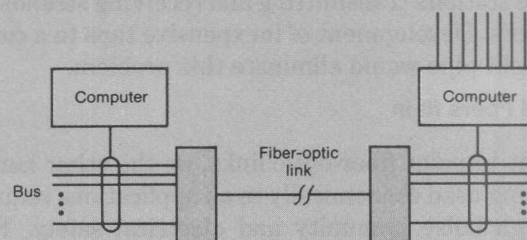
† Minimum startup system in all three cases is two work stations and a shared disk drive.



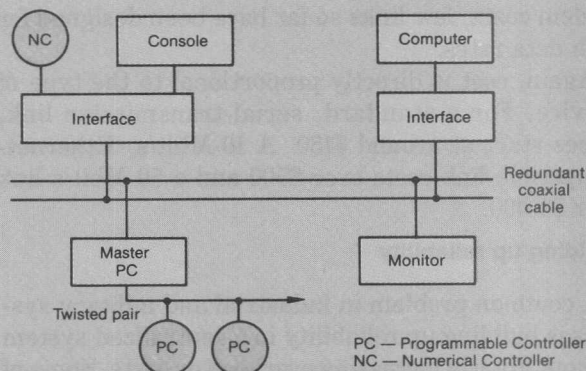
(a) Channels replace wires



(b) Broadcast channel added



(c) Extended IEEE-488 bus



(d) Token-passing bus

2. Industrial networks are being built with broadband cables (a), with additional broadcast channels (b), with extensions of the basic IEEE-488 bus (c), and with token-passing systems (d).

multiport bus interfaces costing about the same as mid-range contention-bus units (about \$4000 to \$10,000, depending on packet-channel bandwidths). However, RS-232-C serial inputs can be interfaced with a channel for about \$1000 using an intelligent modem (Fig. 2).

Thus terminals, microcomputers, and large computers all can be connected economically to the same broadband cable. The drawback in small systems is a high startup cost—to share the costs, there must be enough users to share the channel high/low-frequency converters and channel switchers. LocalNet keeps these costs fairly incremental with expandable subsystems whereas WangNet assumes that the system will start up with numerous users. Its component breakdown is:

- \$850 per 9.6-kbaud port and \$1200 per 64-kbaud port on dedicated serial channels (total of 48 channels)
- \$1250 for the 9.6-kbaud ports on 256 switched point-to-point channels, plus a \$12,000 switch for each system
- \$3800 per interface with a wideband, contention channel using CSMA/CD and proprietary protocols
- User-supplied equipment on the video band.

These facilities use only one-third of the bandwidth of cable television (CATV) cable, yet allow the system to grow to over 65,000 users.

The largest portion of the cost of the transmission medium are for installation and fittings. In an old building, installation is comparable to electrical rewiring, so the costs are high regardless of the medium. In a new one, the owner and architect make a de facto decision on the type of LAN to use in the future. Today, the canny architect puts in coaxial cable and may hedge the future by equipping the new building with fiber-optic cable while it is still economical to do so. Smart OEMs also look ahead. IBM, for one, designed its 8100 business loops to use spare power circuits and encouraged users to put complete spare wiring systems in new buildings.

The media matches

Except for fiber-optic cable, the choice of medium is fairly routine today. Because twisted-pair and standard coaxial cable can carry all the traffic of low-cost systems with bandwidth to spare, they are usually specified by the LAN vendors. Low-loss coaxial baseband or CATV cable, connectors, and taps are very rigidly specified for high-capacity systems and the highest-performance commercial systems use multiple triaxial cables.

Although several experimental fiber-optic bus systems are in operation today at university computing centers and research laboratories, the buses are very

Systems & Software: LAN hardware

expensive to build. Optical mixers are needed to couple one station's transmitting and receiving strands to another's. Development of inexpensive taps to a common light pipe would eliminate this problem.

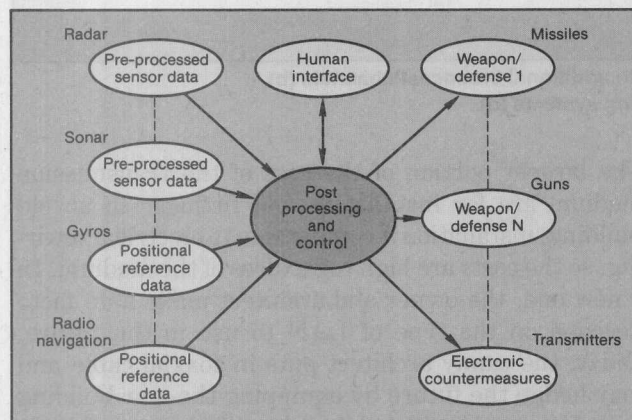
Optical fibers fit in

Point-to-point fiber-optic links, on the other hand, are being used economically in all applications requiring high noise immunity and electrical safety. For instance, plastic optical cable and inexpensive modems are widely used with noisy equipment that would ordinarily be connected by twisted pairs. To save modem costs, few links so far have been designed for high data rates.

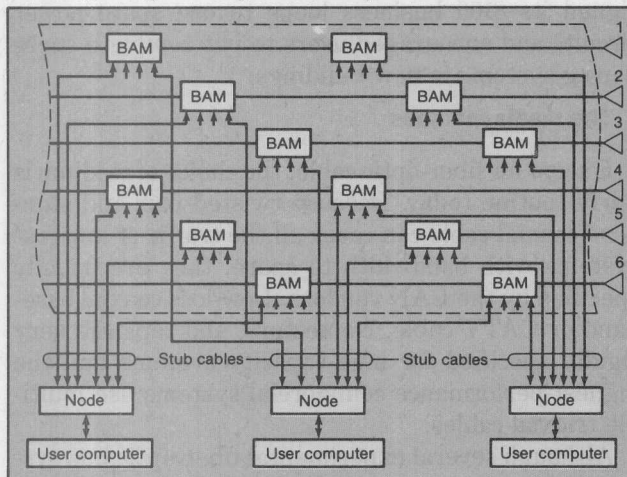
Again, cost is directly proportional to the type of service. For a standard, serial-transmission link, prices start at around \$150. A 10-Mbit/s, Ethernet-compatible link costs over \$500 and a 50-Mbit/s link over \$3,000.

Building up reliability

A common problem in industrial and military systems is building up reliability in a centralized system without greatly increasing overhead or costs. Some of



3. Military networks handle a wide variety of functions, covering navigation signals to weapons control.



4. The Shinpads system uses bus-access modules (BAMs), transformer-coupled, passive taps that attach to four nodes.

the basic approaches that are presently being used in industry are to:

- Replace a rat's nest of plant wiring with one or two broadband cables, using protocol-transparent RF modems (Fig. 2a). Data Exchange (DAX) units have been used in such applications for a decade (Amdax Corp., Bohemia, NY)

- Support rapid-fire polling and transmission with a combination of frequency and time multiplexing (Computrol Corp., Ridgefield, CT). Such systems offer a broadcast-like capability (Fig. 2b)

- Extend an IEEE-488 or HP-IB bus with optical links (Hewlett-Packard, Palo Alto, CA). The standard allows for multicomputer systems and pass-control functions (Fig. 2c)

- Token-passing systems with optional redundancy, such as Modway (Modcom Division of Gould Inc., Troy, MI). This system has a variable topology and redundant network switching and operates at 1.544 Mbits/s for compatibility with the T1 telephone carrier.

Military command and control systems have similar requirements, although the nodes have different names. Some are based on coaxial switches—the AN/USQ-67 is a $2 \times 640 \times 640$ matrix with a data rate of 25 Mbits/s per connection (Fig. 3). Recently, the Canadian Department of National Defense sponsored development of the first bus system for major military systems, the AN/UYC-501(V) Shinpads (Shipboard Integrated Processing and Display system).

Sperry Corp., the developer, plans to make the bus access modules commercially available. The BAMs are transformer-coupled, passive taps that attach to four nodes. The military system uses the BAMs in a highly redundant, 10-Mbit/s triaxial cable system (Fig. 4). In a commercial system, only one BAM per node is needed to handle separate control and data paths (Sperry Univac Defense Systems Division, St. Paul, MN).

Solving future problems

Local packet-switching networks can provide access to remote facilities through standard telephone interface hardware, but the work stations can access the public packet-switching networks only through large host computers equipped with X.25 front-end processors.

Since the public packet networks are widely used for advanced distributed-processing information exchange, LAN vendors are searching for ways around this problem. One solution that will soon be used on Net/One is the C Machine (BBN Computer Corp., Cambridge, MA). This system can interface local packet-switching systems, public networks requiring X.25 interfaces, and the Arpanet as a node on a local network. □

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EXHIBIT A:

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EXHIBIT B:

VAX 11/780 256 KB add-in memory

Monolithic Systems MSC 3610 is a direct replacement for the DEC M8210 VAX memory. The 256KB system is designed to provide maximum heat dissipation and thus extend memory life.

EXHIBIT C:

PDP 11/70 256KB add-in memory

The MSC 3611 is designed for DEC's MK11 semiconductor system and maintains full diagnostic and ECC compatibility.

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EXHIBIT D:

PDP 11/70 256KB to 2MB, add-on ECC memory

The MSC 3602 is extremely fast, has an MTBF in excess of 40,000 hours and contains the most powerful set of on-board diagnostics in the industry. The rugged, modular design allows easy maintenance, low cost spares and extremely low MTTR. On-site repair contracts are available after the standard one year warranty.

EXHIBIT E:

VAX 11/750 256KB add-in memory

The MSC 3612 is a compatible replacement for the M8728 DEC memory with a 32Kx72 bit configuration.

IN CONCLUSION:

Monolithic Systems provides the features and services OEM's value. All memory elements are socketed, all products carry a full one year warranty and delivery is less than 30 days for quantities under 25. Refer to the chart below for the Monolithic Systems product that suits your particular computer's need.

*DEC, VAX, LSI-11, PDP-11/70 are registered trademarks of Digital Equipment Corporation.

MSC MODEL NUMBER	LSI-11	LSI-11/2	LSI-11/23	VAX 11/780	VAX 11/750	PDP-11/70	PDP-11/04	PDP-11/05	PDP-11/10	PDP-11/30	PDP-11/34	PDP-11/35	PDP-11/40	PDP-11/44	PDP-11/45	PDP-11/50	PDP-11/55	PDP-11/60	DATA SYSTEM 330	DATA SYSTEM 350	DATA SYSTEM 570	NEAREST * DEC MEMORY EQUIVALENT
3602					X														X			MK11-
3605						X	X	X	X	X	X	X		X	X	X	X	X				NONE
3606						X				X							X					MS11-L
3607					X	X	X	X	X	X	X	X		X	X	X	X	X	X	X		NONE
3608					X	X	X	X	X	X	X	X		X	X	X	X	X	X	X		NONE
3610			X																			MS780
3611					X															X		MK11-
3612				X																		MS750
3901					X															X		NONE
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4804		X	X															X				MSVII
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Design

With twice the storage capacity of competitive UV-erasable programmable ROMs, this 16-kword \times 8-bit memory features low power, fast access, three-state outputs, and a single 5-V supply.

X-cell architecture packs 128 kbits onto EPROM chip

With an innovative memory-cell architecture called X-cell, Texas Instrument's TMS2528 becomes the highest density UV-erasable memory device available. It packs twice the storage capacity of conventional EPROMs—over 128 kbits on a single chip.

Organized into a 16-kword \times 8-bit configuration, the fully static, nonvolatile unit comes in a 28-pin DIP (Fig. 1) and features a slew of enhanced performance capabilities:

- The lowest per-bit power dissipation of any EPROM—3.05 μ W/bit

- A power-down mode that reduces total standby power to only about 100 mW

- A fast access time of 250 ns (maximum) between valid address inputs, found only in much smaller EPROMs. (A conventional 64-kbit memory accesses in about 450 ns.)

- Operation from a single 5-V supply in the read mode

- Three-state data outputs, which simplify device paralleling and bus interfacing.

The special X-cell architecture reduces the memory-array area by 40% of that of more conventional designs so that the chip occupies just 42 kmils², slightly more than competitive chips having half the storage capacity. And the 3- μ m layout rules of the 2528's geometry allow word and bit

lines to run much closer than in conventional EPROMs. Naturally, the success of the X-cell architecture and dense layout augers well for making the 2528 the forerunner of a second-generation EPROM that will double the storage capacity to 256 kbits in the near future.

Fabricated with n-channel silicon-gate transistors (see "The 2528 EPROM Transistor Structure"), the device interfaces readily with both MOS and bipolar support circuits. All inputs—including programmed-data inputs—can be applied with TTL logic without external pull-up resistors. And each three-state output can drive a single TTL load, also without the need for external resistors.

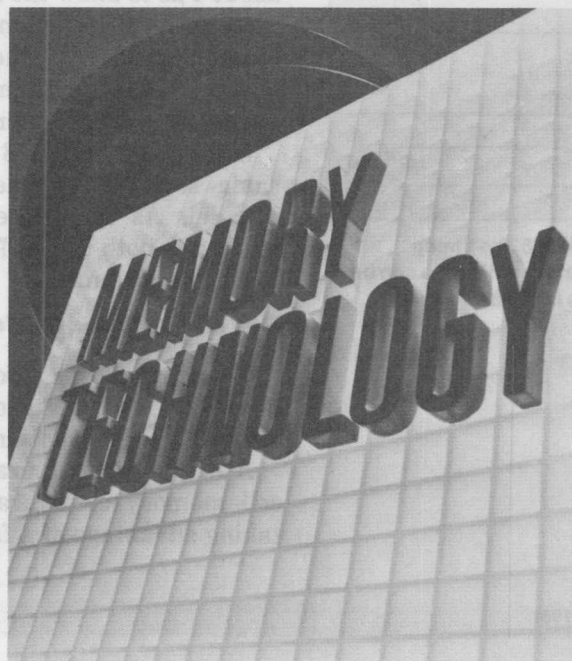
They're easy to use

The three-state data outputs allow several 2528s to be connected directly to a common system bus. Taken together with its static design, the 2528 is extremely easy to address and read, or to program. The read-access timing is simple (Fig. 2). The time from the \overline{CS} (CHIP SELECT) signal to valid-data output

$t_a(S)$, with the address established is just 120 ns (max). The time required between valid-address inputs $t_a(A)$ is 250 ns maximum. And when several 2528 units operate together, the minimum time between \overline{CS} selections $t_p(XZ)$ (the so-called float state) is 100 ns, and almost no time, $t_p(VX)$, is needed between the end of an address and the availability of valid data.

Because of the three-state outputs, when two or more 2528's are connected in common on a single bus, the

Joe Neal, Section Manager of Nonvolatile Memories
Dave McElroy, Branch Manager of Nonvolatile Memories
Texas Instruments Inc.
4000 Greenbriar Drive
Stafford, TX 77477



Memory Technology: 128-kbit EPROM

output of any single EPROM can be read without interference from the others. Low TTL logic signals on both the PD/PGM and \overline{CS} terminals of the selected 2528 enables it; all the other 2528s must be disabled with high logic signals to either the PD/PGM or \overline{CS} terminal. The output data appears on the terminals Q_1 through Q_8 .

A power-down mode for conserving system power by over 80% is entered when a high level is applied to the PD/PGM terminal. In this mode, all outputs present a high-impedance, and the 5-V supply cur-

rent drops to about 15 mA (typically), 30 mA (maximum); thereby, only about 100 mW is consumed. Under normal operating conditions, the chip draws approximately 80 mA and consumes about 400 mW. Current to the 21-V terminal for programming is a maximum of 30 mA.

Programming requires 21-V supply

To program data, the 2528 requires a 21-V power supply to its V_{pp} terminal (which is a few volts lower than the 25 V generally required by the conventional smaller-memory-capacity EPROMs). A single TTL-level pulse per memory location deposits a logic ZERO. Any existing EPROM programming equipment can be used.

However, the programming voltage (V_{pp}) should not exceed 21 V, because higher voltages can punch-through and damage the device. This poses a minor problem, because conventional EPROMs normally withstand 25 V; therefore, most electrical programmers use this higher voltage. Thus, when programming a 2528, a voltage divider must be inserted between the programming unit and the V_{pp} pin on the memory chip to reduce the voltage level to the 21-V level.

Prior to programming, the 2528 must be erased by exposing it to high-intensity (15 W-s/cm²) ultraviolet (UV) light ($\lambda = 2537$ Angstroms). Light enters through a transparent lid on top of the chip. For most applications, the typical 12 mW/cm² filterless UV lamp will erase the device in about 21 minutes when placed about 1 in. above the chip. After erasure, all memory bits are in a high (logic ONE) state.

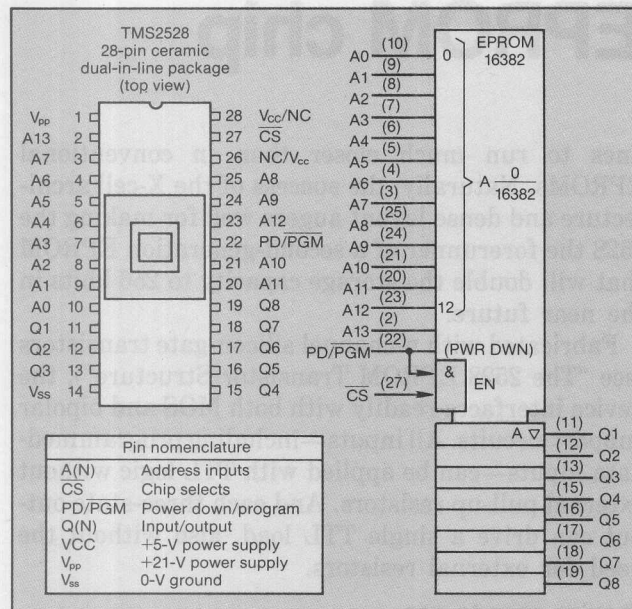
Programming consists of entering logic ZEROS in the desired locations. The programming input data are presented in parallel on pins Q_1 through Q_8 (which become the output pins in the read mode). After about 4 μ s to allow the address and data to stabilize, a 50-ms (typical), 55-ms (maximum) low-level TTL pulse is applied to the PD/PGM terminal for each address location. Memory locations can be programmed in any order, singly or in blocks.

More than one 2528 can be programmed in the same setup when the devices are connected in parallel. As in the read mode, low-level signals applied to both the PD/PGM and \overline{CS} pin select the unit to be programmed.

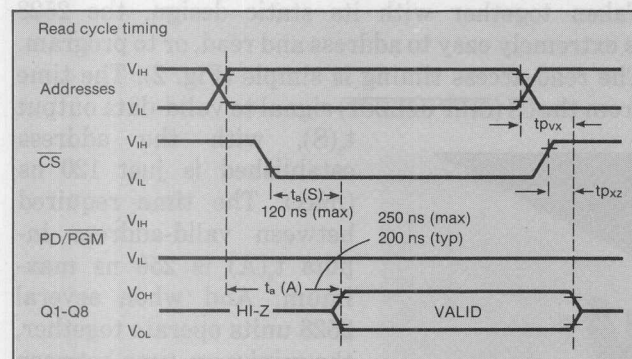
The architecture is different

To achieve this programming and application simplicity, the 2528 requires an architecture unlike that of any conventional EPROM.

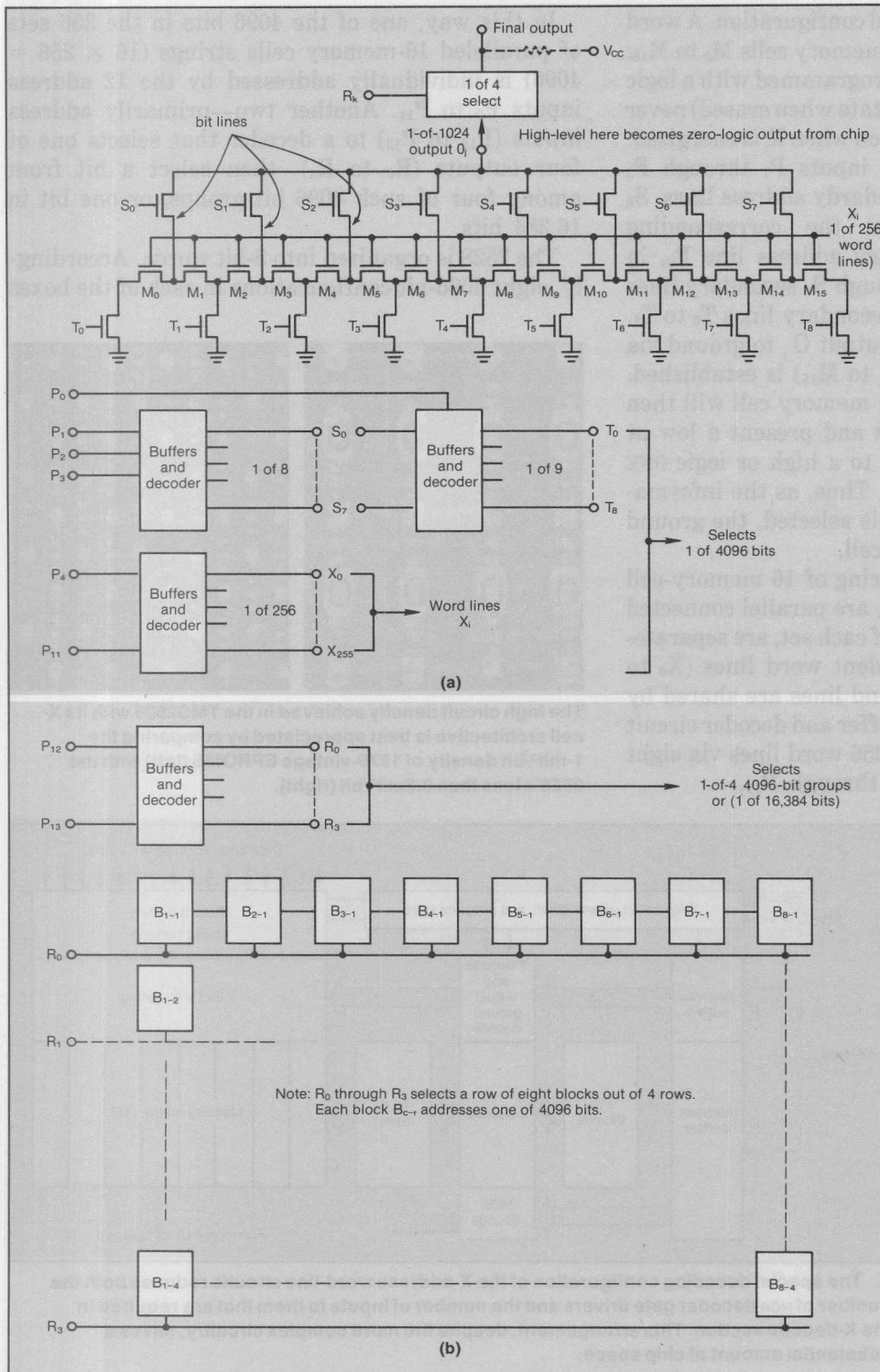
A major architectural innovation is the chip's X-cell memory configuration (Fig.3a), which allows taking advantage of a faster and less space-consum-



1. The simplicity of the TMS2528 EPROM's I/O and control requirements allows housing the memory in just a 28-pin DIP, despite the unit's 128-kbit capacity.



2. Simplicity is reflected also in the TMS2528's timing diagram. About 120-ns must elapse before valid data can be read after a \overline{CS} signal, and about 250 ns is needed after an address change.



3. The TMS2528's virtual-ground parallel-addressing scheme (a) saves hardware and space, and therefore the decoders for the secondary address lines S, T, and R can fit into a central location among the memory cells arranged in blocks of 4096 bits each (b).

Memory Technology: 128-kbit EPROM

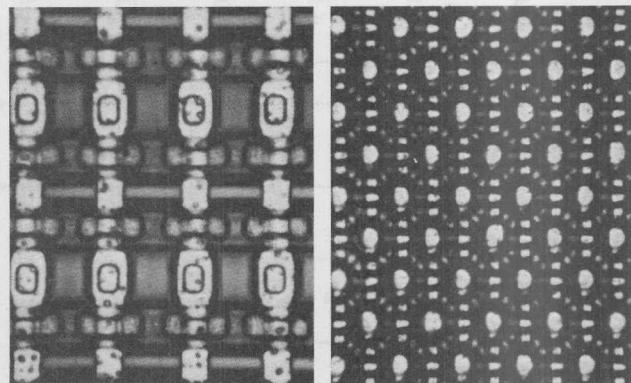
ing virtual, or floating, ground configuration. A word line X_i enables a string of 16 memory cells M_0 to M_{15} . Memory cells that had been programmed with a logic ZERO (they are in a logic ONE state when erased) never turn on; all the others do turn on when X_i is energized.

A primary set of address inputs P_1 through P_3 selects one out of eight secondarily address lines, S_0 through S_7 and turns on the corresponding transistors. A fourth primary address line P_0 , in combination with the S_0 through S_7 secondary lines select one of another set of secondary lines T_0 to T_8 . In this way, the path from output O_j to ground via one of the memory cells (M_0 to M_{15}) is established. An unprogrammed logic ONE memory cell will then complete the path to ground and present a low at output O_j (which is inverted to a high or logic ONE at the chip output terminal). Thus, as the information from each memory cell is selected, the ground moves (floats) from cell to cell.

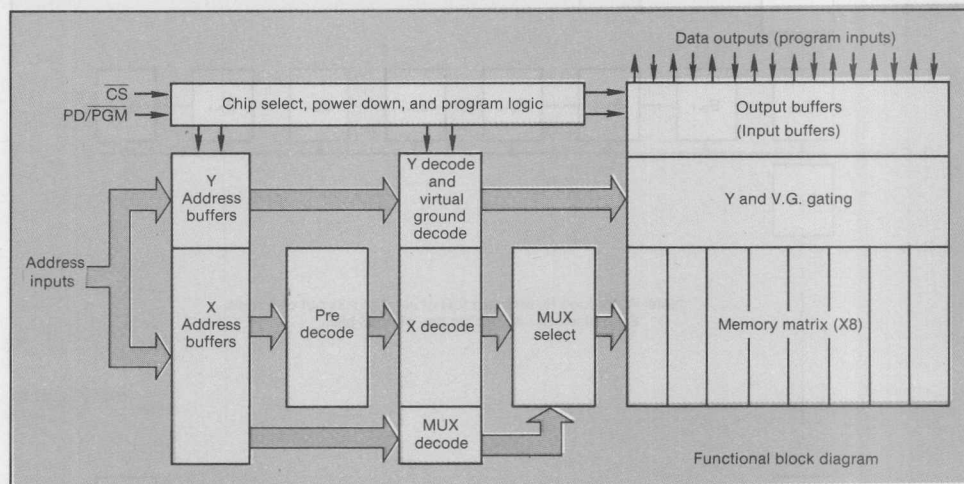
Further, 256 sets of the string of 16 memory-cell transistors, shown in Fig. 3a, are parallel connected—source to drain. The gates of each set, are separately connected to 256 independent word lines (X_0 to X_{255}), but the S, T, and ground lines are shared by all the 256 sets. A separate buffer and decoder circuit energizes one of each of the 256 word lines via eight primary address inputs, P_4 through P_{11} .

In this way, one of the 4096 bits in the 256 sets of paralleled 16-memory cells strings ($16 \times 256 = 4096$) is individually addressed by the 12 address inputs P_0 to P_{11} . Another two—primarily address inputs (P_{12} to P_{13}) to a decoder that selects one of four outputs (R_0 to R_3)—then select a bit from among four of such 4096 bit groups, or one bit in 16,384 bits.

The 2528 is organized into 8-bit words. Accordingly, eight 4096-bit configurations in each of the boxes



The high circuit density achieved in the TMS2528 with its X-cell architecture is best appreciated by comparing the 1-mil²/bit density of 1976-vintage EPROMS (left) with the 2528's less than 0.2mil²/bit (right).



4. The special decoding configuration of the X-address word-line circuits reduces both the number of NOR decoder gate drivers and the number of inputs to them that are required in the X-decode section. This arrangement, despite the more complex circuitry, saves a substantial amount of chip space.

of the matrix B_{c-r} (from B_{1-1} to B_{8-4}) in Fig. 3b are all addressed in parallel by the first twelve primary address inputs P_0 to P_{11} . And, the next two primary inputs P_{12} to P_{13} select only one of the four box rows via the four decoded secondary-address lines R_0 to R_3 . The result? One 16,384 8-bit word is formed for each unique 14-bit input address, P_0 to P_{13} .

This decode scheme could be implemented as is done in many in a conventional memory designs with large numbers of series transistors, which not only occupy more space, but also take more time to access. The parallel-activation of the memory cell transistors and efficient decoding arrangement ensure high-speed operation.

Address split between word and bit lines

The block diagram in Fig. 4 shows the overall organization of the 2528's addressing and control circuitry. Note that the address inputs are split between the X, or word-line, address buffers consisting of the eight primary-address inputs P_4 to P_{11} in Fig. 3a and the Y, or bit-line address buffers (stemming from the rest of the six primary inputs, P_0 to P_3 and P_{12} to P_{13}), which provide the virtual-ground selections via the S, T, and R secondary address lines. What is not apparent from the block diagram is another important architectural innovation that saves hardware.

The conventional approach for obtaining the 256 word lines would involve 256 decoding (NOR) gates (in the X-decode section) with eight inputs each. However, the special precode X-decode mux-select configuration reduces the NOR-gate count to a fourth, or 64 gates, with just four inputs each. The overall effect is a reduction from 2048 to 300 of the number of transistors required. This arrangement then needs about half the area used by other EPROMs for the same function.

Word-line decoder in chip's center

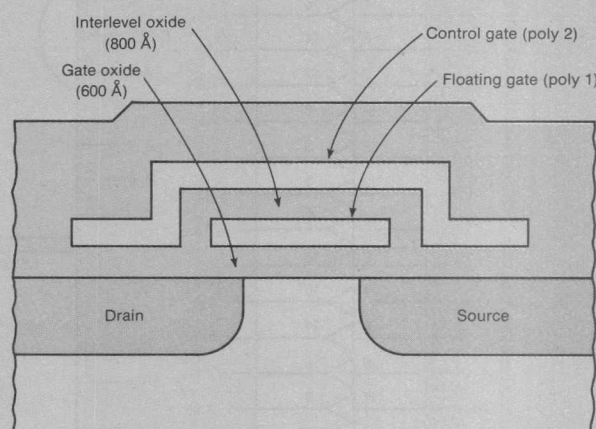
More important, however, the word-line addressing decoder becomes small enough to be placed in the center of the chip, which reduces the average distance, and thus the delay time to the word lines. In addition, with a centrally located decoder, the word-line delay path goes through fewer buffers than needed with the circuitry on the chip's periphery. The result? The 2528 is almost twice as fast as most available 64-kbit EPROMs, even though the 2528 has twice the storage capacity.

Not to be overlooked is that the 2528's virtual-ground scheme enters the power-down mode with a low-level logic signal on the X_i word lines, where conventional devices must be powered-down with a high-level signal. Then, in the 2528, only the selected X_i line draws current on power-up; in the conven-

The 2528 EPROM transistor structure

In addition to improved overall architecture, the 2528 incorporates advanced MOS techniques at the transistor-structure level—source-drain-channel doping with arsenic (instead of with the usual phosphorus), thin gate oxides, and thin interlevel oxides (see figure). With arsenic, the transistor's source-drain channel can be made shorter and thus faster responding. On top of that, the channel also has less capacitance. The result? Despite parallel word lines, they offer low propagation delays.

Moreover, the transistor's thin-gate oxide—about 600 Å compared to the usual 800 Å—also contributes to the higher speed capability. Also, the thin interlevel

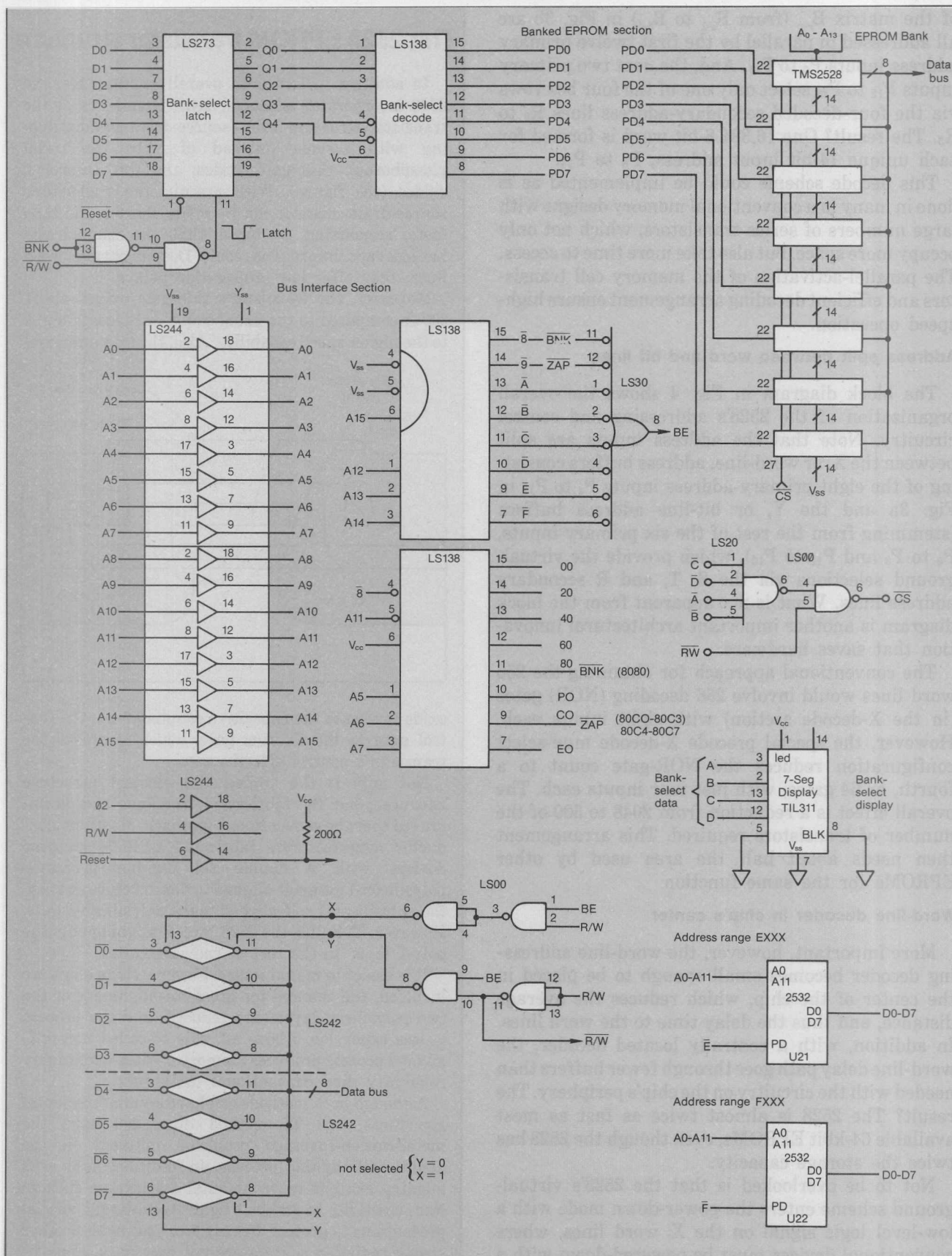


oxide increases the capacitive coupling from the control gate to the floating gate, which improves the transistor's control effectiveness.

Not only is the doping and element structure advanced, but the fabrication technique also is improved over the conventional approach. Most semiconductor manufacturers fabricated EPROM memory devices with a double self-aligning process—polysilicon-1 gate self-aligned to the structure and also the polysilicon-1 self-aligned to the polysilicon-2 gate. However, TI builds the 2528 by self-aligning only the poly-1 layer to the rest of the structure.

It is easier to manufacture: Fewer etching steps are involved, the chances for gross misalignment of the two polysilicon layers are reduced, and the process is less expensive. Above all, this so-called non-self-aligning process produces memory devices with higher reliability than conventional techniques.

Although both methods can handle small elemental structures, the TI method does not have the metallization-coverage problems inherent in the double self-aligning process. In addition, none self-aligning exhibits environmental advantages such as less sensitivity to ambient light. Accordingly, special precautions to protect the chip from sunlight or other strong radiation sources are not necessary. Conventional EPROMs often require an opaque covering.



5. A bank of eight TMS2528 EPROMs can hold 128 kbytes of firmware, which formerly required expensive, bulky and slow disk or tape devices to handle.

tional unit, all draw power except the selected line. Thus, the power-supply and other substrate lines are less disturbed when the 2528 is brought out of the power-down mode.

EPROM bank holds system firmware

But that's not all. It's easy to put together a bank of 2528 EPROM memories that can hold a large amount of firmware. To do so formerly required bulky and expensive moving magnetic-media devices (discs, or tapes). A bank of eight 16-byte TMS2528s provides a formidable 128-kbyte of on-line software.

Of the eight 2528 units in Fig. 5 wired with their address and data buses and \overline{CS} terminals in parallel, only one 2528 in the bank is selected with a low-level logic signal to its PD/PGM terminal selection is by signals designated PD₀ through PD₇ in the figure, from a 74LS138 bank selected decode output. All nonselected 2528's (with PDs high) remain in the low-power standby mode. The whole bank of eight 2528s is selected by a low logic signal to the parallel \overline{CS} terminals.

Loaded from the system bus via terminals D₀ through D₇, a 74LS273 bank-select latch feeds a 74LS138 bank-select decoder. The bank-select latch clears when it receives a system-reset signal to its reset terminal, and selects bank 0 (PD₀) when this occurs.

A 7-segment display driver (the bank-select display), connected to the four least-significant bits of the bank-select latch, provides a readout of the current bank value.

Two 74LS244 chips provide buffers to interface the A₀ to A₁₃ address inputs of the memory chips and the control lines, and 74LS242 bidirectional data-bus buffers interface the memory data lines Q₀ to Q₈. A 74LS138 decodes the high-level address-space (A₁₂ to A₁₅) into 4-kbyte blocks. And a 74LS30 AND gate combines the 74LS183 block-selection outputs into a broad-enable (BE) signal. Finally, another 74LS138 selects the desired bank-select latch and other I/O functions in the system.

When BE goes high, one of the system's EPROMs has been addressed. And BE combined with an R/W signal sets the proper data direction in the bidirectional data buffers. Responsible for system initiation and other control functions, two extra EPROMs—not part of the bank—occupy some of the input address space and are turned on by outputs from one of the 74LS138 decoders.□

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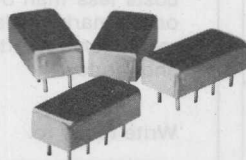


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				DC-1000	1000-1500	DC- 1000-1000	1000 1500	
AT-3	3	± 0.2 dB	DC-1500	0.6dB	1.0dB	1.3:1	1.5:1	1W
AT-6	6	± 0.3 dB	DC-1500	0.6dB	0.8dB	1.3:1	1.5:1	1W
AT-10	10	± 0.3 dB	DC-1500	0.6dB	0.8dB	1.3:1	1.5:1	1W
AT-20	20	± 0.3 dB	DC-1500	0.6dB	0.8dB	1.3:1	1.5:1	1W



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SMOS and circuit design speed up, power down static RAM

Backed by high-speed scaled-NMOS (SMOS) technology, Texas Instruments' new static RAM, the TMS2149, boasts the top speed-power product performance of any currently available 1-k \times 4 device. The 2149 fits a growing number of applications for fast SRAMs on the ever-changing computer-architecture scene.

In addition to the contributions of processing, much of the chip's improved performance rests with an innovative circuit-design technique called column sensing. Here, a differential amplifier is allocated to each of the memory-array columns, and control logic selectively activates a specific amplifier to obtain data from the chip. The advantage of differential amplifiers over conventional SRAM designs is that bit-line loading is reduced significantly. Moreover, instead of relying on small, passive column and row gates, column sensing designs use active-mode amplifiers to achieve much greater drive capability than conventional memory devices (Fig. 1).

As proof of the benefits of SMOS and column sensing, the 4-k device (1024 words \times 4 bits) offers a worst-case access time from address inputs (t_a (A)) of 35 ns, and an access time from chip select (t_a (S)) of just 15 ns. Coupled with a worst-case power dissipation of 660 mW, the 2149 becomes one of the top contenders for high-speed memory systems such as cache, fast buffers, scratchpad and writable control

store. On another front, trends in real-time-data-acquisition system development have created applications for memory devices that operate at cycle-times below 70 ns. For the 2149, both read and write cycle times are specified at 35 ns.

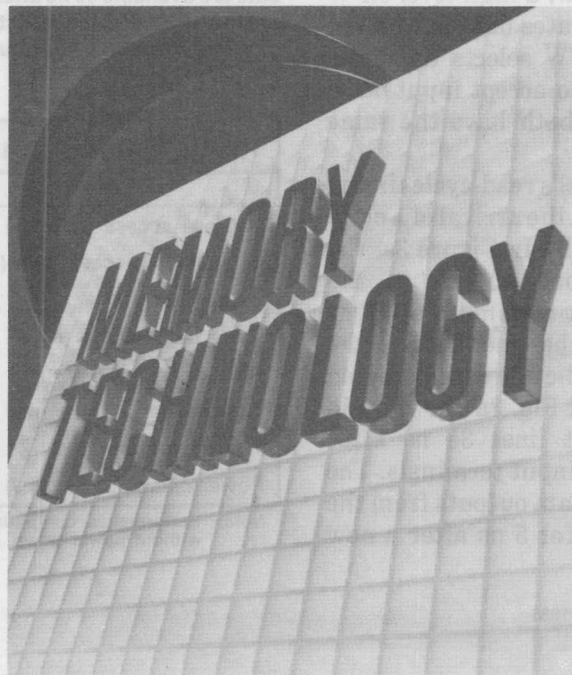
Until recently, SRAMs selected for so-called high-access-frequency, shallow-memory designs (cache, buffer, etc.) were invariably bipolar devices—Schottky TTL or emitter-coupled logic (ECL). But the emergence of SMOS gives memory-system designers several benefits over bipolar TTL devices. These include higher density—leading directly to reduced parts count—lower cost/bit and less power consumption. Even when compared with low-power CMOS, the 2149 offers system performance advantages.

To conserve power, the 2149 again looks to circuit-design techniques, this time in the form of an internal self-power-down feature. Although conventional memory devices provide a chip-selectable power-down, the 2149 takes a portion of the X-address inputs and predecodes them to select one of four groups of 16 X-decoders. Essentially, three of

the four groups are powered-down for any input-address condition. This translates directly to a 75% reduction in X-decoder power dissipation. A similar technique is used on the write circuitry—the write circuits are not powered-up until the device receives the proper control signal.

The 2149 seems certain to influence low-cost, low-package-count cache memories. For example, in a 16-bit system, a relatively simple but high-performance 2-kbyte cache memory can be

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constructed with less than 25 ICs, and only seven of the packages are 2149s. This gives designers an important tool with which to maximize a computer system's cost/performance ratio.

Another architectural trend, the writable-control store, consists of a high-speed SRAM array for storing microprogram instructions. The RAMs need fast access-times because microinstruction fetch operations are on the critical machine-speed path. What's more, control-store implementations usually have a long word width since one bit must directly control each of the computer's primitive operations. Control words of 99 or more bits are not uncommon in such systems. With its 35-ns access time and $1\text{-k} \times 4$ organization, the 2149 is ideal for small-to-medium-density writeable-control-store designs.

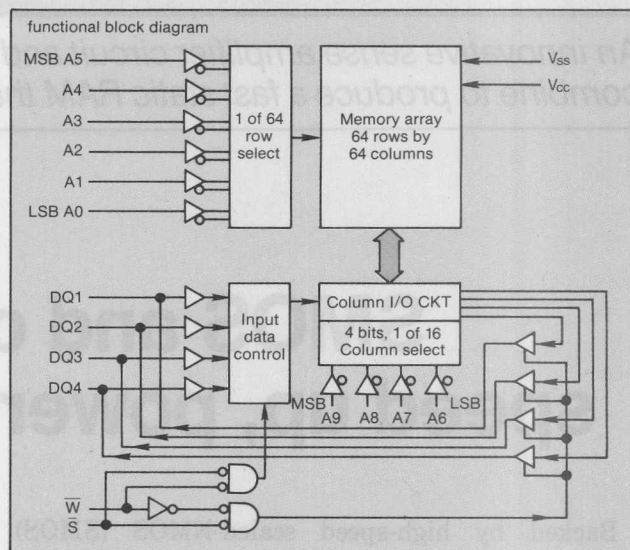
Static, but not slow

The TMS2149 is a completely static memory device; it requires no clocks, no refresh and no timing strobes. Packaged in a high-density 18-pin plastic or ceramic DIP, the chip operates from a single 5-V supply and draws a maximum of 120 mA at 0°C . All inputs and outputs are compatible with Series 74, 74S and 74LS TTL—no pull-up resistors are required.

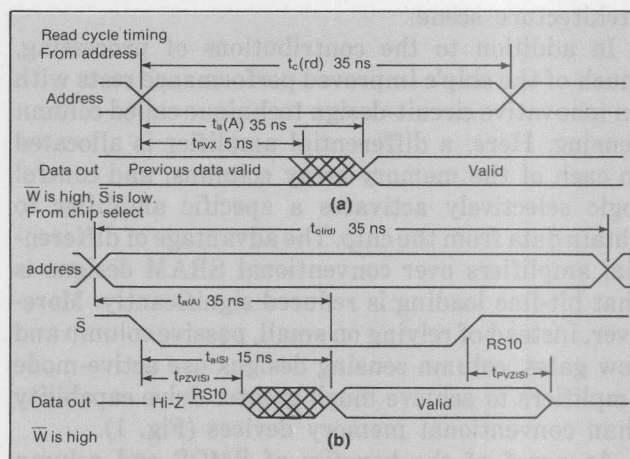
Ten address inputs select each of the 1024 4-bit words stored in the SRAM (Fig. 2). Address inputs must remain stable for the duration of a write cycle. The chip-select terminal (\overline{S}) is central to the 2149's overall operation. When \overline{S} is low (enabled), the chip is in an operational mode. In this condition, the data-in/data-out (DQ) pins serve either as data inputs or data outputs, depending on the logic level at the write-enable (\overline{W}) terminal. And when \overline{S} goes high, the chip is deselected; data-in is inhibited and data-out is in the floating or high-impedance state.

Both the read and write modes are selected via the write-enable pin. With \overline{S} low, a high level on \overline{W} selects the read mode and activates data-out on the DQ terminals. A low level on \overline{W} selects the write mode and allows the DQ pins to accept input data. Data-inputs and data-outputs both have the same polarity.

Figures 3a and b show the 2149's read-cycle timing from address-input (a) and from the arrival of a chip-select signal at the S terminal (b). In Figure 3a, the total read-cycle time—from one address to the following address ($t_c(\text{rd})$)—is a maximum of 35 ns in the top-of-the-line 2149-3. Other members of the series (-4, -5 and -7) have read-cycle times ranging from 45 to 70 ns. Also note that Fig. 3a shows valid data appearing on the output lines 35 ns after addresses are presented at the input terminals. The parameter t_{pVX} indicates that data outputs from the previous address remain valid for 5 ns after a new



1. Address inputs to the TMS2149 come in on lines A_0 through A_9 , while read and write data are handled through the DQ terminals. The main control pin is chip-select (\overline{S}), which controls read and write operations, and internal functions.



2. A read-cycle timing diagram for the 2149 shows that valid data are available 35 ns after addresses are valid (a), and only 15 ns from a chip select signal (b). The chip-select access time is the fastest among current $1\text{-k} \times 4$ static RAMs, MOS or bipolar.

Table. Performance parameters—fast SRAMs

	12149	93415 (4)	TMS2149
Address access time (ns)	45	30	35
Chip select access time (ns)	20	20	15
I_{cc} operating (mA)	180	520	120
Write pulse width (ns)	25	20	20
Write recovery time (ns)	0	25	0
Address set-up time (ns)	0	5	0
Write cycle time (ns)	45	50	35
Power-delay product (pJ)	44.5k	85.8k	23.5k

Note: Performance comparison of existing $1\text{k} \times 4$ static RAMs without power down. All values listed are worst case.

address is presented.

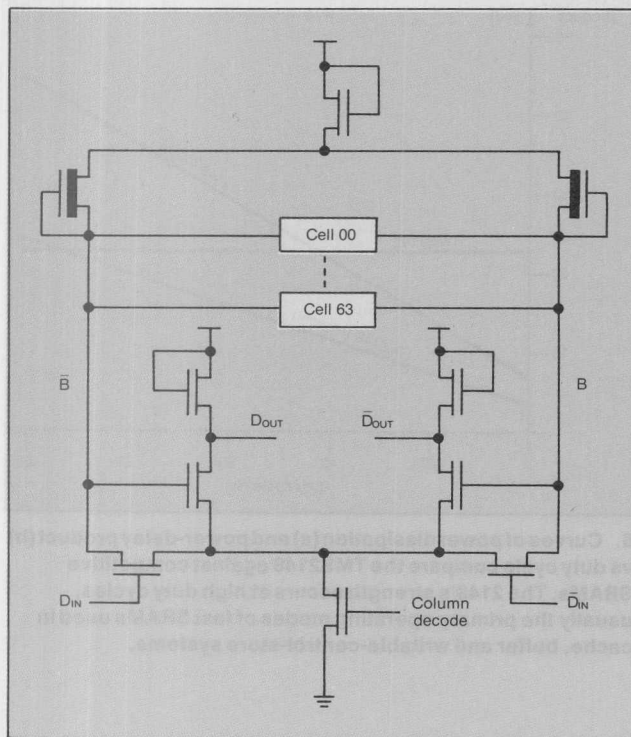
The key feature in Fig. 3b is access time from chip select, or $t_a(S)$. At 15 ns in the -3 version, the specification is a maximum of just 30 ns in the -7 device. This provides ample time for memory-system chip decoding without compromising access time.

The parameter $t_{pZV}(S)$ is a measure of the time to disable the outputs after a change in the chip-select level. This time is specified at a maximum of 10 ns in the -3 and 15 ns in the -7. Access times are measured into a capacitive load of 30 pF and a resistive load consisting of a 480- Ω pull-up resistor plus a 255- Ω pull-down resistor.

Column sensing—a new technique

The most significant speed-power product improvement over previous RAM designs results from the 2149's distributed-column sense-amplifier circuit. In the scheme shown in Fig. 4, each of 64 columns drives its own amplifier to activate the common data-out lines.

A read operation is performed when the desired column is selected. Selection activates the amplifier, which then differentially drives the data line to the correct state. The writing technique is novel since the data-in lines control the gates of the bit-line pull-down transistors. When a column is selected, writing is accomplished by forcing one data-in line to V_{cc} ;



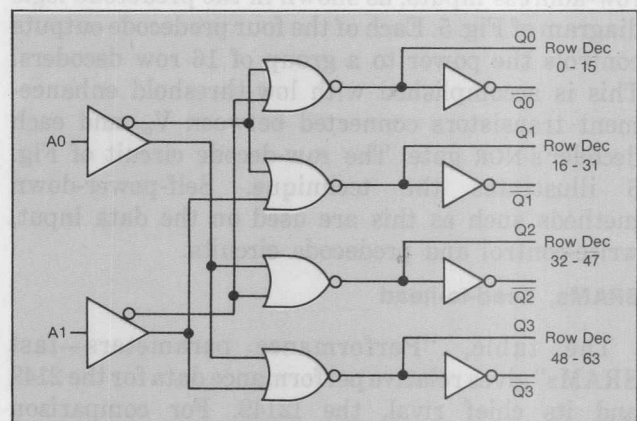
3. The 2149's distributed-column sense amplifier holds the key to the chip's high speed and improved writability. One amplifier connects to each column of cells. Each pair of data lines is common to 16 amplifiers, feeding one of four outputs.

this pulls the bit-line to a low level. Simultaneously, the complement data-in line is held at a low level, allowing the complement bit line to be pulled towards V_{cc} through the bit-line bias circuitry.

The significant feature of this technique is that the bit-lines are completely isolated from any data-line loading. This increases the efficiency of the small memory-cell transistors when they drive the bit lines. Experimental results predict a 6-ns address-access-time improvement over conventional SRAMs using pass-transistor designs.

Although separate data-in and data-out lines occupy more interconnect area than the conventional common data-line approach, this disadvantage is offset by access-time improvement, particularly for read-after-write cycles. In other SRAMs, data lines must recover by as much as 3 V for a read-after-write of opposite data. The data-line voltage split with the column-amplifier circuit, however, is essentially constant for both the read and write cycles (See "Negative Bias Yields Positive Results").

Differential operation of column amplifiers offers several advantages. First, the circuit provides a precisely-controlled differential voltage gain. And the column-decode circuitry's dynamic requirements are reduced since just a single, small transistor is needed to activate the amplifier. Because the source terminal of this transistor is at ground potential, a



4. A row predecode logic circuit, controlled by the two most-significant address inputs, reduces row-decode power dissipation by 75%.

column. As a result, a very-low-power, unbuffered NOR gate is adequate for column selection. Indeed, the less the conductance of the column-select transistor, the greater the common-mode rejection provided by the amplifier. When this technique is coupled with the exclusive use of enhancement-type transistors, it adds to the stability of the design across a wide range of process variations.

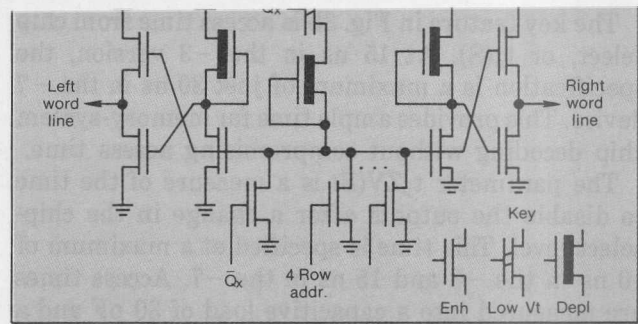
To achieve low-power operation, sufficient voltage gain, and ease of writing, the bit lines are pulled-up with depletion-load transistors. Moreover, to provide better operation in the saturation region, and to prevent leakage through unselected column amplifiers, the bit-line bias is held at least one enhancement-threshold-voltage-drop (V_t) below the minimum data-line voltage. A low bias on the bit line results from placing a common, saturated enhancement-load transistor between V_{cc} and the bit-line depletion-load devices. Together, the series enhancement and depletion combination limit the bit-line current while maintaining efficient operation of the column amplifier.

Rather than opting for a conventional buffered NOR gate on the row decoders, TI's power-conversation method allows only 16 of the 64 row decoders to be powered-up at any time. The activated group is selected by predecoding the two most-significant row-address inputs, as shown in the predecode logic diagram of Fig. 5. Each of the four predecode outputs controls the power to a group of 16 row decoders. This is accomplished with low-threshold enhancement transistors connected between V_{cc} and each decoder's NOR gate. The row-decode circuit of Fig. 6 illustrates the technique. Self-power-down methods such as this are used on the data input, write-control and predecode circuits.

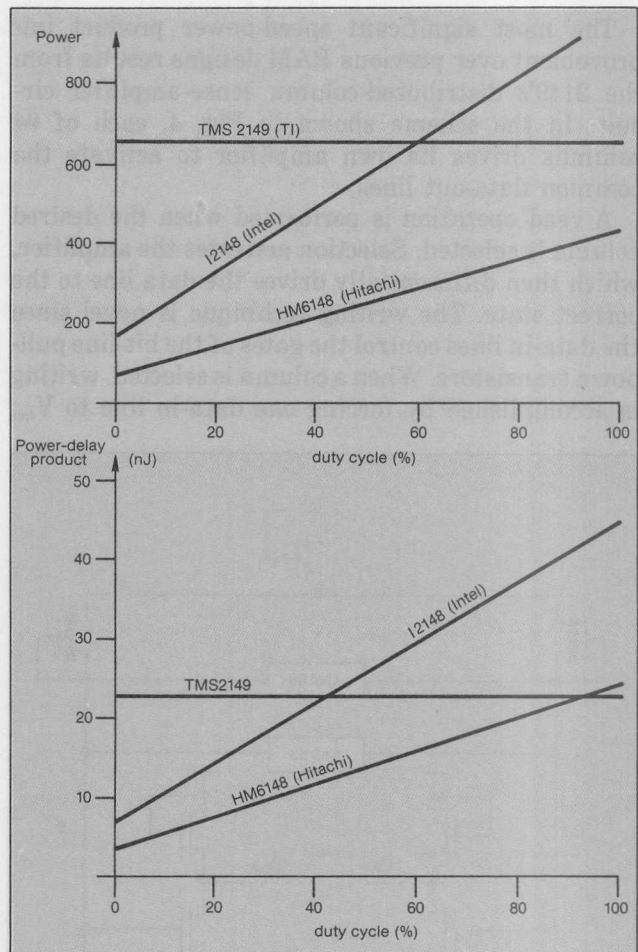
SRAMs, head-to-head

The table, "Performance parameters—fast SRAMs" gives relative performance data for the 2149 and its chief rival, the I2149. For comparison purposes, the table also provides data for a $1\text{-k} \times 4$ bipolar SRAM. However, comparable TTL bipolar devices are available only as $1\text{ k} \times 1$, so four bipolar chips must be operated in parallel to equal a single $1\text{-k} \times 4$ MOS RAM. Thus, the bipolar RAM data are for four 93415 devices. All comparisons are made without powering-down the chips, and data are worst-case.

Speed-power product, or power-delay product, is considered the best overall figure-of-merit—the lower the figure, the better the device. At the bottom of the table, the TMS2149's power-delay product is about half that of its NMOS challenger, the I2149. And not only is the TMS chip far superior to bipolar



5. In a row-decode circuit, signals Q_x and \bar{Q}_x from the predecode circuit (Fig. 5) select one of four quadrants, while the other three are powered-down.



6. Curves of power dissipation (a) and power-delay product (b) vs. duty cycle compare the TMS2149 against competitive SRAMs. The 2149's strength occurs at high duty cycles, usually the primary operating modes of fast SRAMs used in cache, buffer and writable-control-store systems.

RAMs in power-delay product, it consumes far less power, occupies significantly less printed-circuit board area and writes faster. With its worst-case access time of 35 ns, the TMS 2149 beats the other MOS device by 10 ns, or about 25%.

Although the TMS2149 contains an internal self-power-down feature, the device is not classified as a true power-down device like the 2148-type SRAM. Thus, it has speed and power advantages when applied in shallow-memory systems, or in systems in which the device duty cycle is greater than about 40%. In fact, the TMS2149 speed-power product surpasses that of its lone CMOS rival, the HM6148, when the devices remain selected for the majority of the time. Figures 7a and b illustrate power dissipation and power-delay product vs duty cycle

for the TMS2149 and the two primary powered-down MOS competitive devices. At a 60% duty cycle, the TMS device consumes no more power than the original 2148 device. However, the figure shows that the HM6148 maintains a power-dissipation edge, but because of its 55-ns access time, the CMOS chip gives way in speed-power product at a duty cycle of about 92%.

Even at the lowest duty cycles, the TMS chip offers advantages over power-down designs. As duty cycle is reduced, the average access-time approaches the chip-select access time, just as it does for the other NMOS devices. But the TMS2149 gains the upper hand since it can access from chip-select in only 15 ns—three times faster than its nearest power-down rival.

Negative bias yields positive results

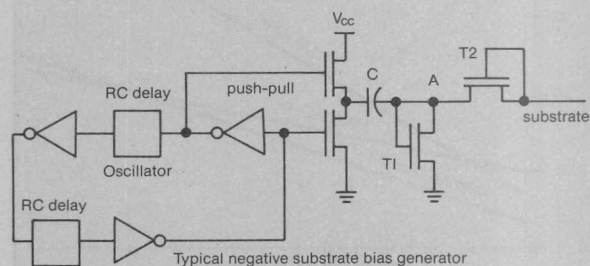
For some time, MOS memory designers have considered an on-chip substrate bias scheme to improve device performance. In dynamic RAMs, on-chip bias creates problems with the control of signal coupling through the substrate, particularly when the DRAM is clocked. Static RAMs, however, are an inherently heartier breed, and do not suffer from the signal-coupling syndrome.

High-speed SRAMs like the TMS2149 operate unclocked; thus large control-signal transients are of less concern than with DRAMs. While DRAMs can control noise with a grounded-substrate, SRAMs—by incorporating an on-chip bias generator—take advantage of the performance enhancements made available through substrate bias (see schematic).

A typical substrate bias generator consists of a ring oscillator serving as an input to a class-B push-pull amplifier. The amplifier output is coupled across a relatively large capacitor, C, shown in the schematic. MOS transistor T₁ functions as a diode-clamp to retard the coupling as the voltage rises across the push-pull.

Node A is pumped down to a voltage between -3.5 and -4.0 V on the negative or falling phase of the amplifier. Node A rises no higher than a single enhancement-transistor voltage drop (V_t) above ground on the rising or positive phase. The inherent filtering action of T₂ (also connected as a diode) plus the substrate capacitance maintains a relatively constant -2.5 V on the substrate.

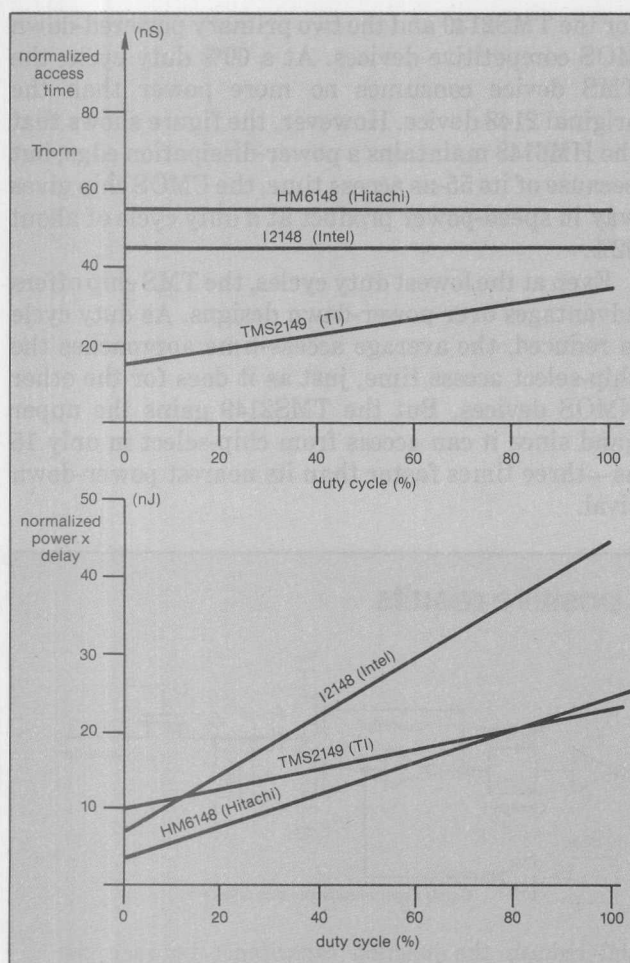
A memory device constructed with substrate biasing benefits in three ways: First, the negative poten-



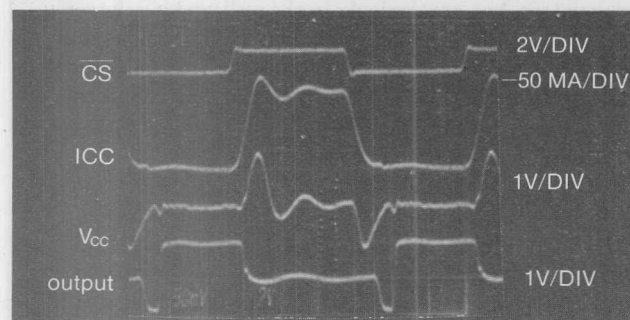
tial reduces the junction capacitance between the active source and drain regions, which are doped as n+ and the p-type substrate. This leads to faster switching. Second, negative bias reduces the so-called back-gate body effect in all of the memory's transistors, but particularly in the pull-up transistors. This results from reducing the effective doping of the substrate by depleting acceptor ions from the implanted channel regions. Reduced body effects improve the switching rise times of the pull-up transistors—otherwise, operation slows because of a gradual increase in threshold voltage as the potential between source and substrate grows more positive.

Finally, an unregulated bias generator typically pumps to a more negative voltage as V_{cc} rises. This occurs because more voltage is available across the capacitor. A higher bias voltage tends to compensate for the added operating current that flows at a higher supply-voltage, since the threshold voltage of all transistors is increased. This reduces the rate of change of current with supply voltage.

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7. Normalized curves of access-time (a) and power-delay product (b) illustrate the significant advantages offered by the 2149 regardless of duty cycle.



8. Current surges complicate the operation of conventional power-down SRAMs during select transitions. This oscilloscope photo shows how the current surge affects the output data.

The curves of Figs. 8a and b show normalized access time and normalized power-delay product as a function of duty cycle. The normalized average access time, T_{norm} , is given by,

$$T_{norm} = \text{duty} \times T_{aads} + (1 - \text{duty}) \times T_{acs},$$
 where duty is the duty cycle,

T_{aads} is the address access-time and

T_{acs} is the chip-select access-time.

The normalized access-time analysis indicates that the TMS device has a decided advantage over the others. In terms of power-delay product, the TMS loses slightly to NMOS chips at very low duty cycles, but gains strongly as the duty cycle increases. Note that at a duty cycle of about 80%, the TMS chip even overtakes the HM6148.

The system-level picture

As a system component, the TMS2149 requires less cooling than competitive devices since it can run at $\frac{1}{2}$ the power of an I2149, and at $\frac{1}{4}$ the power of four bipolar 93415s. And compared with the bipolar chips, the 2149 occupies just $\frac{1}{4}$ the board space.

Another factor favoring the TMS2149 is that it does not rely on the extensive use of ceramic capacitors to eliminate heavy surge currents—because of its self-power-down design, such surges are virtually non-existent. On the other hand, power-down devices experience large surges when the chip-select terminals are pulled down. The significance of the nose problem is shown in Fig. 9. The current and voltage spikes for a powered-down 4-k SRAM show how the surge is conducted to the chip's output.

Because of its simpler semiconductor processing and smaller die area, the TMS2149 gains a cost advantage over CMOS memory devices. The average unit price depends primarily on yield—the number of good die per wafer divided by the total number of chips per wafer. For planning purposes, yield can be expressed empirically as,

$$\text{Yield} = 1/(1 + AD)^{N_c} \times 100\%, \text{ where}$$

A is the die area,

D is the process defect density, and

N_c is the number of critical mask levels.

The equation shows that yield increases exponentially as the number of critical mask levels is reduced. Since SMOS technology typically uses two fewer critical mask levels than comparable CMOS processes, manufacturing cost per die is much less. Thus, system designers can expect to pay a 25% premium for CMOS over SMOS devices. □

How useful?

Immediate design application
Within the next year
Not applicable

Circle

544

545

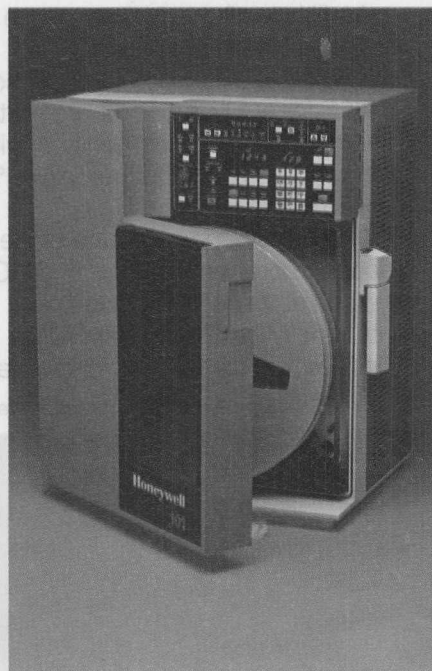
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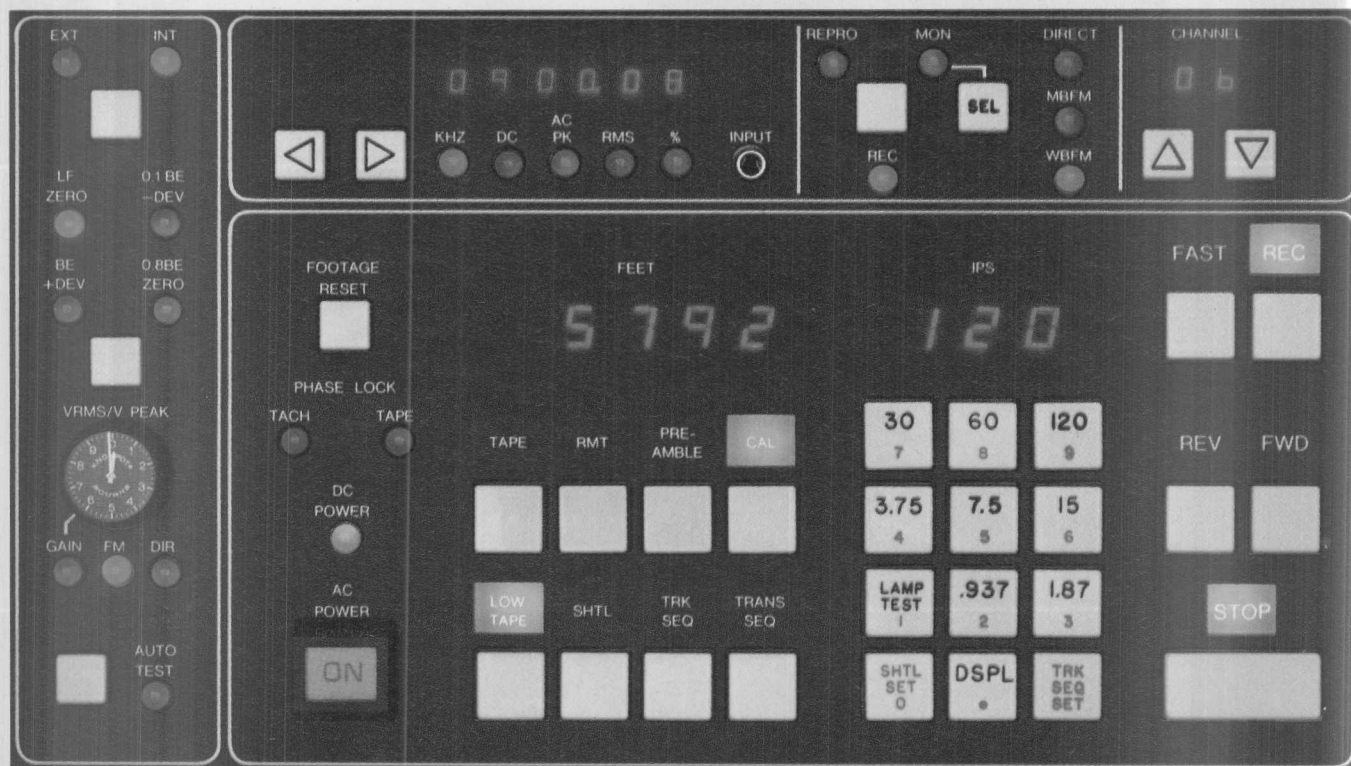


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A track-following drive with speedy access makes floppy-disk technology more than an alternative to Winchester for small-system storage.

High-density floppy drive suits small-system storage

Even as Winchester technology has been promising to fulfill on-line storage requirements for big and small systems alike, floppy-disk technology has been quietly increasing its capacities. Now a high-capacity floppy-disk drive featuring a true track-following servo threatens to steal Winchester thunder in the small-system area. With 8.4 Mbytes of storage already, the Model 899 presents a dilemma to small-system designers who thought lower-capacity Winchester disks were the only choice. But a closer evaluation of the performance, capacity, and positioning accuracy of the floppy should clear that up.

The key innovation in the 899 is the track-following servo (see "The Track-following Servo")—a first in floppy drives—which expands track density from 96 tracks/in. to 150 tracks/in. But several other impressive features should also help make up the designer's mind:

- Two diskettes—each having a dual head—within the standard-size floppy-drive housing stretch storage capacity.
- A voice-coil positioner, used on all PerSci floppy-disk drives, improves full-stroke seek times.
- Microprocessor control reduces chip count and optimizes track-to-track speeds.
- Standard media, in the form of diskettes, cut costs—a major advantage over drives that require special media.
- Read compensation op-

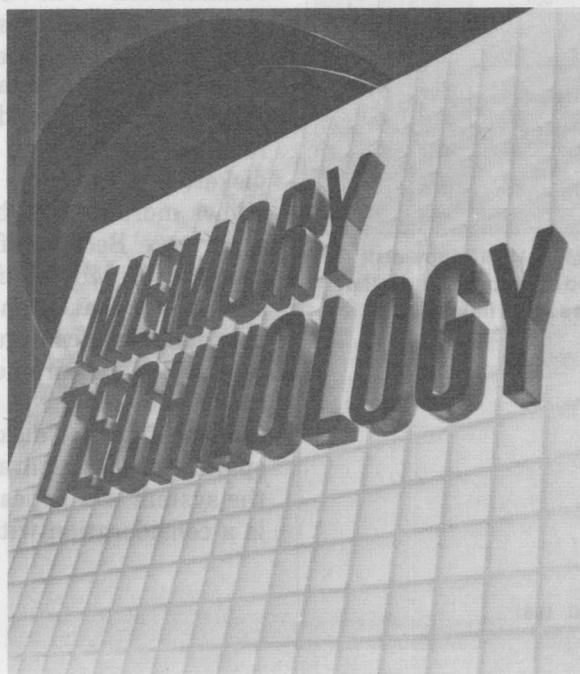
timizes the compensation for each track.

Depending on his application, a system designer faces a number of choices to get 7 Mbytes of on-line storage: 78 single-sided, single-density minifloppies, 24 single-sided, single-density, 8-in. drives; six double-sided, double-density, 8-in. drives; one Winchester disk with tape or floppy backup; or one Model 899 (or two 899 drives for 15 Mbytes of removable storage). If a system requires the high transfer rate and fast random access of hard-disk drives, which are the result of fast rotational speed, then the obvious selection will be a Winchester. However, in most other systems, the Model 899 will be the most economical and convenient choice. Furthermore, the 899 offers faster random access than most stepper-motor-driven hard-disk drives. The reason? Track following.

One critical factor in accomplishing track following is the use of voice-coil positioning (Fig. 1). While the voice coil costs more than a stepper, it eventually pays back in speed and positioning accuracy.

The accuracy of the head-positioning mechanism using the voice coil stems from the closed-loop feedback, which has been referenced to a window on a glass corresponding to the track and has been corrected for each sector by means of positioning information from the diskette. By contrast, a stepper-motor system is mechanically referenced. Although head replacement may be quite accurate when the drive is delivered, this accuracy could degrade over time.

The speed benefits of voice-coil positioning were



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well established before its new-found importance in track following. Take full-stroke seek.

In the Model 899, 230 tracks must be traversed. The fastest available stepper-motor positioned floppy disk can run no faster than 3 ms track-to-track. With the stepper, by nature, moving one step at a time, the fastest full-stroke seek possible on 230 tracks—assuming this density is possible with a stepper—would be 690 ms plus settling time. The voice-coil positioner, moving from one track to another without stopping on intermediate tracks, performs a full-stroke seek in 90 ms.

On single-track, the total speed of the voice-coil positioner has somewhat less impact. (It's like saying a Porsche goes ten feet just a little faster than a Volkswagen.) But in all cases, the track-following scheme makes full use of the fast positioning and

accuracy of the voice coil. If the head is off-track, it can be repositioned to the center of the track by applying the amount of correction necessary to the feedback loop. A stepper-motor positioner might have to move three or four steps to reposition, which makes repositioning very difficult, if not impossible.

System integration improves, too

The use of the voice coil does necessitate certain unique system integration requirements. Since the controller can send the stepping pulses to the drive as fast as every 200 μ s, all the stepping pulses are issued in 5 ms or less. For a long seek, for example, it might take 90 ms for the seek to be completed. In addition, there would be an 85-ms delay between the last stepping pulse and the point at which the head has reached the destination track.

For shorter times, this time is shorter. In order to take full advantage of the fast positioning, some sort of handshaking should be provided to inform the controller that the seek has been completed. PerSci uses a special line to the interface called Seek Complete. However, most disk operating systems (DOSs) are not written with a check for a seek complete, and have to be slightly modified to accommodate this requirement. And even though the 899 updates its internal track-parameter tables (which predict the location of the tracks for seeks) on a continuous basis, sometimes (albeit rarely) the entire table must be recalibrated.

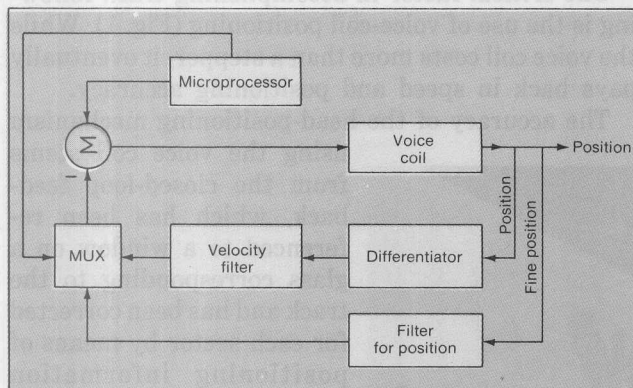
To make this recalibration transparent to the user, it is usually done within the seek timing interval. This might increase the time for that seek to over two seconds, which makes the monitoring of the Seek-Complete line essential.

The tables are recalibrated on each restore or after a new diskette is inserted, and are updated on each sector pulse. Barring a restore or diskette change, recalibration will be needed only under extraordinary circumstances, like an extreme change in humidity or temperature.

Benefits and special considerations alike accrue from the 899's dual-drive configuration. For sure, reading and writing data on both sides of two diskettes in the same drive with shared electronics allows more data to be packed into less space at a lower cost. Because of its packaging design, the 899 can store 8.4 Mbytes of data in a standard-size floppy slot—twice that of one diskette. At the same time, this dual-drive configuration changes some system-integration requirements.

For one thing, the 899's multiple heads move in tandem—if the disk controller treats the two spindles as two separate drives with separate heads, the system will appear to receive seek errors. (This is a consideration with all dual-head floppies.) The

Follow the format	
No. of bytes	Hex value
12	00
1	A1 (missing clock pulse)
1	FE
1	Track No.
1	Sector No.
2	XX (CRC)
18	00
1	A1 (missing clock pulse)
1	FB
256	XX (data)
2	XX (CRC)
The rest of the sector	4E



1. The track-following servo of the Model 899 floppy-disk drive consists of an optical servo and a microprocessor that switches the loop filters and provides some inputs to the servo loop.

problem can be overcome by altering the DOS. Or, a controller can be designed to store the position of the head not selected and reposition the head when it is selected. Even after this is done, however, the DOS may still require changing to take care of possible timing problems.

Off-track considerations

Additional consideration is required in the controller because of the track following of the 899. Since all four heads are referenced entirely to the diskettes, the heads may be off-track with respect to each other. Although this positioning is automatically corrected by the embedded servo system, the controller must be equipped to wait for a delay when a drive is

selected.

Back on the positive side, much of the credit for allowing the drive to be packaged in a standard-sized housing goes to the internal microprocessor, the main reason for a reduction in chip count. Among its functions, the 4-MHz Z80—along with 4 kbytes of ROM, 1 kbyte of RAM, and 30 lines of I/O—drives a 7-bit d-a converter and a 5-bit a-d converter (Fig. 2). It interfaces directly with the STEP, DIR, and RESTORE lines, and reports drive status to the controller, including READY, TROO, and SEEK COMP.

The processor's primary function, however, is to control servo activity—predicting track location and correcting head position—thus yielding the fastest possible seek time. (The table of optimum velocity

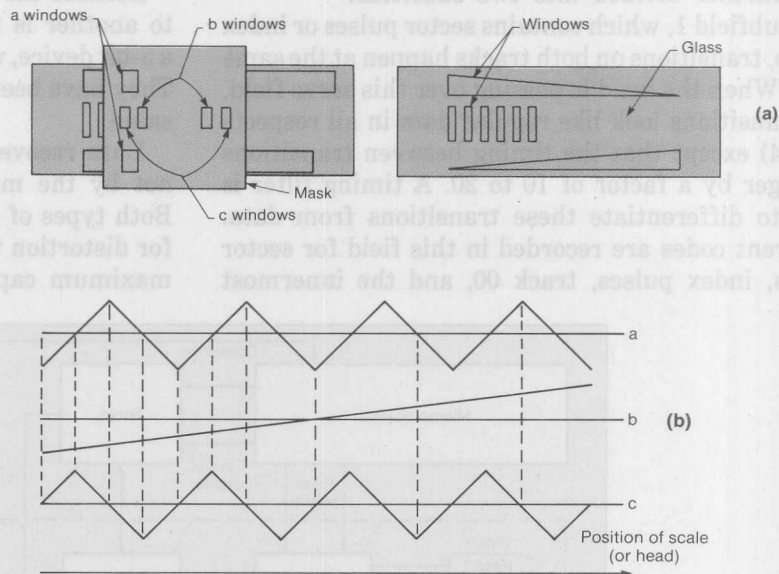
The track-following servo

The optical servo in the Model 899 floppy-disk drive consists of an optical scale, a mask, a lamp, amplifiers, a differentiator, two loop filters, a voice-coil driver, a voice coil, and the microprocessor. The processor switches the loops and provides some inputs to the servo loop.

The scale, which is attached to the head carriage, has a mask on one side and a lamp on the other (Fig. a). The mask and lamp are both attached to the drive. There are six windows on the mask and behind each window is a photocell. The photocells are paired.

The position of the scale relative to the mask generates the position-related output signals at the photocells (Fig. b). Signals a and c are used for fine positioning, while signal b is differentiated and used for velocity control. All the cross-points of the a and c signals and the zero-volt line are at the center of the optical tracks.

A detent pulse, generated at each of these points, is sent to the microprocessor to signal how many tracks the head has moved. To move from one track to another, the microprocessor puts



the velocity loop "in" and the position loop "out." It then outputs a velocity value through a d-a converter to the servo and counts the detent pulses.

The microprocessor increases the velocity as it receives the stepping pulses from the controller and decreases the velocity as it receives the detent pulses until the head is positioned on the required track, after which the processor

switches the loop to "position." The loop holds the head on the center of the track and removes the velocity value from the input of the loop. In the hold mode, the position of the head is changed by outputting a position value into the loop. This procedure is used for positioning the head over the center of the track during track following. Preformatted disks are normally used.

Memory Technology: High-density floppy

values is stored in ROM.)

Track following enables the use of standard media on the 150-track/in. drive with no more environmental consideration than with standard floppies. This is fortunate because cost considerations regarding higher-density floppies make it paramount that the new drives use standard, flexible-disk media. Not only do special media greatly escalate costs but high-performance diskettes have been slow in coming. The best solution is the standard diskette.

Preformatted diskettes

The diskettes used to implement track following in the 899 are preformatted with servo information (Fig. 3). Each track is divided into 32 sectors, which are preceded by a servo field. The servo field, which contains sector or index pulses and positional information, consists of two side-by-side servo tracks, each further divided into two subfields.

In subfield 1, which contains sector pulses or index pulses, transitions on both tracks happen at the same time. When the head is passing over this servo field, the transitions look like regular data in all respects (Fig. 4) except that the timing between transitions is longer by a factor of 10 to 20. A timing filter is used to differentiate these transitions from data. Different codes are recorded in this field for sector pulses, index pulses, track 00, and the innermost

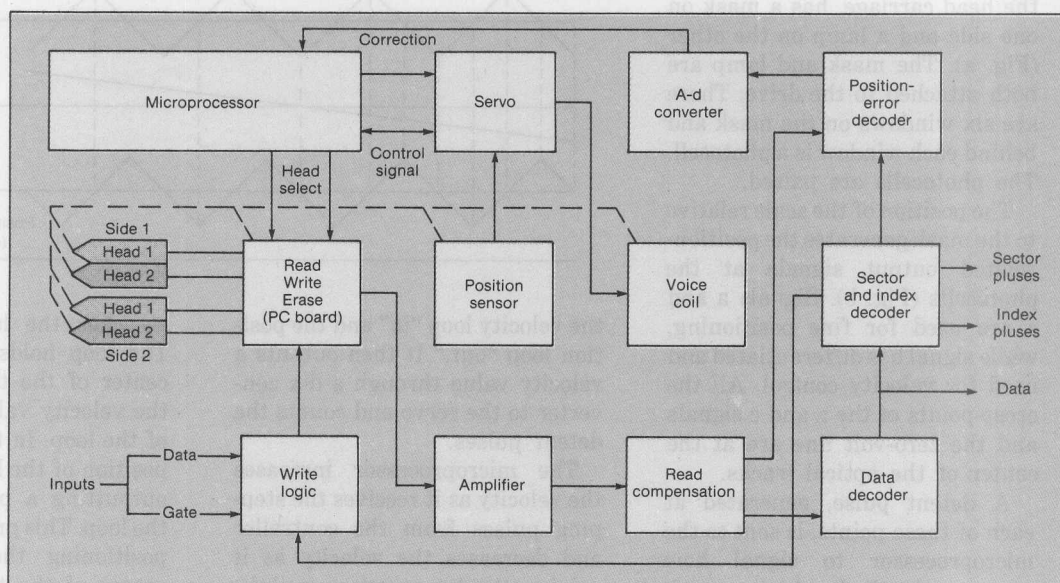
track, track 230.

In subfield 2, there are two transitions, or one per servo track. The transitions occur at different times. Depending upon the position of the head, the corresponding read-back signal from one of these transitions might be stronger than the other (Fig. 5). The difference in the amplitude of these two signals indicates how far off track center the head is positioned.

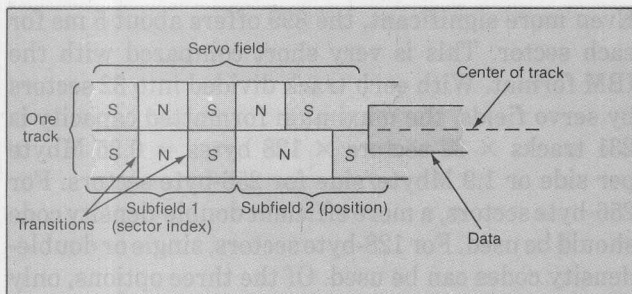
These two signals are further separated by a timing filter, and the difference is sent to the microprocessor through the a-d converter. Accordingly, the microprocessor corrects the position of the head through the d-a converter. If required, the microprocessor can also correct its reference tables. The head stays in its new position for the sector and is corrected again on the next sector and the next, and so on.

Because the amount of correction from one sector to another is relatively small, the a-d converter is a 5-bit device, while the d-a converter is a 7-bit device. They have been scaled so that their resolution is the same.

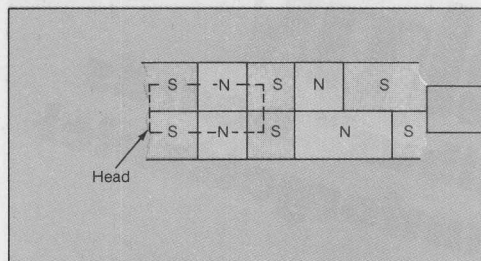
Data recovery is handled by read compensation, not by the more familiar write precompensation. Both types of compensation are intended to correct for distortion that occurs when data are recorded to maximum capacity on the diskette's inner tracks.



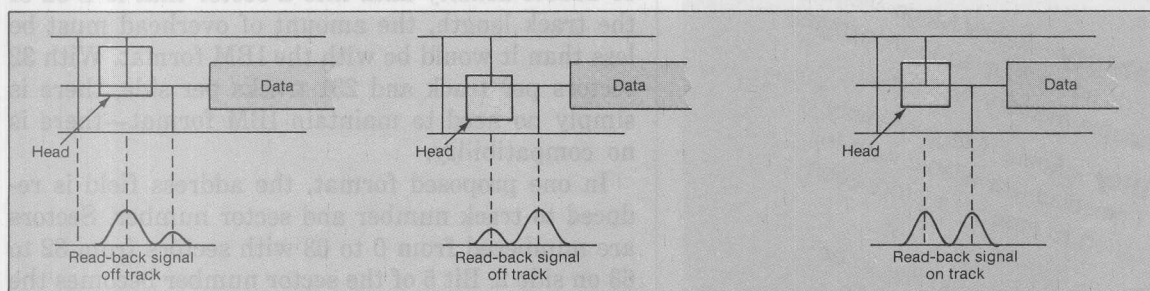
2. Put together voice-coil positioning, a track-following servo, and a dual-head/dual-drive configuration, and one result is high-density floppy-disk recording.



3. Track following is implemented using disks preformatted with servo information. The servo field consists of two side-by-side servo tracks and two subfields.



4. When the recording head is passing over the servo field in subfield 1, the transitions look like normal data, except for the timing between transitions by a factor of 10 to 20.



5. Depending on the position of the head in subfield 2, the corresponding read-back signal from one or two transitions might be stronger than the other.

Because the flux reversal corresponding to one bit cell at the inner track is very close to the next bit cell, they interact. This interaction may cause a shift of position on one or both bits. Read-back signals have a lower amplitude in areas where the transitions are close together. Write precompensation will cause the data to be distorted before being recorded on the disk in such a way that the data will be compensated for by distortion caused by the head and media. Unfortunately, the amount of distortion is different from track to track. This precompensation function is done in most systems by the disk controller. In order to avoid complexity, nearly all controllers are designed to divide the diskette into two areas—the inside tracks and outside tracks. Each area has different amounts of compensation for each portion. Usually, no compensation is used for outside tracks and some compensation for inside tracks. This becomes a compromise between cost and performance.

With read compensation, a linear-phase amplifier with proper frequency response is added to the read amplifier. The gain of the compensating amplifier is controlled by the track number so the amount of compensation can be optimized for each track, which means very reliable data recovery. However, this technique cannot improve the signal-to-noise ratios. Only the frequency response is improved without destroying the phase response.

The read circuit of the 899 has also been designed to allow longer periods of no flux transitions than

is possible with standard floppies. The traditional data recovery normally consists of a differentiator and a zero-crossing detector, which will ideally detect all the peaks. If there are some flat areas in the signal, or data, however—resulting from having no flux reversal for greater than 5- μ s periods—then these areas will be adversely detected as transitions.

FM, MFM, and M²FM codes, which are widely used in floppy drives, all meet the common data-recovery timing requirements. Since more efficient codes do not have such frequent flux transitions, they cannot be used on standard drives. The 899 incorporates a level detector in the data-recovery circuit to differentiate between real and false transitions. As a result, the system designer can choose the code best fitting his application.

Formatting and interfacing

The interface for the 899 has characteristics similar to PerSci's Model 299B 3.2-Mbyte floppy drive and Model 699 6.4-Mbyte floppy drive. This commonality allows a single controller to be developed for controlling all three drives. The few notable differences bare in the interface of the track-following drive. For example, the double-sided signal has been eliminated: Because there are no single-sided 150-track/in. drives, there is no need for compatibility. What's more, floppy-disk signals Separated Data, Separated Clock, and Sync are not on the interface.

Data separation is left entirely to the controller.

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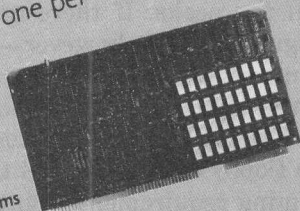
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CIRCLE 56

Even more significant, the 899 offers about 5 ms for each sector. This is very short compared with the IBM format. With each track divided into 32 sectors by servo fields, the maximum formatted capacity is 231 tracks × 32 sectors × 128 bytes = 0.95 Mbyte per side or 1.9 Mbyte/side for 256-byte sectors. For 256-byte sectors, a more efficient double-density code should be used. For 128-byte sectors, single or double-density codes can be used. Of the three options, only the 128-byte sector double-density doesn't require specific restrictions on timing.

To fit 128 bytes of single-density data or 256 bytes of double-density data into a sector that is 1/32 of the track length, the amount of overhead must be less than it would be with the IBM format. With 32 sectors per track and 231 tracks per side, there is simply no need to maintain IBM format—there is no compatibility.

In one proposed format, the address field is reduced to track number and sector number. Sectors are numbered from 0 to 63 with sectors from 32 to 63 on side 2. Bit 5 of the sector number becomes the side number. The address field is preceded by 12 bytes of ZEROs for double density or six for single density followed by 1A1 and 1FE.

This is followed by 2 CRC bytes, 18 bytes of ZEROs or 9 for single density, then A1, FB, 256 bytes of data, and 2 CRC bytes. This creates a total of 296 bytes per sector for double-density recording (see table).

This format should be repeated for each sector. There is no index mark. The read function can be performed in the same way as a 48-track/in. drive and all servo information and sector pulses can be ignored by the controller.

Because most existing floppy-disk controller chips are built to implement the IBM format, they cannot take advantage of the performance characteristics of this high-density drive. Since the TI9909 controller chips give the designer more freedom to select his own format, this chip could be used to control the 899 drive with the seek function outside the chip, thus taking full advantage of the voice-coil speed. And to be able to monitor the Seek Complete line, the seek function should be performed outside the chip. Also, PerSci offers controllers for the S100, Multibus, and Q bus.

The upshot for the design engineer has been a major increase in the importance of the floppy disk drive. □

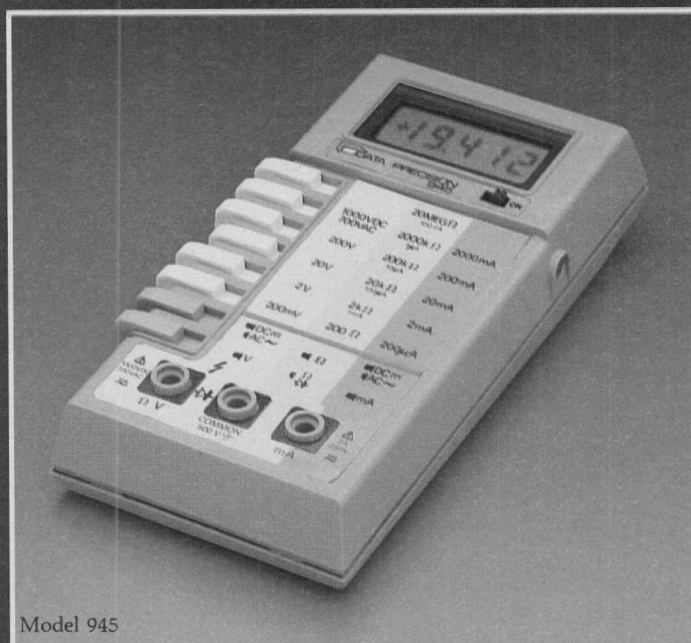
How useful?

- Immediate design application
- Within the next year
- Not applicable

Circle

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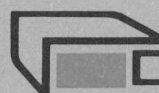
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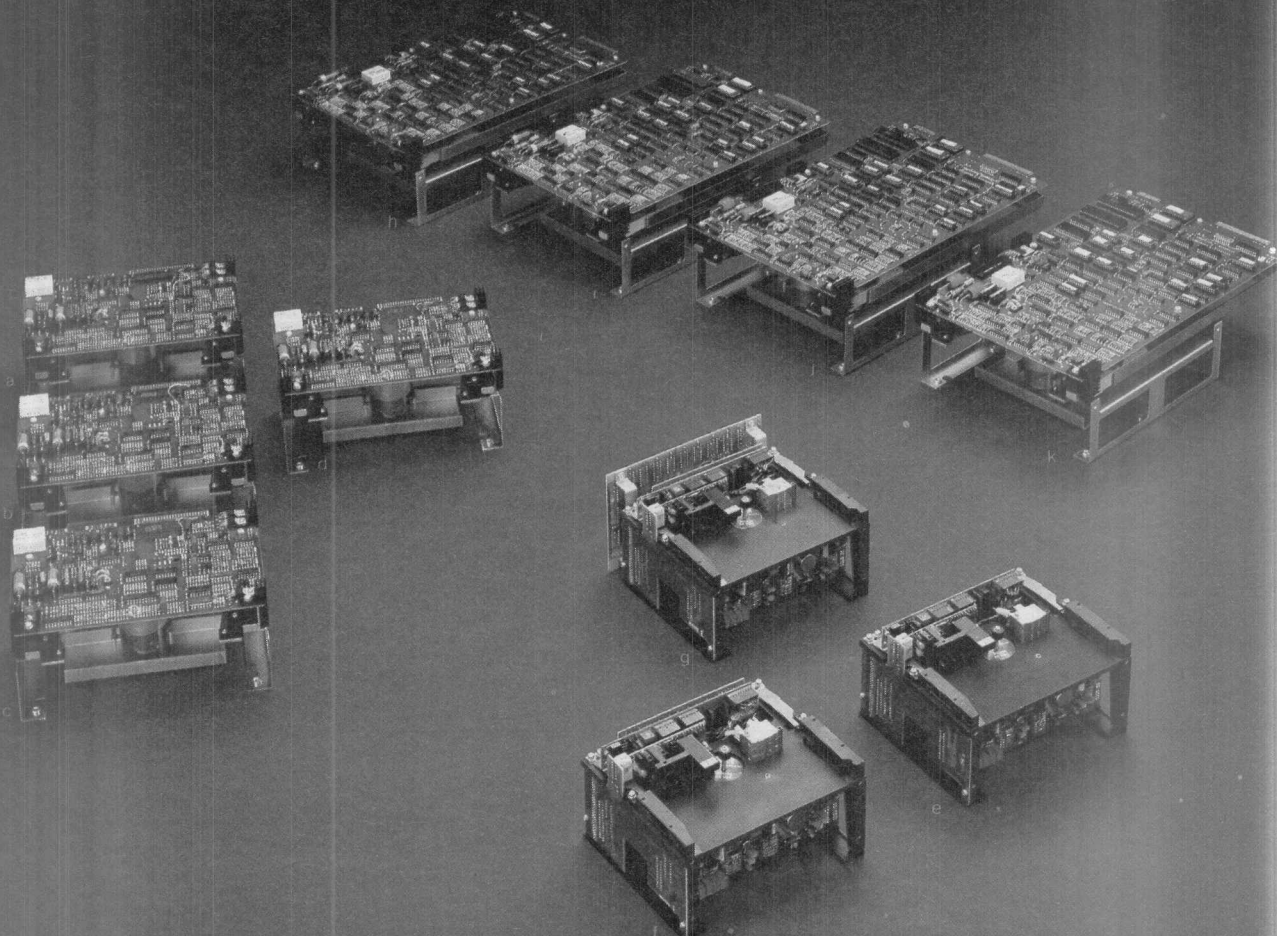
- a. 10 Mbytes/30 ips
- b. 10 Mbytes/90 ips
- c. 20 Mbytes/30 ips
- d. 20 Mbytes/90 ips

The Funnels

- e. 17.3 Mbytes/30 ips with
- f. Read/write electronics
- g. Control electronics
- h. Codec electronics

The Streamers

- i. 10 Mbytes/30 ips
- j. 10 Mbytes/90 ips
- k. 20 Mbytes/30 ips
- l. 20 Mbytes/90 ips



A new error-correction chip with dual-bus architecture interfaces easily with dynamic RAMs. Memory-system reliability soars and the additional parts count is relatively modest.

Keep memory design simple yet cull single-bit errors

In memory-system design, the demand for greater reliability is reflected by an increasing interest in error-detection and correction circuitry. Several semiconductor manufacturers have recently introduced error-detection and correction chips. They share a common architecture that features a multiplexed data bus. But the Intel 8206 error-detection and correction unit (EDCU) is different: This LSI device, fabricated in HMOS II, allows error correction to be added to memory systems with minimal overhead.

A single 8206 handles 8 or 16-bit data widths, and up to five 8206's can be cascaded to handle all multiples of eight bits (up to 80 bits). The 8206 corrects single-bit errors in a maximum of 65 ns for 16-bit systems and typically replaces 20 to 40 ICs, depending upon the number of features in the system.

Common error detection circuits simply recognize that data has a parity error. Correction circuits use the Hamming code as an extension of parity to detect and give the position of the error, allowing it to be corrected.

Single-bit correction and multiple-bit detection is the typical implementation, reflecting the tradeoff between the probability of errors in a system and the cost of additional memory. For a 16-bit system, single-bit error correction and double-bit error detection is im-

plemented by using 6 additional check bits, for an overhead of 37% (Table 1). Adding single-bit error correction to a system improves system reliability by at least a factor of 24 (Table 2).

Error correction is used extensively in mainframe and minicomputer design where memory sizes of several megabytes are common. Here the probability of error is directly related to the error rate of the individual RAMs and the number of RAMs in the system. As the number of RAMs increases, so does the system error rate.

With today's microprocessors, like the Intel eight-bit iAPX 88 and 16-bit iAPX 86 (each can directly address 1 Mbyte), typical RAM memory sizes are 100 kbytes and climbing. As a result, microprocessor system designers are looking to add error correction as simply as possible.

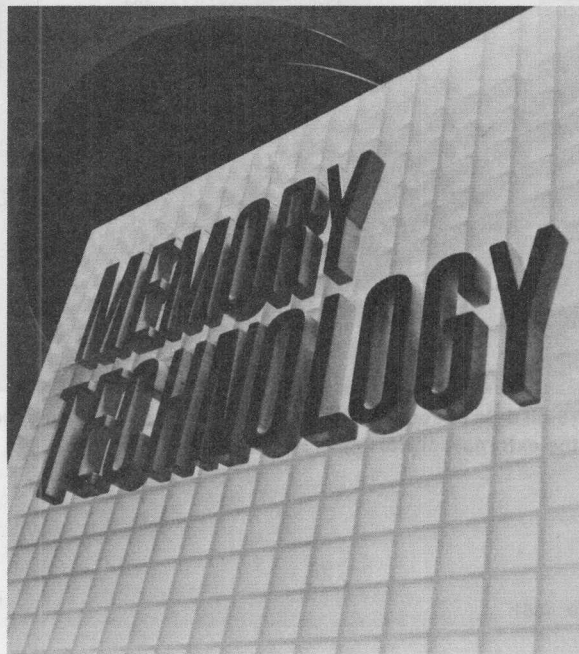
New bus architecture

The 8206 is the first 16-bit EDCU to use separate input and output data buses, a feature that simplifies system design, saves board space, and reduces parts

count. The new architecture is made possible by packaging the 8206 in a JEDEC type A 68-pin leadless chip carrier. Figure 1 shows the 8206's functional blocks.

During read cycles, data and check bits enter via the data input (DI) and check-bit input (CBI) pins, where they are optionally latched by the STB input. The data then take two parallel paths. The first path is to the data-output (DO/WDI) pins, where the uncorrected data are available 32 ns later. The second path is to the check-

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Santa Clara, CA 95051



Memory Technology: Error-correction chip

bit generator, where check bits generated from the data are compared with the check bits read from the memory.

The result of the comparison is the *syndrome*, a 5-to-8-bit value identifying which bit (if any) was in error. The syndrome is then decoded to a 1-of-16 bit strobe which is used to "flip" the bit in error (assuming the CRCT input is active). Syndrome decoding also tells the 8206 whether to assert the error flags. The 16 data output pins are enabled on a byte basis by the \overline{BM} inputs.

For write cycles, data enter the write data input (DO/WDI) pins and goes to the check-bit generator. The check bits are then written to the check-bit memory by the check-bit output (SYO/CBO/PPO) pins. These pins also output the syndrome bits during read or read-modify-write cycles.

Note that only the 8206's R/\overline{W} pin is typically used for control during a memory cycle. This pin informs the 8206 whether the cycle is a read (generate new check bits and compare to those from memory) or a write (generate new check bits only). During a read-modify-write cycle, a falling edge of R/\overline{W} tells the 8206 to latch the syndrome bits internally and output check bits to be written back into memory. The strobe input (STB) may optionally be used to latch data and check bits internally.

The 8206's dual-bus architecture saves the additional control lines and the sequencing logic required

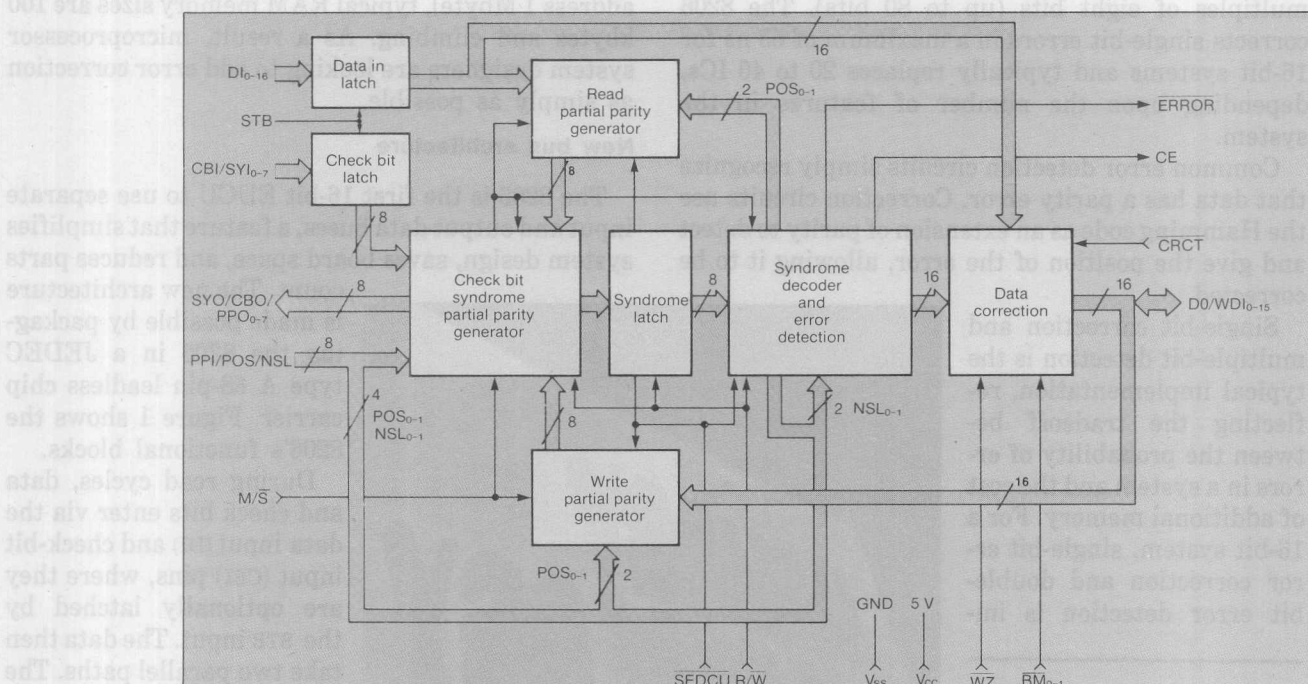
Table 1. Check bits required for single-bit correction, multiple-bit detection.

Data word bits	Check bits	Overhead % (#check bits/# data bits)
8	5	62
16	6	37
32	7	22
64	8	12
80	8	10

Table 2. Single-bit error correction increases memory reliability a minimum of 24 times.

*Memory size	MTBF (no error correction)	MTBF (single-bit error correction)	MTBF improvement ratios
32 kbytes	5.6 Years	133.6 Years	24
64 "	2.7 "	75.1 "	28
128 "	1.4 "	40.5 "	29
5 Mbytes	16 Days	10.8 "	246
8 "	8 "	6.1 "	278
16 "	4 "	3.3 "	301

*Based on a 16 kbit dynamic RAM with a failure rate of 0.127% every 1000 hours. Note: MTBF, though related to memory size, also depends on memory organization (e.g. word width, number of pages) that is not detailed in this table.



1. The 8206's two 16-bit data buses, one for data from the RAM (DI_{0-15}) and one for data to the system bus (DO_{0-15}), minimize the external control logic required.

by single-bus EDCUs. The principal advantages of dual-bus architecture can be illustrated by looking at the three types of memory cycles: reads, writes, and read-modify-writes.

In a read cycle (Fig. 2), data and check bits are received from the RAM outputs by the DI and CBI pins. New check bits are generated from the data bits and compared to the check bits read from the RAM. An error in either the data or the check bits read from memory means the generated check bits will not match the read check bits. If an error is detected, the **ERROR** flag is activated and the correctable error (CE) flag tells the system if the error is (or is not) correctable.

With the **BM** inputs high, the corrected word appears at the DO pins (if the error was correctable), or the unmodified word appears (if the error was uncorrectable). Note that for this correction cycle there is no control or timing logic required. The 8206's dual buses isolate the RAM outputs from the EDCU outputs. Special transceivers that prevent contention between the uncorrected RAM data and corrected EDCU data are not needed.

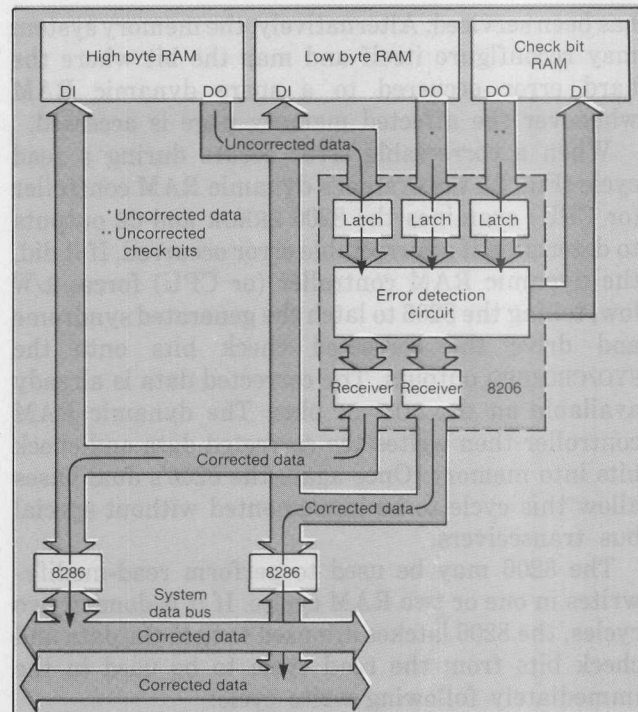
A syndrome word, five to eight bits in length and containing all necessary information about the existence and location of an error, is provided at the syndrome output (SYO/CBO/PPO) pins. Error logging is accomplished by latching the syndrome and the memory address of the word in error. The syndrome decoding of Table 3 can be used as a table lookup by the CPU.

If an error is detected during a read, the read cycle is extended to a read-modify-write cycle where the corrected data is rewritten to the same location. This offers several advantages:

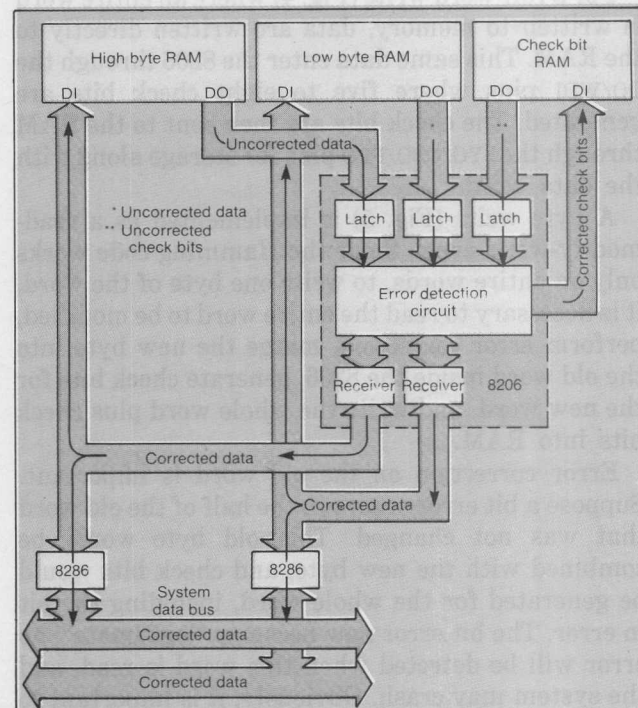
- Since soft errors are random, independent processes, the longer a soft error is allowed to remain in memory, the greater the probability that a second soft error will occur in the memory word, resulting in an uncorrectable double-bit error. By writing the correct data back to RAM, the mean "lifetime" of soft errors is reduced, greatly reducing the chance of double-bit errors, and increasing reliability.

- "Error scrubbing" (going through the entire memory and correcting any soft errors) may be done as a background software task. For instance, the 8086 microprocessor's load string (LODS) instruction can consecutively read all addresses in RAM. Any soft errors will be corrected. Scrubbing further increases system reliability.

- Error logging may be used to detect hard errors. (A soft error is seen once when the affected word is read and is then corrected, while a hard error is seen again and again.) An error logger shows a consistent pattern if a hard error is present in a particular word. A system may be configured to



2. The 8206 requires no control logic or timing inputs to perform read-with-correction cycles.



3. The 8206 can correct both data bits and check bits.

generate an interrupt when the 8206 detects an error.

This last advantage allows the operating system to re-read the address where the error occurred. If the same error re-occurs, it is assumed to be a hard error, and while the system can continue to function, maintenance is indicated. The operating system may mark that page of memory as "bad" until its PC card

Memory Technology: Error-correction chip

has been serviced. Alternatively, the memory system may reconfigure itself and map the bit where the hard error occurred to a spare dynamic RAM whenever the affected memory page is accessed.

When a correctable error occurs during a read cycle (Fig. 3), the system's dynamic RAM controller (or CPU) examines the 8206 ERROR and CE outputs to determine if a correctable error occurred. If it did, the dynamic RAM controller (or CPU) forces R/\overline{W} low, telling the 8206 to latch the generated syndrome and drive the corrected check bits onto the SYO/CBO/PPO outputs. The corrected data is already available on the DO/WDI pins. The dynamic RAM controller then writes the corrected data and check bits into memory. Once again the 8206's dual buses allow this cycle to be implemented without special bus transceivers.

The 8206 may be used to perform read-modify-writes in one or two RAM cycles. If it is done in two cycles, the 8206 latches are used to hold the data and check bits from the read cycle to be used in the immediately following write cycle.

Write cycle corrections

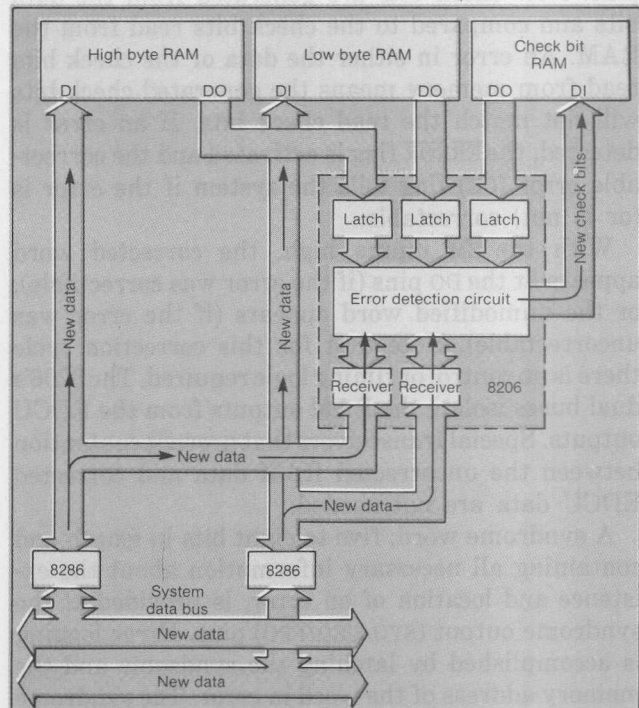
For a full-word write (Fig. 4) where an entire word is written to memory, data are written directly to the RAM. This same data enter the 8206 through the DO/WDI pins where five to eight check bits are generated. The check bits are then sent to the RAM through the SYO/CBO/PPO pins for storage along with the data word.

A byte write (Fig. 5) is implemented as a read-modify-write cycle. Since the Hamming code works only on entire words, to write one byte of the word, it is necessary to read the entire word to be modified, perform error correction, merge the new byte into the old word inside the 8206, generate check bits for the new word, and write the whole word plus check bits into RAM.

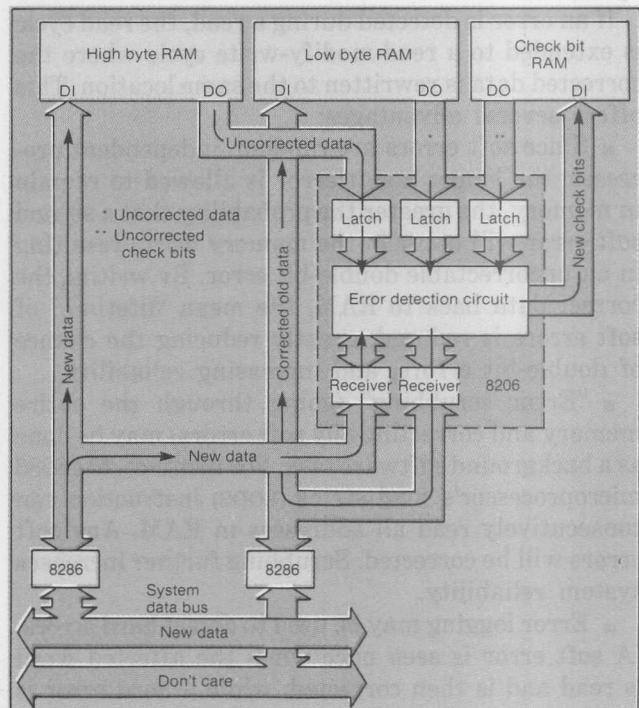
Error correction on the old word is important. Suppose a bit error occurs in the half of the old word that was not changed. This old byte would be combined with the new byte, and check bits would be generated for the whole word, including the bit in error. The bit error now becomes "legitimate"; no error will be detected when this word is read, and the system may crash. Obviously, it is important to eliminate this bit error before new check bits are generated.

The 8206 may alternatively be used in a "check-only" mode with the correct (\overline{CRCT}) pin left inactive. With the correction facility turned off, the delay of generating and decoding the syndromes is avoided, and the propagation delay from memory outputs to 8206 outputs is significantly shortened. In the event of an error, the 8206 activates the \overline{ERROR} flag to the

CPU or dynamic RAM controller, which can then perform one of several options: lengthen the current cycle for correction, restart the instruction, perform a diagnostic routine, or activate the \overline{CRCT} input to enable error correction. Even with the \overline{CRCT} pin



4. The 8206 generates check bits and writes them to memory.



5. The "new data" byte is supplied by the CPU, while the 8206 supplies the corrected old byte. The 8206 also generates new check bits.

inactive, the 8206 generates and decodes the syndrome bits, so that data may be corrected rapidly if the $\overline{\text{CRCT}}$ is activated.

Multiple 8206 systems

A single 8206 handles eight or 16 bits of data and five or six check bits, respectively. Up to five 8206's can be cascaded for 80-bit data words with eight check bits. When cascaded, one 8206 operates as a master, and all others work as slaves (Fig. 6).

As an example, during a read cycle in a 32-bit system with one master and one slave, the slave calculates "partial parity" on its portion of the word and presents it to the master through the partial-parity output (SYO/CBO/PPO) pins. The master receives the partial parity at its partial-parity input (PPI/POS/NSL) pins and combines the partial parity from the slave with the parity it calculated from its own portion of the word to generate the syndrome. The syndrome is then returned from the master to the slave for error correction.

The 8206 uses a modified Hamming code which was optimized for multi-chip EDCU systems. The code is such that partial parity is computed by all 8206's in parallel. No 8206 requires more time for logic propagation than any other, hence no single device becomes a bottleneck in the parity operation.

The 8206 is easy to use with all kinds of dynamic RAM controllers. Because of its dual-bus architecture, the amount of control logic needed is very small.

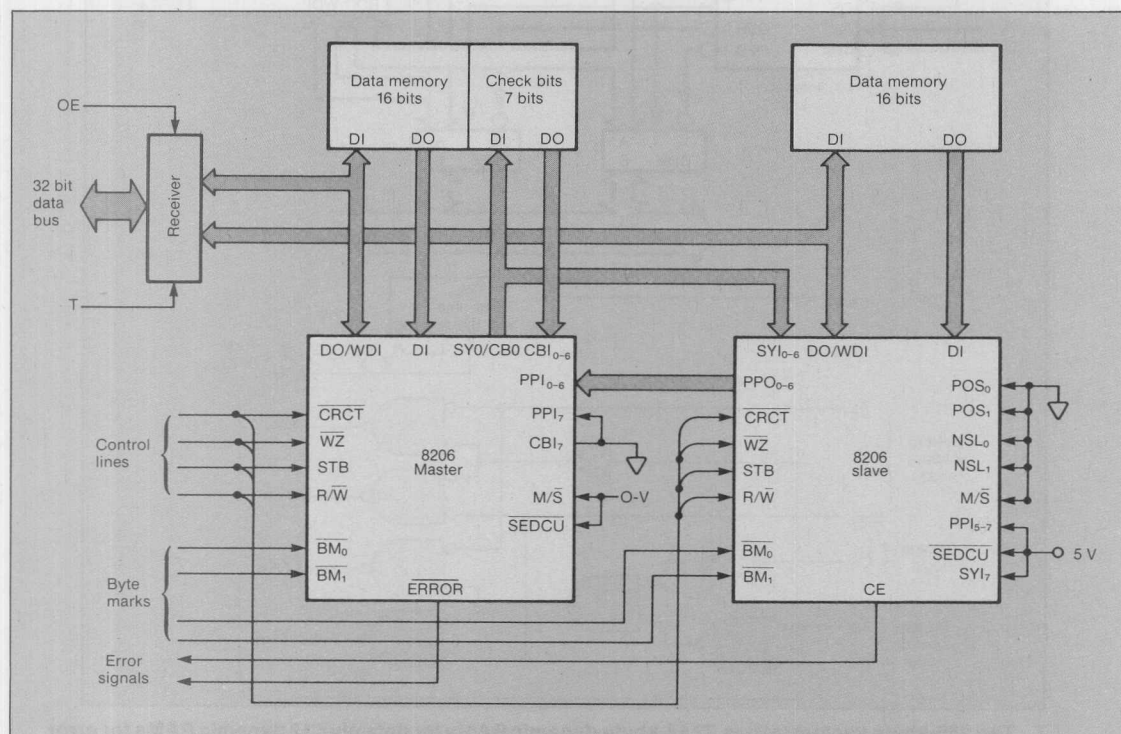
Figure 7a shows a memory design using the 8206 with Intel's 8203 64-kbit dynamic RAM controller and 2164 64-kbit dynamic RAM. As few as three additional ICs complete the memory control function (Fig. 7b).

For simplicity, all memory cycles are implemented as single-cycle read-modify-writes (Fig. 8). This cycle differs from a normal read or write primarily in when the RAM Write Enable ($\overline{\text{WE}}$) is activated. In a normal write cycle, $\overline{\text{WE}}$ is activated early in the cycle. In a read cycle, $\overline{\text{WE}}$ is inactive.

A read-modify-write cycle consists of two phases. In the first phase, $\overline{\text{WE}}$ is inactive, and data are read from the RAM; for the second phase, $\overline{\text{WE}}$ is activated and the (modified) data is written into the same word in the RAM. Dynamic RAMs have separate data input and output pins so that modified data may be written, even as the original data is being read. Therefore, data may be read and written in only one memory cycle.

In order to perform read-modify-writes in one cycle, the 8203 dynamic RAM's CAS strobe must be active long enough for the 8206 to access and correct data from the RAM, and write the corrected data back into RAM. CAS active time (t_{CAS}) depends on the 8203's clock frequency. The clock frequency and dynamic RAM must be chosen to satisfy:

$$t_{\text{CAS(min)}}^{8203} \geq t_{\text{CAC}}^{\text{RAM}} + \text{TDVQV}^{8206} + \text{TQVQV}^{8206} + t_{\text{DS}}^{\text{RAM}} + t_{\text{CWL}}^{\text{RAM}}$$

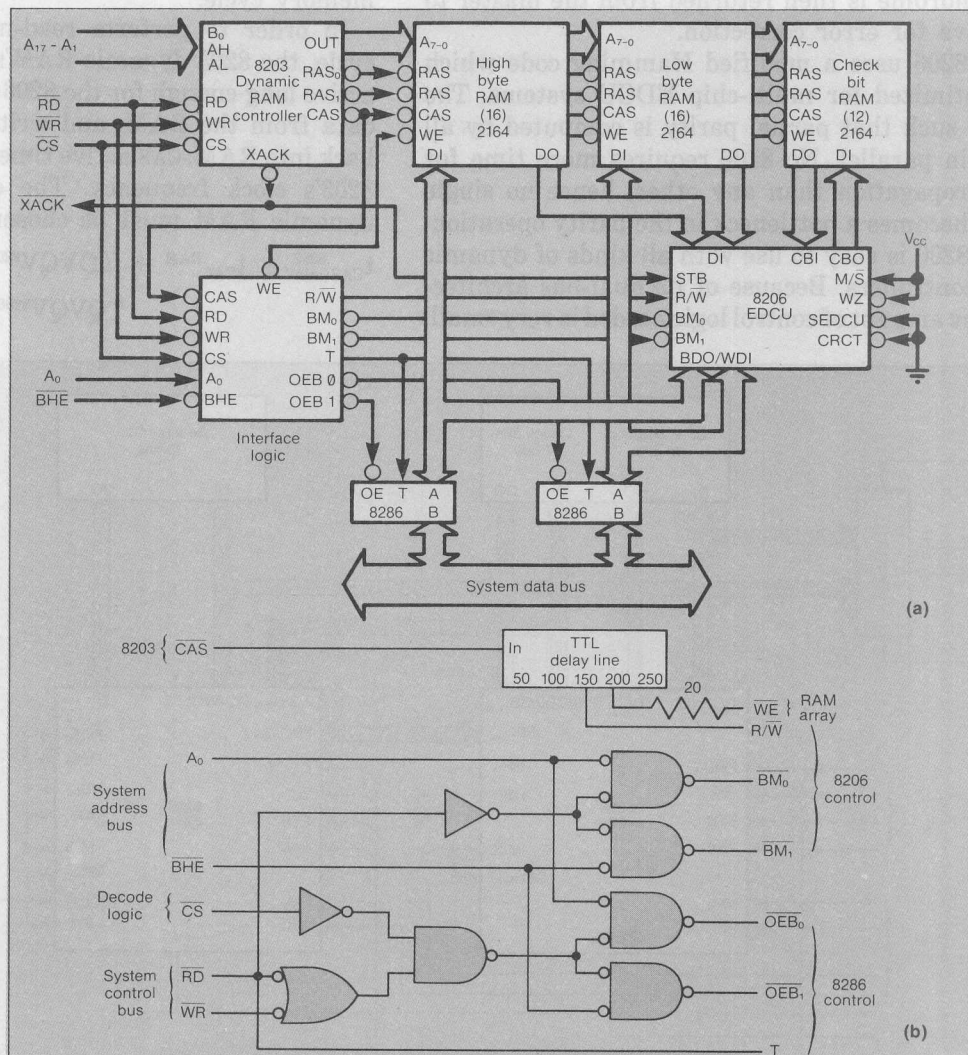


6. No additional logic is required for this 32-bit master-slave system. The slave calculates partial parity on its half of the data, and the master determines which of the 32 data bits and 7 check bits is in error.

Table 3. Syndrome decoding identifies and corrects all single-bit errors.

Syndrome bits	0 0				1	0	1	0	1	0	1	0	1	0	1	0	1	0	1
	7	6	5	4	3	0	0	0	0	1	1	1	1	0	0	0	0	1	1
0 0 0 0	N	CB0	CB1	D	CB2	D	D	18	CB3	D	D	0	D	1	2	D			
0 0 0 1	CB4	D	D	5	D	6	7	D	D	3	16	D	4	D	D	17			
0 0 1 0	CB5	D	D	11	D	19	12	D	D	8	9	D	10	D	D	67			
0 0 1 1	D	13	14	D	15	D	D	21	20	D	D	66	D	22	23	D			
0 1 0 0	CB6	D	D	25	D	26	49	D	D	48	24	D	27	D	D	50			
0 1 0 1	D	52	55	D	51	D	D	70	28	D	D	65	D	53	54	D			
0 1 1 0	D	29	31	D	64	D	D	69	68	D	D	32	D	33	34	D			
0 1 1 1	30	D	D	37	D	38	39	D	D	35	71	D	36	D	D	U			
1 0 0 0	CB7	D	D	43	D	77	44	D	D	40	41	D	42	D	D	U			
1 0 0 1	D	45	46	D	47	D	D	74	72	D	D	U	D	73	U	D			
1 0 1 0	D	59	75	D	79	D	D	58	60	D	D	56	D	U	57	D			
1 0 1 1	63	D	D	62	D	U	U	D	D	U	U	D	61	D	D	U			
1 1 0 0	D	U	U	D	U	D	U	D	D	U	U	D	U	D	D	U			
1 1 0 1	78	D	D	U	D	U	U	D	D	U	U	D	U	D	D	U			
1 1 1 0	U	D	D	U	D	U	U	D	D	U	U	D	U	D	U	D			
1 1 1 1	D	U	U	D	U	D	U	D	D	U	D	U	D	U	D	U			

N = No error
 CBX = Error in check bit X (correctable)
 X = Error in data bit X (correctable)
 D = Double-bit error (detected but not corrected)
 U = Uncorrectable multi-bit error



7. The 256-kbyte system (a) has 32 64-kbyte dynamic RAMs for data plus 12 dynamic RAMs for error correction. The dynamic RAMs are controlled by the 8203 dynamic RAM controller while error correction control is supplied by the 8206. Interface logic (b) allows the 8203/8206 system to implement read-modify-write cycles by generating Write Enable (WE) to the RAMs, Read/Write (R/W) to the 8206, and byte-control signals.

The 8203 itself performs normal reads and writes. To perform read-modify-writes, simply change the timing of the \overline{WE} signal. In Fig. 7b, \overline{WE} is generated by the interface logic—the 8203 \overline{WE} output is not used. All other dynamic RAM control signals come from the 8203. A 20- Ω damping resistor reduces the \overline{WE} signal ringing. These damping resistors are included on-chip for all 8203 outputs.

The interface logic generates the R/\overline{W} input to the 8206. This signal is high for read cycles and low for write cycles. During a read-modify-write cycle, R/\overline{W} is first high, then low.

The falling edge of R/\overline{W} tells the 8206 to latch its syndrome bits internally and generate corrected check bits to be written to RAM. Corrected data are already available from the DO pins. No control signals at all are required to generate corrected data. R/\overline{W} is generated by delaying CAS from the 8203 with TTL-buffered delay line. This delay ($t_{\text{DELAY 1}}$) must satisfy:

$$t_{\text{DELAY 1}} \geq t_{\text{CAC}}^{\text{RAM}} + \text{TDVRL}^{8206}$$

The 8206 uses multiplexed pins to output the syndrome word and then the check bits. The R/\overline{W} signal may be used to latch the syndrome word externally for error logging. The 8206 also supplies two useful error signals: $\overline{\text{ERROR}}$ indicates an error is present in the data or check bits; $\overline{\text{CE}}$ tells if the error is correctable (single bit) or uncorrectable (multiple bits).

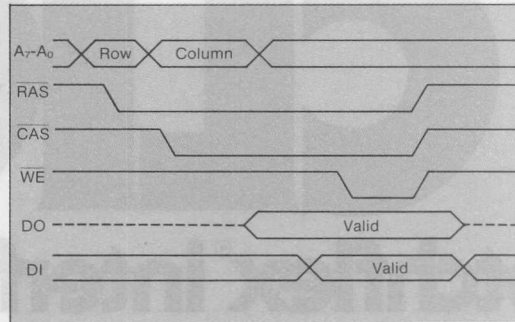
After R/\overline{W} goes low, sufficient time is allowed for the 8206 to generate corrected check bits, then the interface logic activates \overline{WE} to write both corrected data and check bits into RAM. \overline{WE} is generated by delaying $\overline{\text{CAS}}$ from the 8203 with the same delay line used to generate R/\overline{W} . This delay, $t_{\text{DELAY 2}}$, must be long enough to allow the 8206 to generate valid check bits, but not so long that the spec of the RAM (t_{CWL}) is violated. This is expressed by:

$$t_{\text{DELAY 1}} + \text{TRVSV}^{8206} \leq t_{\text{DELAY 2}} \leq t_{\text{CAS(min)}}^{8203} - t_{\text{CWL}}^{\text{RAM}}$$

Errors in both data and check bits are automatically corrected, without special 8206 programming.

Since the 8203 terminates $\overline{\text{CAS}}$ to the RAMs at a fixed interval after the start of a memory cycle, a latch is usually needed to maintain data on the bus until the 8086 completes the read cycle. This is conveniently done by connecting $\overline{\text{XACK}}$ from the 8203 to the $\overline{\text{STB}}$ input of the 8206, latching the read data and check bits inside the 8206.

The 8086, like all 16-bit CPUs, is capable of reading and writing single-byte data to memory. As just explained, the Hamming code works only on entire words, so in byte writes, and new byte and old byte must be merged, and new check bits written for the



8. In all memory cycles, the row and column addresses are strobed to the RAMs by $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$. Sometime after the data out is valid, the control logic in Fig. 7b generates Write Enable ($\overline{\text{WE}}$) to write the data back into the RAMs.

composite word. This is difficult with most EDC chips, but it is easy with the 8206.

Further qualifications on 8206 operation

Referring again to Fig. 7b, the 8206 byte-mark inputs ($\overline{\text{BM}}_0$, $\overline{\text{BM}}_1$), are generated from A0 and BHE, respectively (off the 8086's address bus) to tell the 8206 which byte is being written. The 8206 performs error correction on the entire word to be modified, but 3-states its DO/WDI pins for the byte to be written; this byte is provided from the data bus by enabling the corresponding 8286 transceiver. The 8206 then generates check bits for the new word.

During a read cycle, $\overline{\text{BM}}_0$ and $\overline{\text{BM}}_1$ are forced inactive (i.e., the 8206 outputs both bytes even if 8086 is only reading one). This is done since all cycles are implemented as read-modify-writes, so both bytes of data (plus check bits) must be present at the RAM data in pins to be rewritten during the second phase of the read-modify-write cycle. Only those bytes actually being read by the 8086 are driven on the data bus by enabling the corresponding 8286 transceiver.

The 8286's Output Enables ($\overline{\text{OEB}}_0$, $\overline{\text{OEB}}_1$) are qualified by the 8086's $\overline{\text{RD}}$, $\overline{\text{WR}}$ commands and the 8203's $\overline{\text{CS}}$ command. This serves two purposes: It prevents data bus contention during read cycles and it prevents contention between the transceivers and the 8206 DO pins at the beginning of a write cycle.

Thanks to the use of a 68-pin leadless chip carrier, the 8206 error detection and correction unit is able to implement an architecture with separate 16-pin input and output buses. Thus single-bit error correction may be added to a system with a minimum of control signals or external logic. □

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551
552

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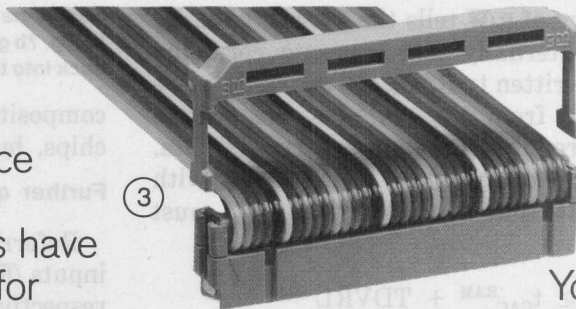
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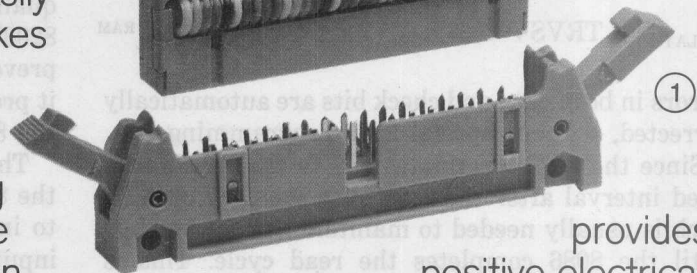
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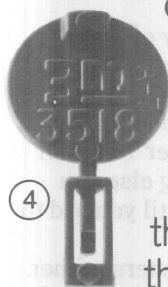
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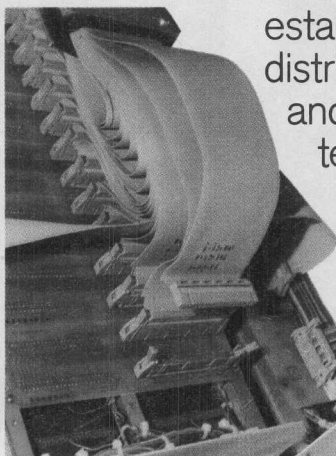


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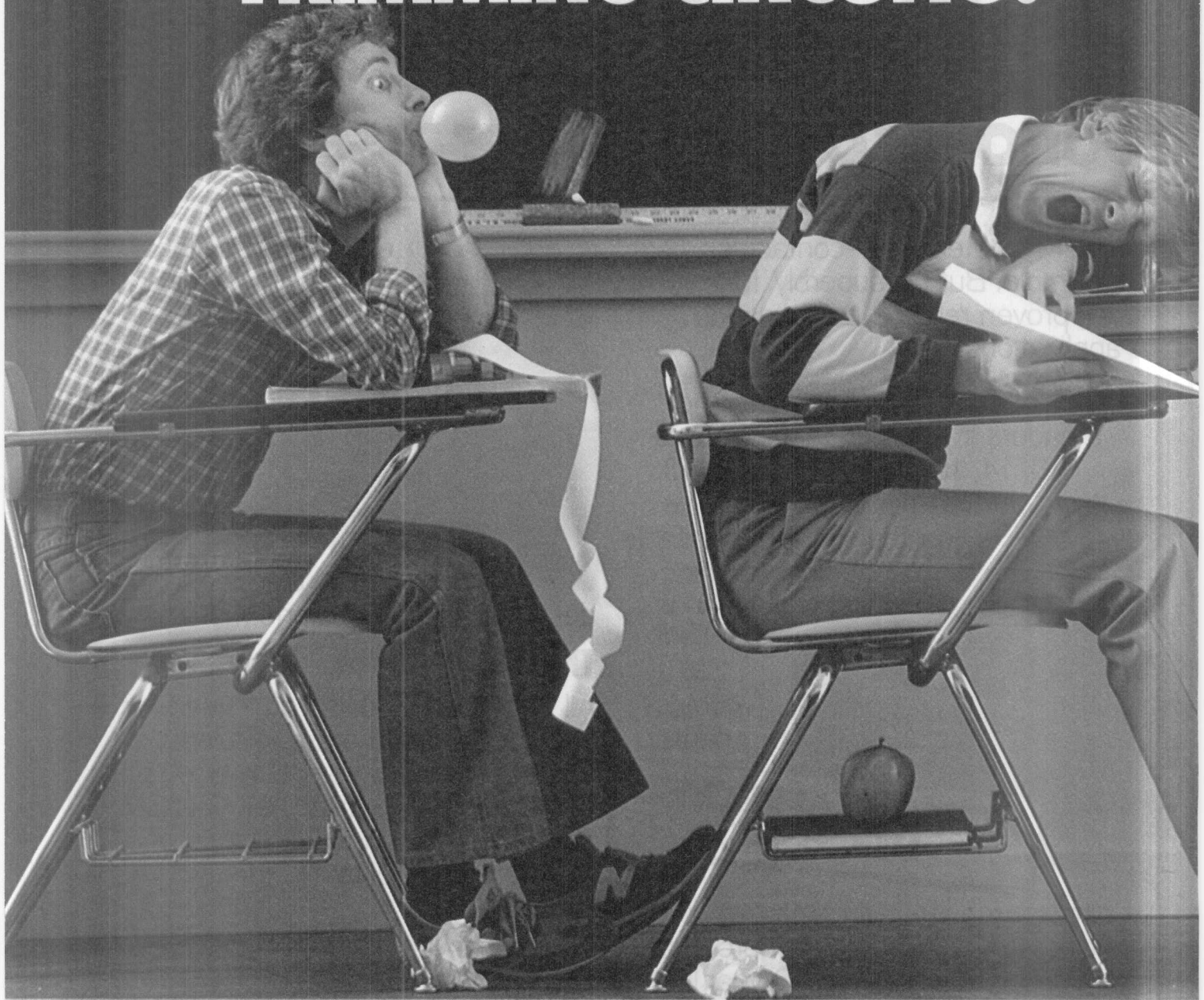
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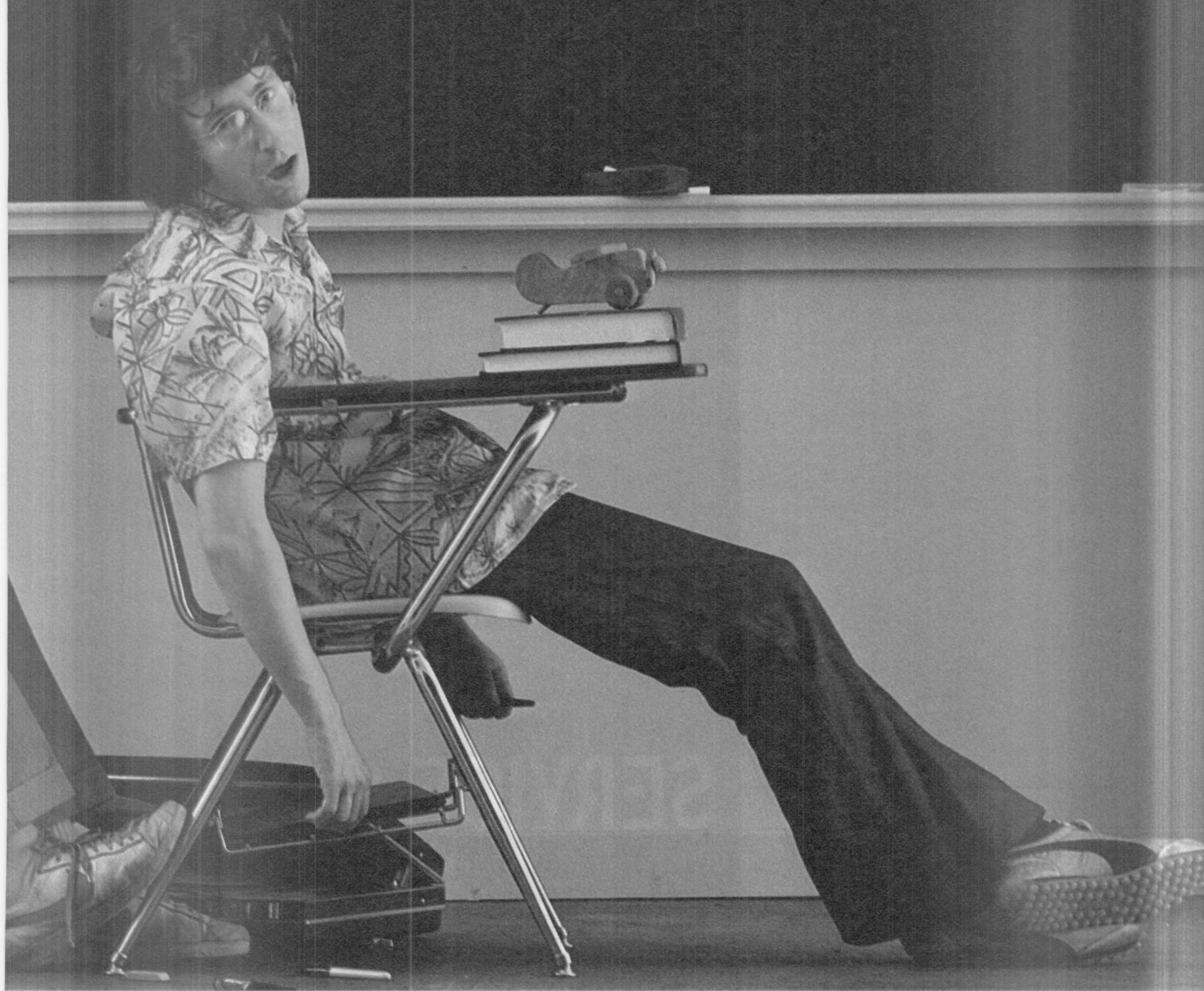
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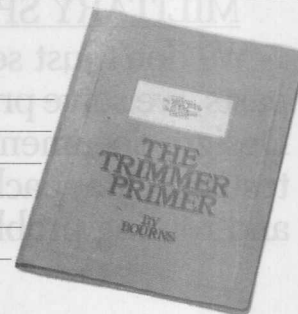
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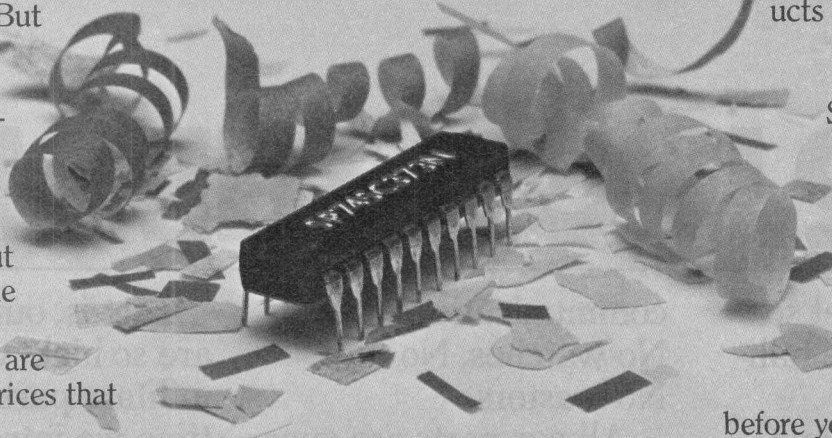
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First-in/first-out buffers are often essential for interfacing computer peripherals and other applications. Now, thanks to a new LSI controller chip, large yet economical FIFOs can be built from standard RAM chips.

Organize RAMs as FIFO buffers with an LSI controller chip

More and more digital systems require large first-in/first-out (FIFO) buffer memories to interface asynchronous subsystems. Now, with the introduction of the Signetics 8X60, large FIFO buffers can be built from high-density RAM chips to form compact and economical systems. The new LSI chip, known as a FIFO RAM controller (FRC), can be used with RAM chips to produce FIFO registers with depths of up to 4096 words (where the words can be of any desired length).

In many applications—examples include peripheral interfacing, data communications and data acquisition—there has been an urgent need for large FIFO buffers (see "Where FIFO Buffer Storage Is Needed"). But, until the introduction of the new controller chip, all the available techniques for building large FIFOs resulted in bulky and expensive systems. For example, FIFO memory chips have been available for several years, but the ICs have very limited capacity—typical storage capability is 64×4 bits. Most FIFO applications require a large number of IC packages to produce the required buffering capability. However, in applications where only a limited amount of buffering is required, LSI FIFO chips may yield the most compact and cost-effective design.

Fitting the FIFO to the task

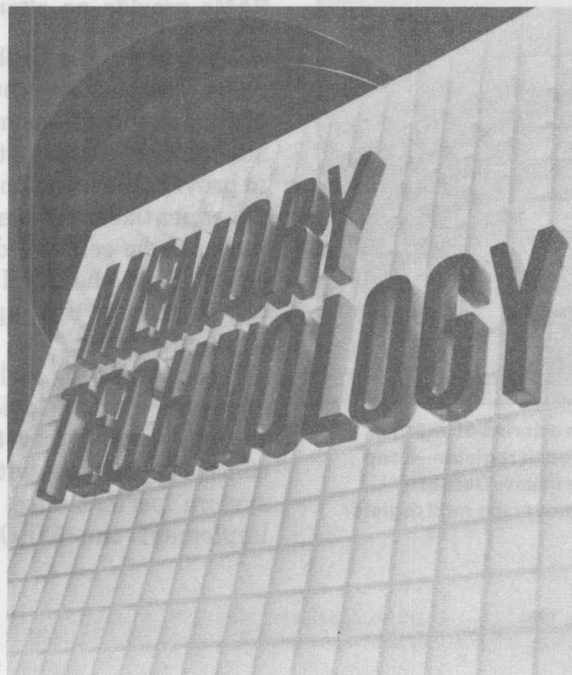
Before examining the FIFO RAM controller in detail, first look at some of the alternatives. This will

help to select the best method for a specific application, and will highlight some of the advantages of the new approach. Of course, regardless of the specific technique employed, the application determines the required buffer size. The memory itself may be built from standard RAMs or from available FIFO memory chips.

For buffer memories in general—though not necessarily for FIFO buffers—semiconductor RAMs are commonly used because they are inexpensive and readily available. The specific memory chip used depends on the buffer size and speed requirements. In most buffer applications, high speed is required, and static RAMs are a popular choice because they tend to be faster and are more easily interfaced than dynamic RAMs. However, even with static RAMs, additional logic is required to address the buffer from both system interfaces. This logic must be capable of generating and keeping track of addresses in the RAM where data are stored. Also the logic must control read and write cycles, and provide status signals to indicate buffer availability.

An advantage of RAMs as buffers, of course, is that they allow random access. Data in the RAM can be directly accessed, and new data can be directly written into any RAM location. A disadvantage of the technique, however, is the need for a sophisticated buffer controller, or for substantial logic in the buffered subsystems to generate addresses and interpret control signals. To avoid undue cost and complexity, RAM-based buffer designs usually must be operated under the

Jeff Seltzer, Applications Engineer, Signetics Corp.
811 East Arques Ave.,
Sunnyvale, CA 94086



control of the systems that are being interfaced. This, in turn, means that they often must be completely filled up by one subsystem before being completely emptied by the other subsystem. The net result of this constraint is that, if large amounts of data are flowing through the buffer, there will be inherent delays that detract from overall system performance. In fact, where real-time response is required, RAM buffering may prove impractical.

Fortunately, RAM buffering isn't essential in most applications—because direct access to the buffer is rarely needed. Most systems require sequential data transfer that can be handled by a straightforward FIFO buffer—and without the need for complex address-control circuitry in either subsystem. With FIFO organization of the buffer memory, information can be read by the receiving subsystem immediately after it has left the transmitting subsystem. The only restrictions on the speed of data transfer are the relative speeds of the subsystems and the capacity of the buffer.

For applications where random access to the buffer is not required, the most common technique

is to use one of several FIFO memory chips that are currently available. However, existing FIFO devices have limited capacity, and are available in only a few specific depth and word-width configurations. The devices have separate data and control lines for input and output operations—which facilitates their use by two independent subsystems. Two asynchronous handshake lines allow read/write control, as shown in Fig. 1 for a typical LSI FIFO chip. Usually, these circuits can sustain quite high I/O clocking rates of about 10 MHz.

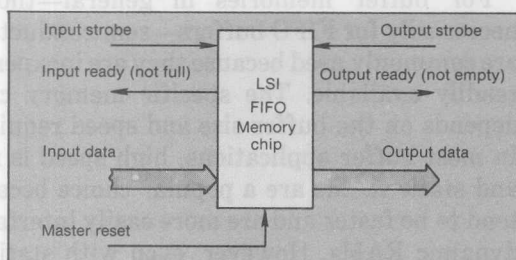
Internally, a FIFO memory circuit consists of a series of storage registers daisy-chained to form a stack as shown in Fig. 2. A flip-flop associated with each register indicates whether that register contains valid data or is empty. Data presented to the FIFO circuit enter the first register and propagate through the stack. Propagation continues until the signal either encounters a full register or reaches the end of the stack. New data can be written into the buffer as soon as the previous entry has been copied forward from the first register. When data are read from the last register, data in all the preceding registers are copied forward by one location. The read operation can be repeated as soon as data in the last register have been replaced.

Construction of a large FIFO memory from FIFO chips—using a configuration such as that shown in Fig. 3—presents two significant problems. Firstly, the chips have only a small capacity. Therefore a large number of chips must be cascaded to achieve depth and/or paralleled to achieve width. Secondly, there is a “fall-through” delay—the time required for a piece of data to propagate from the first register in the FIFO to the last. When FIFO devices are used to build a large buffer, the fall-through time increases as the stack becomes deeper. For large memories the problem becomes quite significant.

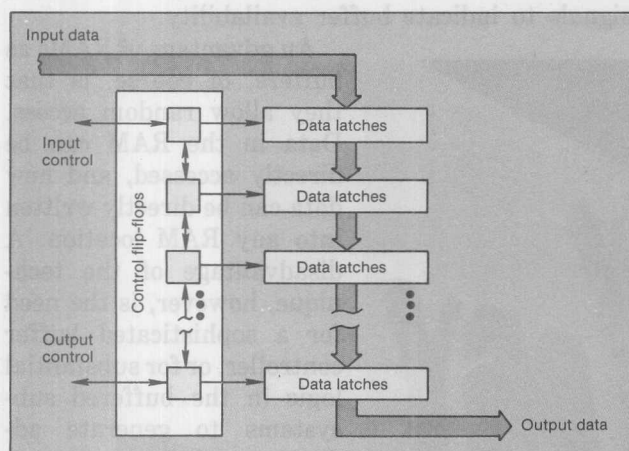
RAMs provide an alternative

Because of the problems that occur when FIFO chips are used to build large buffer memories, alternative solutions must be considered. Most of the alternatives employ standard semiconductor RAMs to provide the data storage. Then, data can be stored in sequential locations in the RAM, and the address lines can be controlled to achieve the desired FIFO effect. Since the RAM controller can directly access any location, this approach eliminates the fall-through problem.

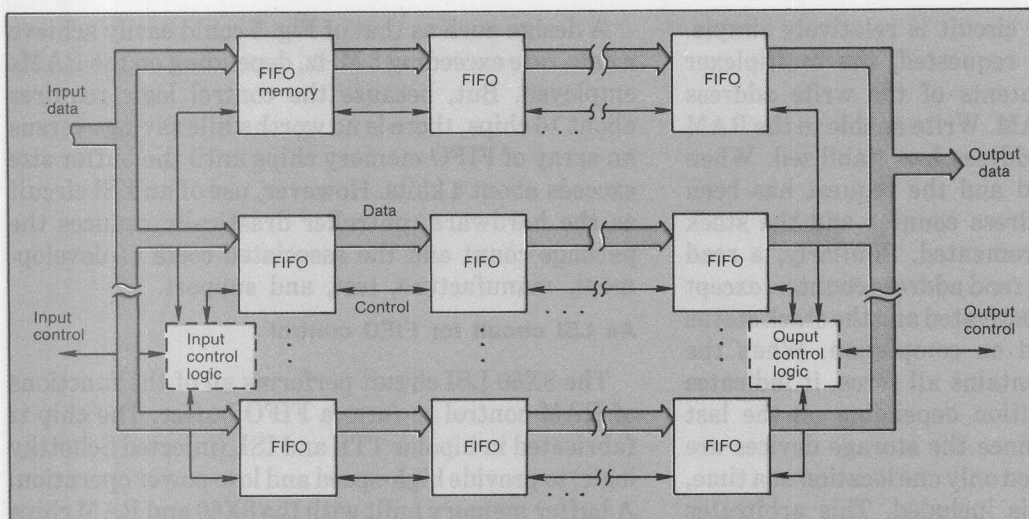
As mentioned earlier, unless the RAMs have dedicated control logic to achieve FIFO operation, the interfaced subsystems will have to provide the control functions—with a consequent loss in overall system performance. There are several ways to implement the FIFO controller. Sometimes, the



1. For a typical FIFO memory chip, an input strobe enters data into the stack, and another strobe later removes the data. Status lines can be used to prevent entry or removal of data if the stack is full or empty, respectively.



2. In a FIFO circuit, data are stored in a series of internal registers. Control flip-flops—one for each register—keep track of how many stack locations are in use. Data in a register are propagated forward whenever the next register is empty.



3. To build a large FIFO buffer, several FIFO memory chips can be cascaded. Depth of the buffer can be increased by connecting more chips in a chain. Width can be expanded by connecting chains in parallel.

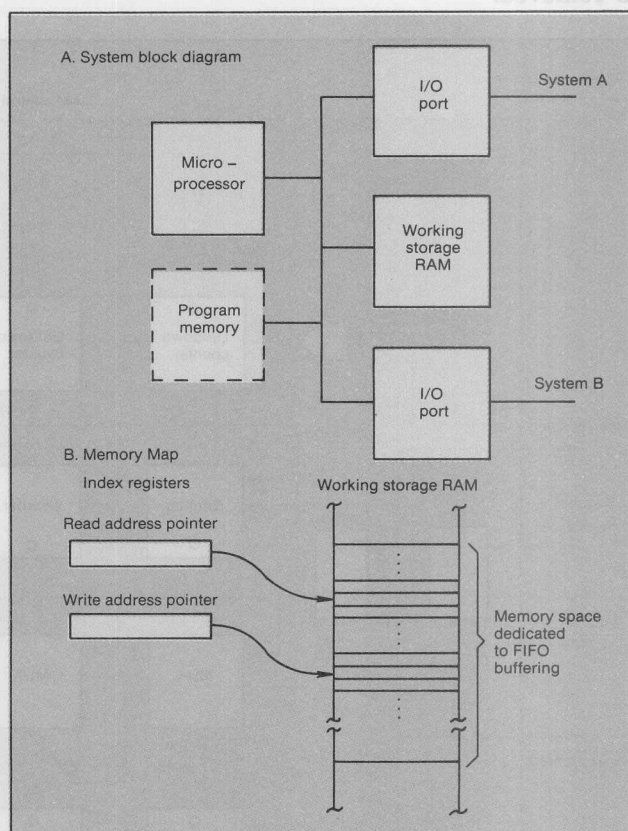
function can be conveniently implemented in software. Since digital systems often use microprocessors, the software approach can minimize the hardware overhead.

The software solution to the FIFO-control problem is quite straightforward. As shown in Fig. 4, two address indices can act as pointers for the next read and write locations in the RAM space dedicated to FIFO buffering. The normal I/O ports of the microprocessor provide access for data to be written into and read from RAM. A software routine increments the associated pointers when a read or write operation is performed—resulting in circular addressing of the data storage in the buffer memory. Comparison of the address pointers determines the full or empty status of the buffer.

While this technique can often be used to manage a FIFO buffer when a microprocessor is present, it is unacceptable for many applications. The slow execution of programmed I/O can result in inadequate performance. Also, the additional burden on the microprocessor can detract from other processing functions, and outweigh the advantages of the FIFO. These problems can be avoided with a hardware implementation of the RAM controller.

A hardware controller for RAMs

The hardware controller shown in Fig. 5 can be built with approximately 16 logic ICs to perform a function similar to the software version. This controller generates 12-bit address pointers and therefore can address up to 4-k words of RAM. The word width is determined solely by the number of RAMs connected in parallel. The control logic can be expanded to support deeper buffers by adding more counter stages.



4. A microcomputer can be programmed to store and retrieve I/O data in FIFO order. With the configuration shown (a), a segment of the microcomputer's memory is reserved as the FIFO buffer (b). The processor maintains two pointers, which index locations where data are to be written and read.

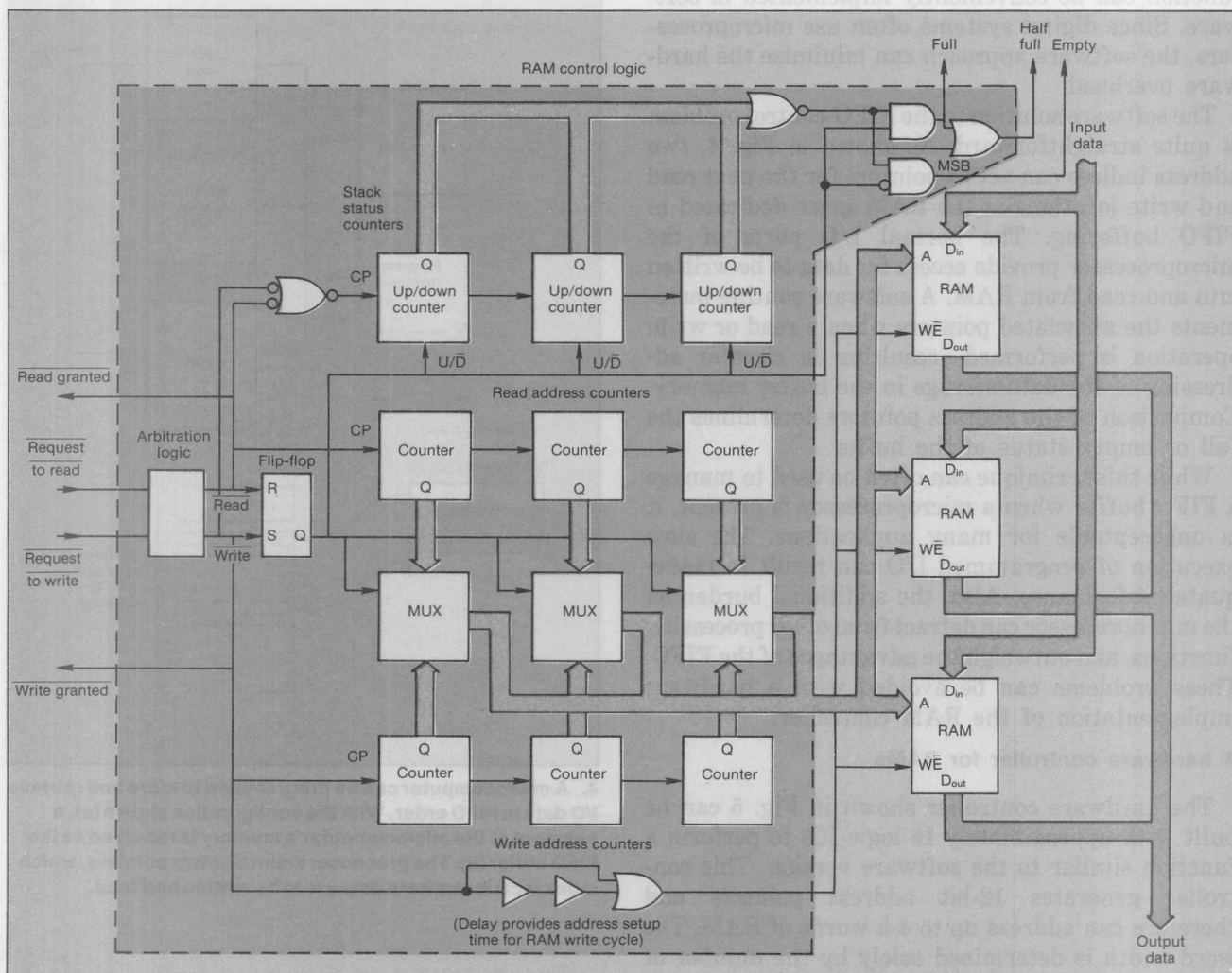
Memory Technology: FIFO controller chip

The operation of the circuit is relatively simple. When a write cycle is requested, the multiplexer selects the current contents of the write address counter to access the RAM. Write enable to the RAM is activated once the address has stabilized. When the cycle has concluded and the request has been removed, the write address counter and the stack status counter are incremented. Similarly, a read cycle proceeds using the read address counter, except that write enable is not activated and the stack status counter is decremented on completion. When the stack status counter contains all zeros, it indicates an empty or full condition depending on the last operation performed. Since the storage devices are RAMs and can be accessed only one location at a time, an arbitration circuit is included. This arbitrates between read and write requests, should they occur concurrently. Once a read or write cycle has begun, it continues until the corresponding request signal is removed.

A design such as that of Fig. 5 could easily achieve a data rate exceeding 5 MHz, depending on the RAMs employed. But, because the control logic requires about 16 chips, there is no worthwhile savings versus an array of FIFO memory chips until the buffer size exceeds about 4 kbits. However, use of an LSI circuit as the hardware controller drastically reduces the package count and the associated costs of development, manufacture, test, and support.

An LSI circuit for FIFO control

The 8X60 LSI circuit performs all of the functions of RAM control to form a FIFO buffer. The chip is fabricated in bipolar TTL and ISL (injected Schottky logic) to provide high-speed and low-power operation. A buffer memory built with the 8X60 and RAM chips competes with arrays of FIFO memory chips for buffer sizes as small as 512 bits (see Fig. 6). Readily available 4-kbit static RAM chips offer high speed and economize on board space for larger capacity

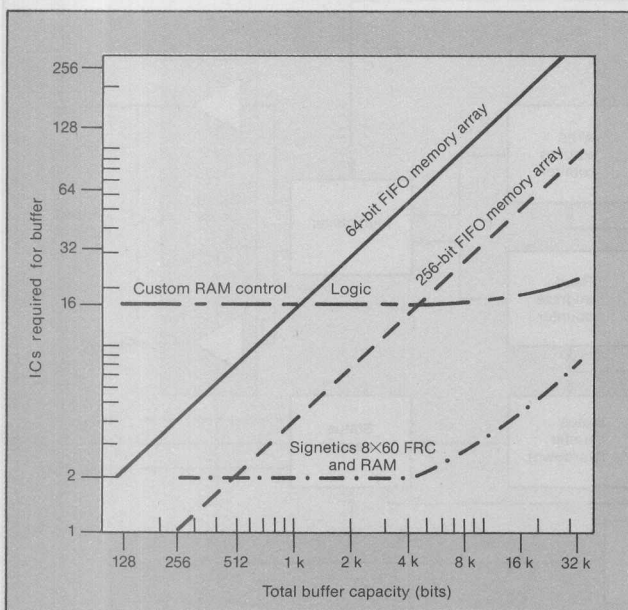


5. Conventional RAM chips can be addressed in FIFO sequence by using this hardware controller. The disadvantage of this method is that the circuit requires about 16 digital ICs plus additional RAM chips.

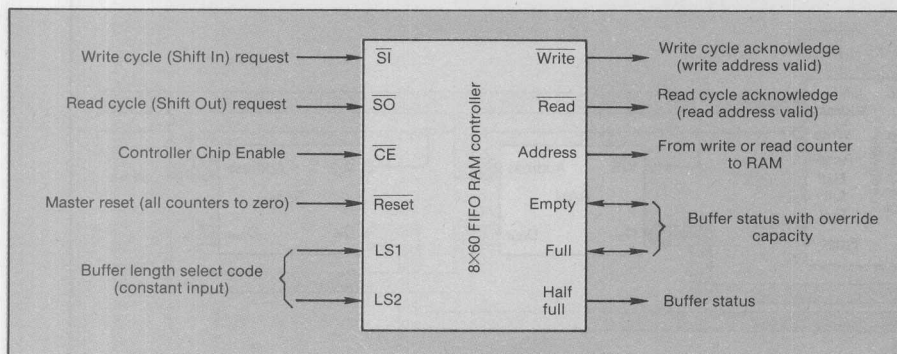
buffers.

The 8X60 provides a unique combination of features. It can control buffers with depths of up to 4096 words and with any width. The width is determined by the type and quantity of RAM devices used. Data rates achievable with this FIFO/RAM

Signal combinations for buffer-length selection			
LS1	LS2	Half length (words)	Full length (words)
L	L	2048	4096
H	L	32	64
L	H	512	1024
H	H	128	256



6. As the size of a FIFO buffer memory increases, the parts count increases rapidly when FIFO chips are used. When RAMs are used, the count climbs more slowly. Use of the Signetics 8X60 provides the most compact system for large FIFO buffers. (These log-log graphs assume the use of RAMs with capacities up to 4-kbits.)



7. Signal connections to the 8X60 RAM controller are shown here grouped by function. Of course, the actual pin connections are arranged in a different sequence. The \overline{SI} and \overline{SO} lines initiate write and read cycles, respectively.

combination can exceed 8 MHz, which competes with current FIFO memories. However, this approach does not suffer the lengthy data fall-through delays associated with FIFO chips.

The pin connections for signals associated with the 8X60 are shown in Fig. 7, while a block diagram of the controller chip is shown in Fig. 8.

The 8X60 controls FIFO buffering by generating the addresses used to access the RAM. Also it interprets control signals from the subsystems that are being interfaced and provides appropriate status information. Separate handshake control lines are used to request either write or read operations. A request for either operation causes the appropriate RAM location to be addressed. Once the address is stable, the corresponding control output acknowledges that the request has been granted. Upon completion of the data transfer to or from the RAM, the request input is removed. This causes the control output, and then the address output, to be terminated.

Write-cycle operation is as follows: When the \overline{SI} (Shift In) request input goes low, the write operation will start—provided the read cycle is not in progress (as determined by the arbitration logic) and provided the stack is not full (as determined by the status signal). Then the write address will appear on the outputs and, after the address has stabilized, the \overline{WRITE} output will go low. When the \overline{SI} input is returned to the high state, the \overline{WRITE} output goes high before the address outputs are disabled. The write-address counter and status counter are then both incremented.

When the \overline{SO} (Shift Out) request input goes low, the read cycle will begin—provided a write cycle is not in progress and the buffer is not empty. The read address will appear on the outputs and the \overline{READ} output will go low. When \overline{SO} is returned high, \overline{READ} goes high. Also the Address outputs are disabled, the read-address counter is incremented, and the status

Memory Technology: FIFO controller chip

counter is decremented.

To prevent the possibility of operational conflicts, arbitration logic ensures that \overline{SI} and \overline{SO} are treated on a first-come first-served basis. If one cycle is requested while the other is in progress, the requested cycle will begin as soon as the current cycle is completed.

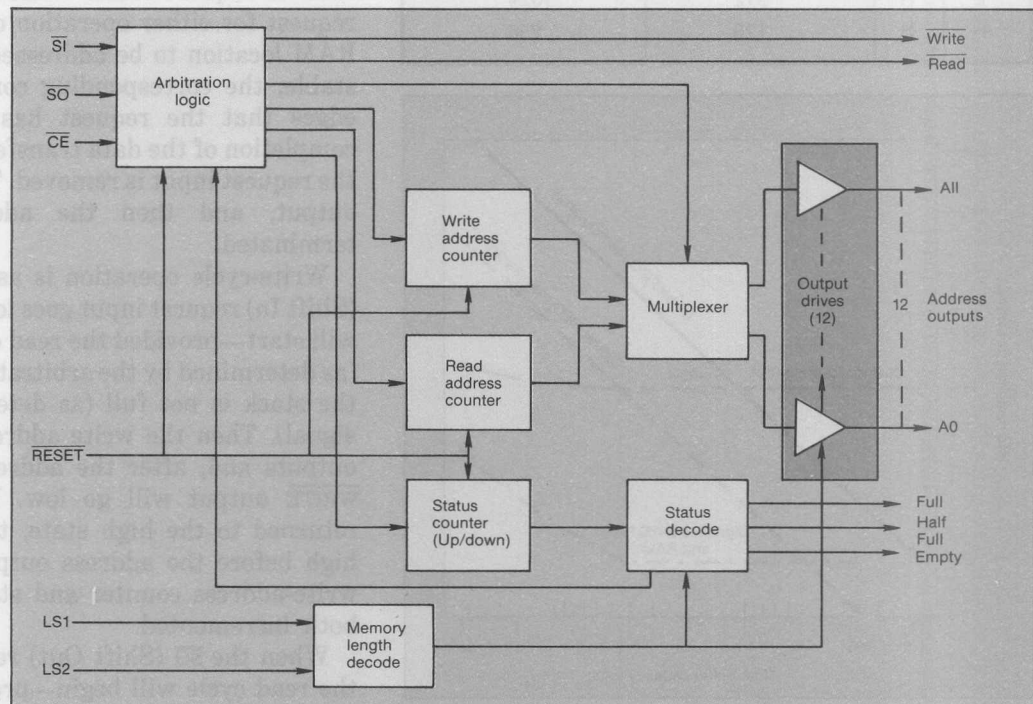
The buffer length of the FIFO memory can be hardware selected via the Length-Select inputs (LS1 and LS2) as shown in the table. When the selected length is less than the maximum available, the unused high-order address outputs are inhibited

(placed in the high-impedance state).

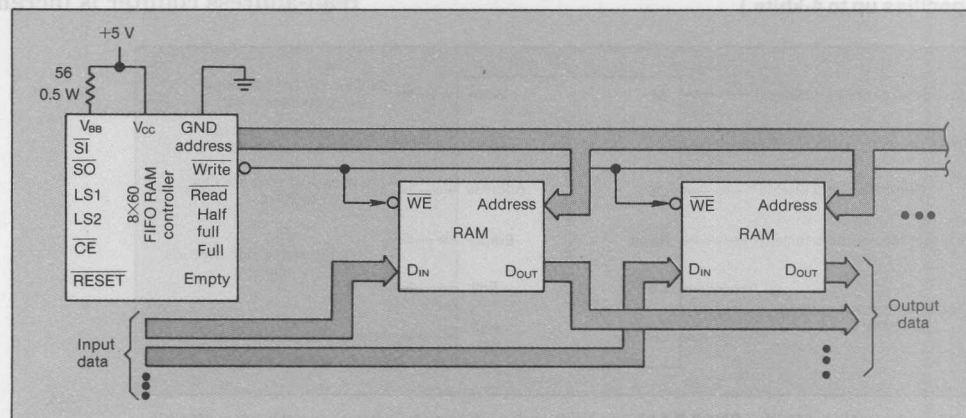
The 8X60 also generates status signals indicating whether the FIFO buffer is empty, full (no more available locations), or at least half-full.

Almost any semiconductor RAM can be used with the 8X60. The device provides control signals that can be used directly to control the Write-Enable (\overline{WE}) input to a RAM (Fig. 9) provided that the address setup time required by the RAM is sufficiently short (no more than 5 ns).

The most convenient way to build a buffer memory around the 8X60 is to use RAMs that have an address



8. The 8X60 controller provides all the functions needed to control RAMs so that they function as FIFO buffers. As shown in this internal block diagram, the LSI circuit generates all necessary addresses and status codes. Arbitration logic establishes priorities in the event of concurrent read and write requests.



9. A FIFO buffer can be built by connecting the 8X60 controller to RAM chips as shown. Several RAMs can be connected in parallel to achieve the desired word width. For this simple configuration, the address space of each RAM equals the desired FIFO buffer length.

Where FIFO buffer storage is needed

Wherever two digital subsystems operate asynchronously, yet must communicate, a first-in/first-out buffer memory may be required. As shown in the diagram, a FIFO buffer can be used to interface two asynchronous subsystems, A and B. Instead of being transferred directly from subsystem A to subsystem B, data are first accumulated in a FIFO buffer from which they are read into subsystem B at a different speed, but in the same sequence.

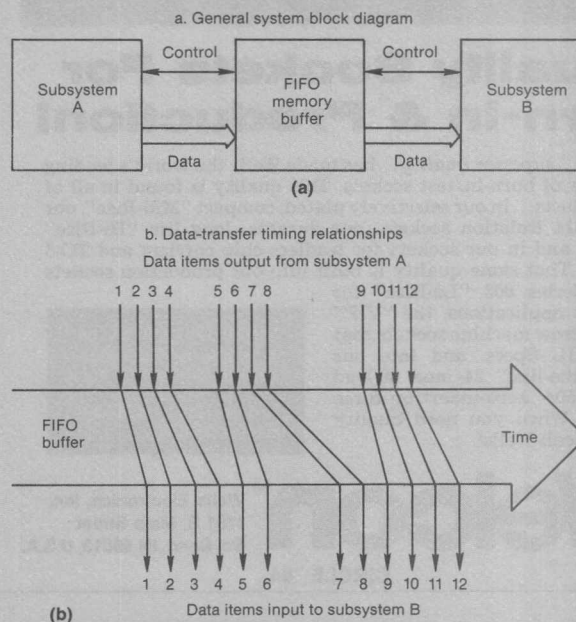
The buffer used must be sufficiently large to hold an entire block of data from the first subsystem (e.g. a complete sector from a disk). Though FIFO memory chips are available, they tend to have limited storage capability (typically 64×4 bits). The new Signetics controller chip meets the need for increased buffer capacity by allowing registers with depths of up to 4096 words to be built from high-density RAM chips.

There are many situations in which the speed of one or more subsystems cannot be controlled by the system designer and where the data rate required by one of the subsystems exceeds the capacity of the other. For example, high-speed peripherals must often be interfaced to computers that have limited channel or memory speed. The data rate of the peripheral may be fixed by mechanical characteristics (such as the rotation speed and recording density of a disk), while the I/O speed of the computer may be limited by memory speed. This type of situation could become more prevalent in the future as transfer rates of peripherals increase due to technological advances.

Another application where FIFO buffers can prove useful is in data-acquisition systems that must monitor and respond to a large number of real-time events. The events may occur at any time including the period during which the processor is retrieving previously stored data. A FIFO buffer can store the events as they occur and present the data to the

computer when it can handle the processing.

Data-communications systems often require buffering. In distributed communication networks, efficient use of the communication channel is important. Stations in the network must be capable of receiving or transmitting messages as soon as the communica-



tion channel becomes available. Use of FIFO buffers for interfacing allows efficient use of the communication channel even during periods when a station's processor is busy. In other data-communications systems, FIFO buffers can optimize use of the channel and processor by allowing messages or sets of messages to be stored and assembled for subsequent transmission.

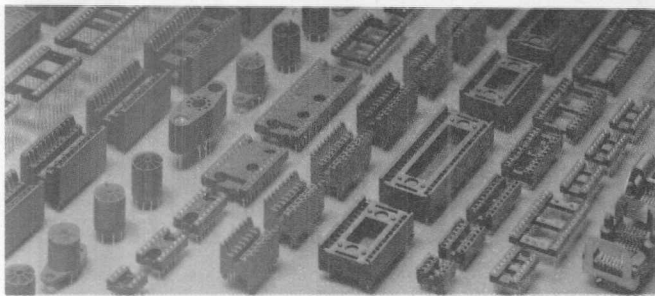
space equal to the desired FIFO buffer depth. The number of devices required is then determined solely by the word width. The buffer can also use RAMs of different sizes, but some design effort will be required to address them using conventional address decoding techniques. In this case, the chip-select decoder itself must be disabled until an I/O operation commences—to provide sufficient address setup time during a write cycle.

Since the 8X60 achieves FIFO operation through simple control of address lines, a number of interesting memory designs and FIFO applications become possible. For example, consider an 8X60 connected to the low-order address lines of a large computer memory. The Chip-Enable (\overline{CE}) input to the 8X60 could be controlled to enable the address outputs and FIFO control operations upon request from the

processor. A large, hardware FIFO memory space would then be available to the system and/or software designer (see Fig. 10).

The arbitration logic in the 8X60 allows it to interface between two asynchronous systems—much like a dual-port memory. However, an important difference is that the RAM may not be immediately available for access upon request if the opposing cycle is in progress. For applications that cannot tolerate the arbitrary delay of one cycle before a request is granted, data latches may be used to interface the RAM input and/or output data, thus forming a data pipeline.

One solution for implementing a full input and output pipeline is shown in Fig. 11. The block diagram also shows where time-delay circuitry could be included, if necessary, to provide sufficient access



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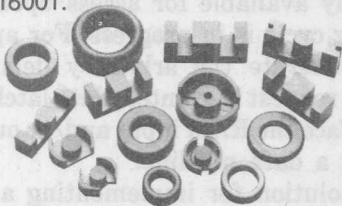
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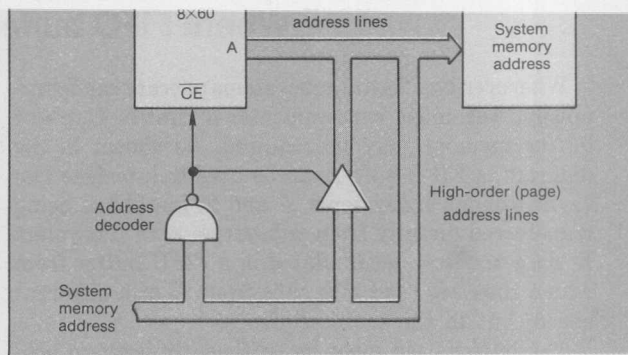
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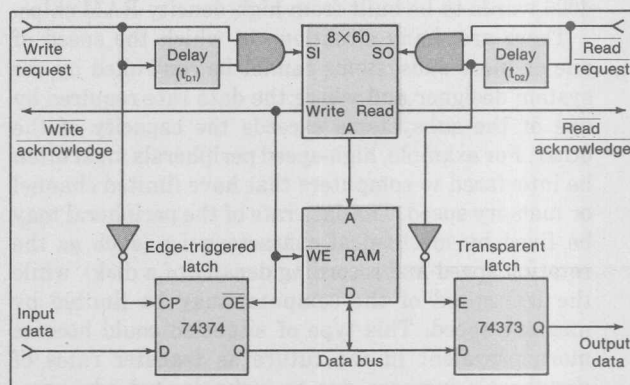
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10. To use a segment of a large system memory as a FIFO buffer, you can connect the 8X60 to the low-order address lines of the memory. In this way, a page of the computer's memory is dedicated as a FIFO buffer. The \overline{SI} and \overline{SO} inputs to the 8X60 can be derived from the system's read/write control lines.



11. Data pipeline latching avoids system delays when data must be written into or read from the buffer instantaneously. The scheme requires extra logic, and time delays may have to be included to allow access time for data transfer to and from the RAM. Delay t_{D1} maintains an adequate write pulse for the RAM; delay t_{D2} provides RAM address access and latch set-up times.

time for data transfer into and out of the RAM.

Since the 8X60 does not actually handle the buffered data, any interfacing to the RAM data lines should be designed to suit the particular application. With an interface as shown in Fig. 11, a data word can be written or read immediately upon request, while the actual data transfer to or from the FIFO buffer may occur at any time thereafter.

As we've seen, large buffer memories can be extremely useful in system design. The 8X60 controller, coupled with standard RAMs, provides designers with the most cost-effective and straightforward method for building large FIFO buffers. □

How useful?

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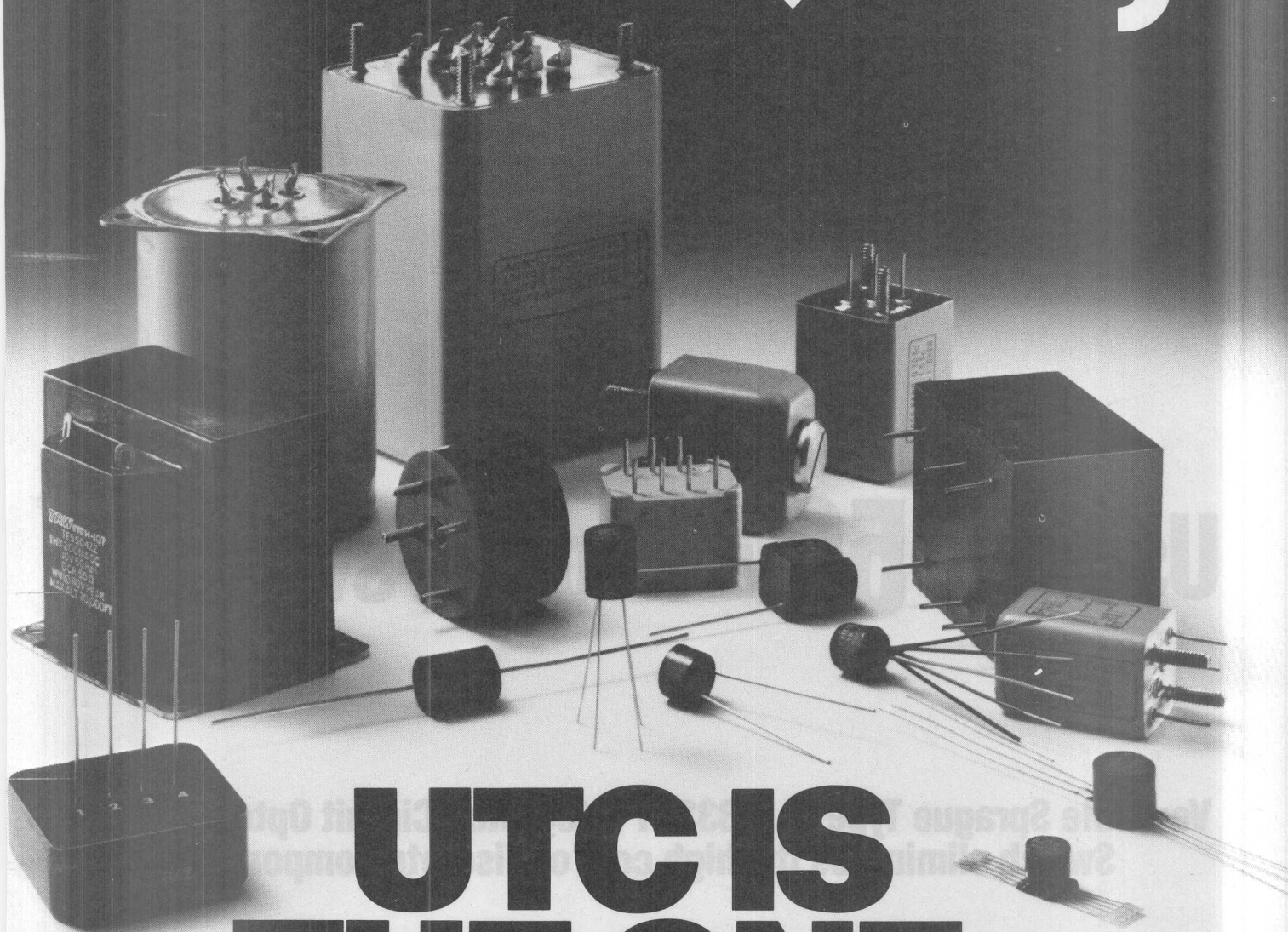
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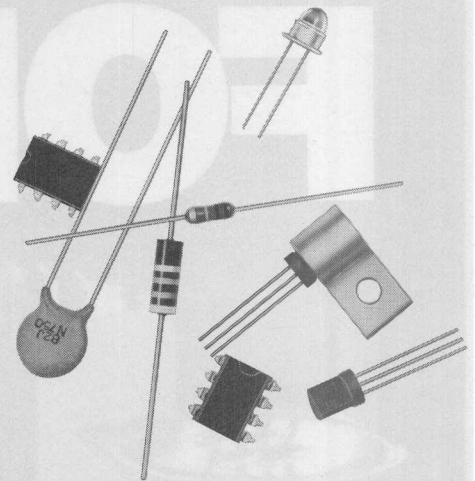
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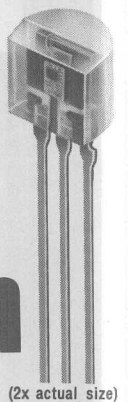
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The greater capacity and smaller size of recent Winchester disk drives have reopened the backup question. A 1/4-in. streaming tape cartridge drive with a data-transfer rate of 90 kbytes/s, is prepared for the task.

Intelligent streaming tape unit ready to back up Winchesters drives

At last a 1/4-in. streaming tape drive has arrived to attack the Winchester backup problem. Capacity, packaging, and reliability improvements in Winchester technology can be negated if no effective data backup is available to system designers. Until now, uncertainty in providing a reliable and cost-effective backup in the 20-to-80-Mbyte range has been a major obstacle to small-system designers.

The requirements for backup are stringent: such a device must be low in cost yet equal to the Winchester disk drive in performance and ease of use. The only solution that can be delivered today to meet all these requirements is the Sidewinder 1/4-in. streaming tape drive.

Originally, floppy disks could handle the job, but that is no longer true, because of the recent increase in capacity and reductions in size of the latter. The Sidewinder steps into that breach, opening up the use of a streaming tape drive for backup, thanks to its impressive qualifications:

- A data-transfer rate of 90 kbytes/s, to handle the majority of system timing requirements effectively and not tax system buffers.

- A host interface designed for a variety of microprocessor and mini-computers. It includes an 8-bit bidirectional bus and control and status lines. With just two software instructions, read and write, the drive can appear to the user as a 20-Mbyte first-in,

first-out (FIFO) buffer.

- Controller software that eliminates time-consuming design work, tape formatting, error processing, and motion controls become transparent to the host system.

- Intelligence, in the form of a microprocessor, that accommodates DMA I/O system architectures and relieves the host of the need to control tape-processing parameters.

- A tape utilization efficiency—the ratio of the length of the data record to that length plus the length of the gap between records—of 97%.

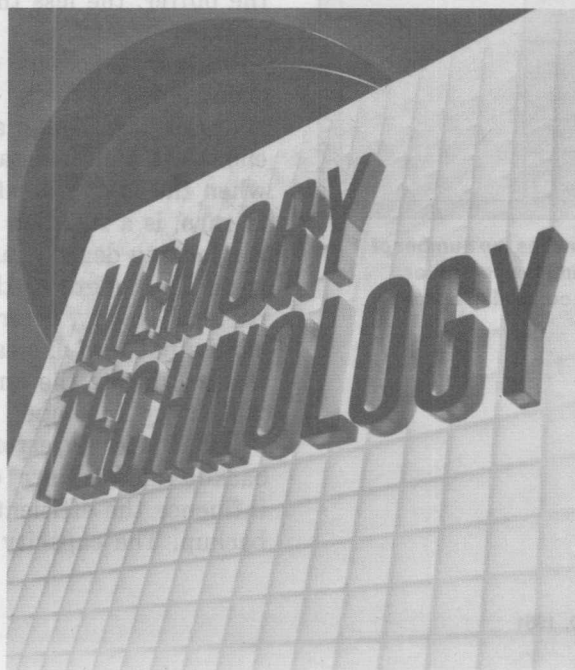
- Hard error rates of 1 in 10^8 and 10^{10} , commensurate with those of Winchester disk drives.

A comparison of the various backup solutions puts the Sidewinder in perspective (see Table 1). The Sidewinder relies on a standard 450-ft 1/4-in. cartridge and delivers a formatted capacity of 20 Mbytes at a transfer rate of 90 kbytes/s. The next option, the 1/4-in. start/stop cartridge drive, requires multiple media insertions, has a formatted capacity of 8.6 Mbytes, and costs more per given capacity. What's

more, it loses to the Sidewinder in all the other performance and operational considerations shown in Table 1.

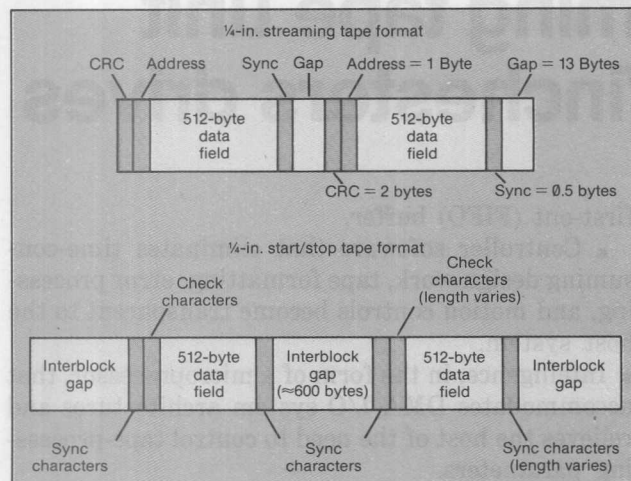
Another factor to consider when comparing streaming and stop/start 1/4-in. drives is that the streaming tape format separates data fields with gaps of 2 to 13 bytes. The start/stop cartridge drives rely on 600-byte blocks, for a tape utilization factor of 45%. On the other hand, the streaming format is about 97% efficient at a 20-Mbyte formatted and a

Wes Theriault, Vice President of Marketing
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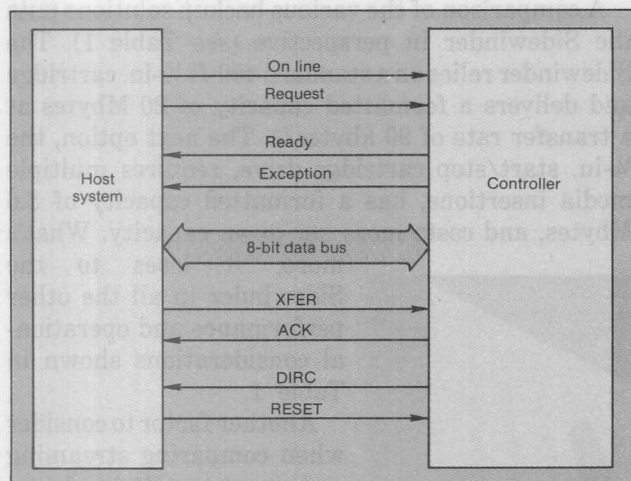


The floppy-disk drive cannot support disk drives of more than 15 Mbytes, which is hardly sufficient for mass compilation and storage of data. Furthermore, the total recording time of both 5¼ and 8-in. floppies negates their use for Winchester backup.

The major concerns in integrating a tape subsystem into a system design are matching the disk,



1. Whereas the 1/4-in. streaming tape format separates data fields with gaps of 2 to 13 bytes, a conventional 1/4-in. start/stop drive may consume up to a 600-byte interblock gap. These gaps translate into a 97% tape utilization with streaming and only about 45% for start/stop operation.



2. The host interface hardware minimizes the number of interconnections between the host and the controller. Communications between the two is controlled by four programmed I/O (PIO) lines.

Another serious consideration is the use of programmed I/O (PIO) or direct memory access (DMA). If a small, single-user computer is the goal, a PIO channel can be used without purchasing a fast peripheral subsystem. Conversely, if the final goal is a fast multiuser system, DMA will generally be the choice. Both PIO and DMA host parameters will be dealt with below.

The main consideration for the disk drive is to match its requirements with those of the host computer system. Overall, the capacity and speed of the disk must meet or exceed the operational needs of the CPU. The goals for tape backup mean that it too must meet these same stringent parameters.

Track seek time and rotational latency time must be taken into account as simple operational parameters. Bit packing density and error-recovery procedures, on the other hand, contribute to the overall performance of the drive.

For example, if the disk seeks out tracks slowly and has a slow rotational latency, low bit packing density, low capacity, and few error-recovery procedures, then a fast, high-capacity tape subsystem will be inefficient and too costly. What's more, the tape drive's performance will suffer because the system will not be able to support the speed of the tape drive.

Selecting a tape drive

In selecting a tape drive, the key factors are transfer rates, capacity, and reliability. The tape's record size must match well with the disk's file size and provide the needed data access when the data are on tape. Tape speed and bit packing density directly translate into how fast the system will put data down on the tape. Buffering, too, affects how fast the host can deliver data to the tape: The larger the buffer, the less the bus or the computer's core memory is tied up.

If the transactional speed matches the computer's speed, then capacity is the next parameter to be addressed. Although a backup system may be fast enough to handle data, its basic purpose is defeated when the media must be changed often. Capacity, in turn, is a function of the length of the tape, the bit packing density, and the size of the interrecord gaps. The length of the tape, coupled with the bit packing density, determines how much data overall can be put into one cartridge. The interrecord gap, in turn, limits the amount of formatted data that will fit on the tape.

Data buffering, error-recovery procedures, and the backup method are operational parameters that influence the efficient interface of CPU, disk, and backup. The capacity of subsystem buffering will

Table 1. Possible Winchester backups

Device	Formatted capacity (Mbytes)	Cost/Mbyte (in 500-unit lots)	Number of media required*	Total media cost	Recording time* (min.)	Operator involvement
Sidewinder 1/4-in. streaming tape cartridge	20.0	\$ 31	1	\$30	4 (90 in./s) 12 (30 in./s)	One media insertion
1/4-in. start/stop tape cartridge	8.6	\$140	3	\$90	60 (30 in./s)	Multiple media insertion
8-in. floppy-disk drive, dual-sided, double-density	1.3	\$400	16	\$80	34	Multiple media insertion
5 1/4-in. floppy-disk drive, dual-sided double-density	0.409	\$685	50	\$150	100+	Multiple media insertion
Fixed/removable disk drive	6.4 fixed 6.4 removable	\$300 removable	4	\$500	4	Multiple media insertion
Removable disk cartridge drive	8.8	\$180	3	\$375	4	Multiple media insertion

*For 20 Mbytes

Table 2. Commands of the Sidewinder's controller

Command	Command code	Description
Select	000MMMMM	Determines which tape drive is accessed. Up to four drives can be daisy-chained.
Position	001XXMMM	Instructs the tape drive to handle all tape positioning internally. Now the host system need not recognize and act on tape-positioning commands.
Write data	010XXXXX	Initiates the writing of data.
Write file mark	011XXXXX	Lays a GCR file mark on the tape for later access to a particular file.
Read data	100XXXXX	Reads data; includes retries and transfers to the host of data that contain hard errors so that the host can determine and correct them.
Read file mark	101XXXXX	Permits access to any file number off line.
Read status	110XXXXX	Provides the ability to monitor the performance of the drive, showing how many times data blocks had to be rewritten or reread. This auditing feature helps to indicate when a tape is wearing out.

M = Modifier bit

X = Not used (must be 0s)

Memory Technology: 1/4-in. streaming tape backup

determine whether or not the CPU's internal memory will be used or if host buffering is required. Error-recovery procedures provide the parameters for hard and soft-error recovery circuitry needed in the host.

The user can decide if mirror-image, individual data-file, or transactional backup best fits his needs. Since most backup tape systems are relatively new and not many models are on the market, the question really becomes, What kind of data management can the user actually accomplish? Streaming systems,

such as the Sidewinder, offer the user both mirror-image and data-file management.

Factors influenced by the tape cartridge

If the backup is used continually, reliability is paramount. That means that the tape must run at a constant speed, the tape tracks must always align with the head, and the tape must be kept free of dust and other foreign matter. In the case of a 1/4-in. cartridge tape drive, the tape itself plays a very important role in the overall data reliability.

Making the most of tape recording technology

To achieve high performance, minimum maintenance, and high reliability, the Sidewinder 1/4-in. streaming tape drive incorporates advanced tape recording technology usually found in high-performance 1/2-in. reel-to-reel drives.

Unique among 1/4-in. drives, it erases with an ac signal, permitting light writing to be employed. That in turn makes possible extremely high-density recording with existing head technology. Light writing means that the tape is not saturated. Conventional 1/2-in. NRZI tape drives record in a saturation mode, but large tape drives using 6250-bit/in. group-code-recording (GCR) of the IBM 3420 type cannot achieve the required density on existing tape with saturation recording. Therefore they operate with a much lower output from the read head than conventional drives. That presents a problem, in that most conventional machines erase with dc and the dc signal has an ambient noise level that would be too close to the level of the read/write signal for reliable operation. Consequently, most manufacturers have gone to ac erasing on large 6250-bit/in. units. (As can be verified by any high-quality audio recorder, ac erasing significantly improves the signal-to-noise ratio over a dc erase.)

The Sidewinder employs two other important recording techniques. A third-order phase-locked loop follows instantaneous speed variations (ISV) that are inherent in the cartridge, and a 4-to-5-bit run-length limited coding minimizes bit shifts by avoiding worst-case data patterns (see figure).

One of the principle advantages of the run-length limited codes in this particular case is that no data stream ever has more than two 0s in a row. That enhances the

operation of the phase-locked loop and improves data integrity through the use of the coding scheme. The 6250-bit/in. GCR is merely one of several run-length limited codes.

4-bit			5-bit	
Hex	Binary		Hex	Binary
00	0000	=	19	11001
01	0001	=	1B	11011
02	0010	=	12	10010
03	0011	=	13	10011
04	0100	=	1D	11101
05	0101	=	15	10101
06	0110	=	16	10110
07	0111	=	17	10111
08	1000	=	1A	11010
09	1001	=	09	01001
0A	1010	=	0A	01010
0B	1011	=	0B	01011
0C	1100	=	1E	11110
0D	1101	=	0D	01101
0E	1110	=	0E	01110
0F	1111	=	0F	01111

Archive block format
GAP = 1F
SYNC = 07
File mark = 1C

The Sidewinder's data stream is an 8-bit byte coming in through the interface. This word is broken down into two nibbles of 4 bits each. Each nibble is passed to run-length limited encoders, which put out 5 bits for each nibble. These bits are then serialized and sent to the read/write electronics.

Another improvement is the NRZI recording method.

The first factor to affect the total system performance is tape speed. When data are clocked onto the tape with nanosecond resolution, the tape speed must be constant for effective recording and reading. Another key element is tape tension. Insufficient tension can cause the tape to pull away from the recording head, possibly resulting in recording skips, so that the cartridge must be designed to be self-tensioning. Track registration is yet another consideration: The cartridge and transport must align perfectly so that the tape will always be

This approach ensures data reliability at data densities of 8000 bits/in. What's more, NRZI offers a lower bandwidth and a high packing density/area than other recording techniques.

Another feature adding to the integrity and accuracy of the data being recovered is a variable data window. In addition to having separate write and read thresholds as conventional tape drives do, the Sidewinder, while checking the CRC character, factors the cell time of that byte by only 75% on read after write, versus a 100% cell time on a straight read operation. That ensures that a tape is never written that another ¼-in. Sidewinder unit could not read.

The Sidewinder uses a 48-step stepper motor for track registration to align tracks precisely. The motor moves approximately 7¼% per step. Each step has a horizontal up/down registration to within 0.001 in. In addition, the mounting plate assembly for the entire read/write head has adjustment screws that are set at the factory to control head azimuth and tilt in relationship to the outer and inner surface of the tape. This precise control over track alignment, positioning, and so on, maintains and guarantees interchangeability of media from one unit to the next.

Speed control by the microprocessor and associated circuitry ensures constant nondistorting operation at 30 to 90 in./s. The capstan motor produces clock pulses for each revolution of the capstan motor, which are fed to a comparator. Feeding into the other side of the comparator is a reference frequency supplied by a crystal. The comparator produces an error signal if there is any deviation from the nominal. This signal is fed to a phase-modulated amplifier, which in turn drives the motor.

positioned against the head in the same place.

Data reliability also depends on the subsystem design criteria. As with any device with rotating media, the system must control:

- Amplitude variations. The data must be put down with signal strengths compatible with the system circuitry to assure accurate recovery (read).
- Signal phase distortion. Such control is needed because distorted signal inputs yield distorted data.
- Pulse crowding. Bit shifting and crowding produce soft errors in the system. When data are clocked down and bits shift, data are lost and reliability suffers.
- Mechanical head-tape interface. The tape-to-head contact must be precise to ensure that all cartridges perform identically.

All that is done by the Sidewinder.

Intelligent drive

The Sidewinder consists of two components: the tape drive and a controller. The latter has been designed specifically for a streaming environment at a recording density of 8000 bits/in. The tape controller has been designed to complement the drive's DMA I/O architecture by incorporating a microprocessor to relieve the host CPU of such overhead functions as buffering, positioning the tape, detecting errors, rereading, formatting the tape, searching for files, and determining the read status. The microprocessor also minimizes the engineering hardware and software efforts required to interface the ¼-in. streaming cartridge tape drives with a host CPU, as mentioned earlier.

Interrecord gaps

In conventional ½-in. tape systems, the recorded data are blocked into records that can be individually accessed and updated. To preserve the individuality of each record, the tape system must start and stop between records. This requirement necessitates fairly long interrecord gaps.

The length of these gaps must be considered in the tradeoffs among tape utilization, the tape's speed, the start and stop times of the tape drive, and the complexity of the tape drive. Conventional tape systems have established themselves as cost-effective computer peripherals that provide sequential access to small individual blocks of data. However, because of the long interrecord gaps, their tape utilization efficiency is typically low.

In conventional tape cartridge systems, utilization efficiency can vary from less than 20% to almost 80%. At 80% the record length is 4 kbytes, and the advantages of short individual records are lost. What's more, the throughput rate of a start/stop tape unit is directly proportional to the tape utiliza-

reduces the throughput drastically.

In contrast, a streaming tape system employs very short interrecord gaps and keeps the tape moving at a constant high speed to achieve maximum tape utilization and data throughput rate. That makes it particularly well-suited to those applications that do not require the tape system to access and update individual records—like backing up disk drives.

Minimizing the large interrecord gap reduces the usual penalty of higher cost for increased storage and performance. When applied to the conventional 1/4-in. tape cartridge, streaming techniques raise tape utilization to a booming 97%, which makes for a low cost/bit ratio. The Sidewinder achieves a system throughput of 20 Mbytes in a little over 4 minutes by eliminating high-performance start/stop requirements and by moving the tape at 90 in./s.

The cartridge tape controller enables a user to take advantage of the cost savings afforded by a streaming cartridge tape system without the usual delays associated with a full engineering program to develop

independent read and write channels, three 512-byte buffer memories, a host interface, a drive interface, and a microcomputer. The controller makes tape formatting, error processing, head positioning, and motion control transparent to the host system.

The host interface hardware is designed for easy connection to a variety of microprocessors and system buses (Fig 2). It consists of two programmed I/O control lines, two programmed I/O status lines, two DMA control lines, an 8-bit bidirectional bus, a bus direction line, and a controller reset line.

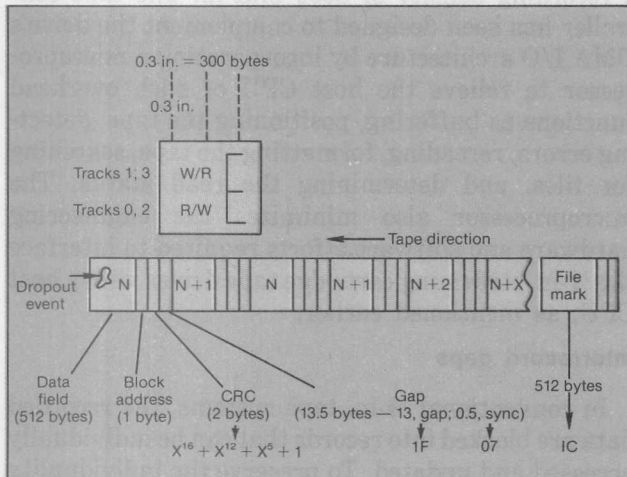
As mentioned, the host software drivers can be designed with as few as two commands—read and write. With this software configuration, a 20-Mbyte intelligent drive will appear as a 20-Mbyte FIFO in which data is blocked into 512-byte blocks. For applications requiring a more conventional tape format, the controller has a set of seven commands (see Table 2).

The streaming approach provides other benefits. For example, marginal areas of the tape are bypassed and bad records are rewritten on the fly. Read errors are reread automatically. The read-after-write check is appended to guarantee nominal read performance. Another benefit is that the read-after-write error sequence does not require host intervention by the host (Fig. 3). In addition, there is no need for error-checking and correction codes (Fig. 4).

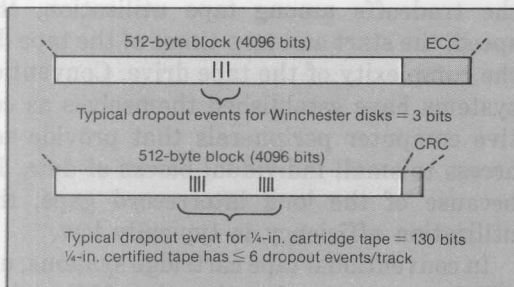
Since the drive automatically monitors the number of rewrites or rereads, the user can tell the performance of the cartridge. If he sees the number of rewrites going up and the rereads remaining constant, he knows that the tape is starting to degrade and the cartridge should be changed.

Furthermore, the drive can generate file marks, which allow easy searches of individual data files and provide the ability to append records to previously recorded tapes. The latter capability can be extremely useful when employing the tape to distribute software. During a write operation, if the host system starves the tape in its streaming mode, the device ramps down. At the next command to write, it will automatically reposition, read forward to the last block written, and begin writing into the next logical block. This activity takes less than 1 second.

To maintain a high level of integrity—or long-term reliability of the data written on the tape—the Sidewinder employs several advanced techniques (see "Making the Most of Tape Recording Technology"). □



3. The controller processes read-after-write error recovery automatically. Since this process is transparent to the host, a statistical counter is provided to inform the host of the number of blocks automatically rewritten by the controller.



4. Error-checking and correcting codes cannot be used to correct errors on the tape efficiently and cost-effectively. Furthermore, ECC adds cost and complexity to the tape drive design, in addition to reducing the available capacity by about 1%.

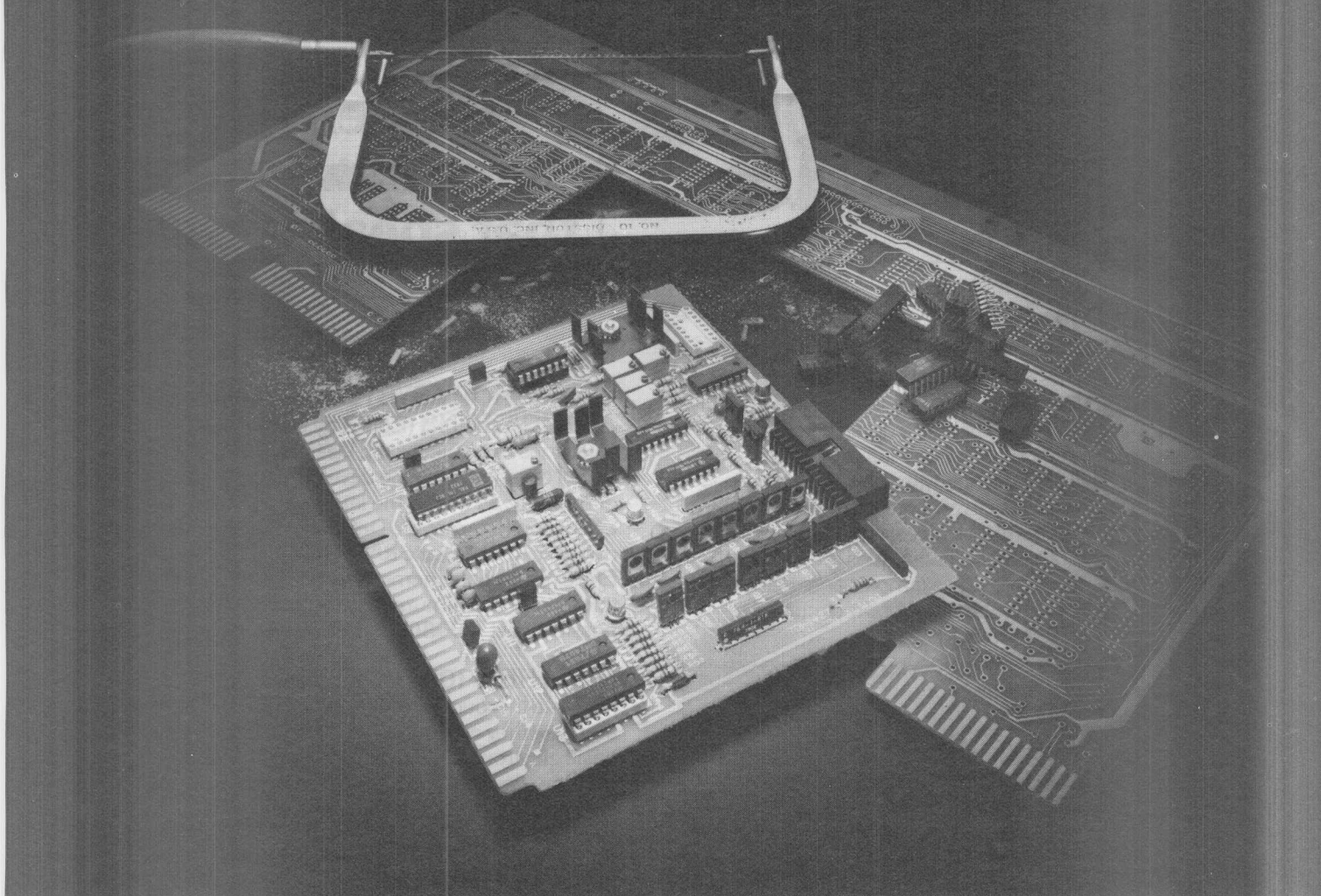
How useful?

Immediate design application
Within the next year
Not applicable

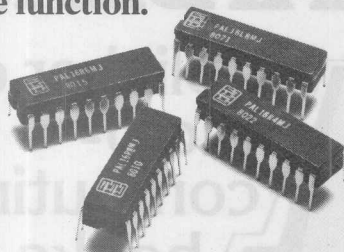
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With a byte-wide family of upgradable and pin-compatible RAMs, ROMs, and UV EPROMs to draw from, designers need only design one board to fit many applications.

Byte-wide memories keep system design in the family

Byte-wide memory outputs are nothing new—PROMs and some low-density RAMs organized that way have been available for years. But a byte-wide family that also includes high-density, high-speed static RAMs (1-kbyte and larger) along with ROMs and EEPROMs is something else again. Typical organizations of 1-k \times 8, 2-k \times 8, 4-k \times 8, 16-k \times 8, and 32-k \times 8 all within the same family—give system designers a growth path that maintains pin compatibility and incremented expansion on a compact board layout.

High-speed static RAMs like the 1-k \times 8 MK-4801A and the 2-k \times 8 MK-4802 or the medium-access-speed MK48D02 (with low data retention power drain) are just gaining the densities and pinouts to make them compatible with today's 16-k and 32-k UV EPROMs. This pin compatibility between RAMs and non-volatile memories is an essential element in Mostek's decision to take the 24-pin, 600-mil-wide package and develop a family of byte-wide memory products that includes even EEPROMs. In addition, the pinout has been approved by JEDEC, along with extensions that expand it to 28 pins for future growth.

Memories in the Mostek "Bytewyde" family are completely interchangeable. To upgrade, just pull out the old chip, plug in the larger unit, and add the extra address line. The family's new 28-pin package could handle up to 15 address lines and up to 32

kbytes of memory. Figure 1 shows the various pinouts of the current family members and proposed future members. (Leadless chip-carrier versions are also available.)

For systems in which the total RAM capacity is less than 16 kbytes, the byte-wide memory products permit extensive granularity (sometimes called incremental-modular expansion) without a high packaging overhead or a lot of extra memory space. Otherwise, a system that requires, say, 8 kbytes of RAM couldn't take advantage of 16-k \times 1 memories without wasting half the capacity.

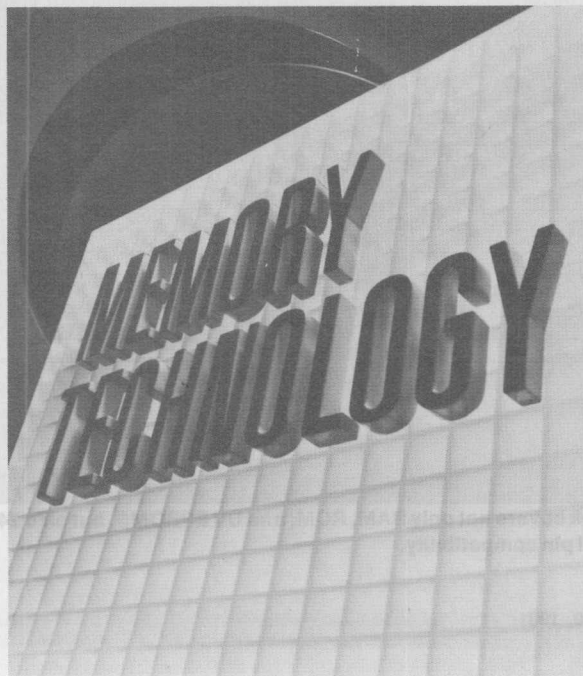
Up to now, even granularity could be wasteful. If, for example, a user had \times 1 memories in a system, and more memory was needed, eight more chips had to be added (with the increment typically being 4096 words if 4-k static RAMs were used). But if only 1 kbyte more was actually needed, 3 kbytes went to waste.

With available Bytewyde-family products, a single chip provides 1 or 2 kbytes of RAM; 8-kbyte chips should be available by the mid-1980s. Then, major areas on a printed-circuit board will no longer have to be reserved for RAM expansion—the byte-wide RAMs follow the ROM and UV EPROM pinouts, and can often be plugged right into the nonvolatile memory locations.

Getting more control

The Bytewyde family is distinctive in many other ways, with advantages that extend far beyond the realm represented by \times 1 memories.

For example, because most



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output lines, a single control function (chip enable) provides complete control of the memory's output buffer. The individual data-in and data-out lines are interfaced to separate buffers, and the enable lines of those buffers control the interfacing of the common I/O bus. When a bidirectional I/O data bus is used, an output-enable control on the memory chips helps control the time multiplexing of the data-in and data-out lines.

When memories are pushed to their top performance limit, however, output-enable control may be used improperly, which causes bus contention. One of the most telling examples of the need for independent control of the outputs in high-speed systems occurs during the write cycle.

Proper memory timing requires that the write-enable line be brought high for a certain period (t_{WPL}) before the write cycle actually ends (Fig. 2). This time, equal to about 50 ns in the -70 versions of the MK-4801A memories, allows the write cycle to be completed internally.

After t_{WPL} has elapsed, an internal read cycle of the memory begins. But if the chip-enable line is held low for too long, a read access will occur and the memory's outputs will turn on. Since this occurs during a write cycle, the memory and data-buffer

But a separate output-enable line avoids this potential problem and others as well.

Bus contention also can cause problems in adjacent circuitry; for example, current peaks between competing outputs can reach 400 mA and couple to other board traces. The trace-to-trace coupling, in turn, can produce phantom signals that appear as soft errors. All these potential problems fail to materialize, thanks to the separate output-enable line.

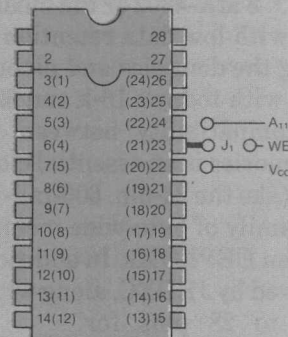
In many cases, packaging considerations play a major role in the selection of a particular memory type for a system. High-performance memories are available in $\times 1$, $\times 4$, and $\times 8$ organizations. The choice should not be made without scrutinizing the final memory array.

If the array is to be $4\text{-k} \times 32\text{-bit}$, then the user needs 32 $4\text{-k} \times 1$ chips, 32 $1\text{-k} \times 4$ chips or just 16 $1\text{-k} \times 8$ chips. Should $4\text{-k} \times 1$ RAMs be selected, an overdrive condition on the address-line buffer would immediately surface, since the address buffer would have to drive 32 bus pins. To eliminate the overdrive problem, the array could be set up as four rows of eight chips each.

If board-design rules of one driver per eight address lines are used, the $4\text{-k} \times 1$ array would require four sets of 14 drivers. On the other hand,

Memory type	Part number	Capacity	Package	Jumper
ROM	MK34000	$2\text{ k} \times 8$	24-pin	NC
ROM	MK37000	$8\text{ k} \times 8$	28-pin	A_{11}
ROM		$32\text{ k} \times 8$	28-pin	A_{11}
RAM	MK4802	$2\text{ k} \times 8$	24-pin	WE
RAM		$4\text{ k} \times 8$	28-pin	A_{11}
RAM	MK4118A/4801A	$1\text{ k} \times 8$	24-pin	WE
E PROM	MK2716	$2\text{ k} \times 8$	24-pin	V_{CC}
E PROM	MK2764*	$8\text{ k} \times 8$	28-pin	A_{11}

*Available 1981



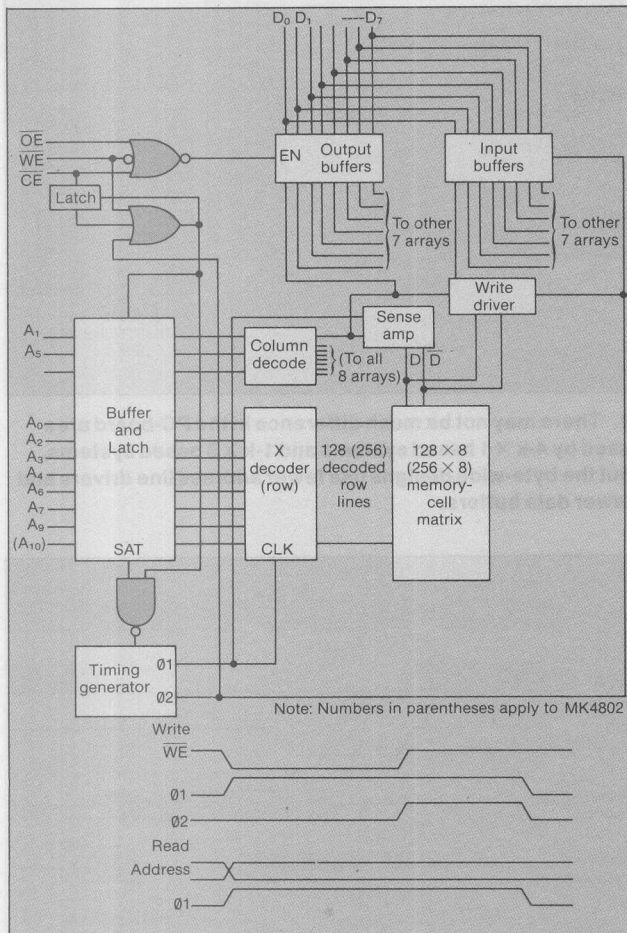
4118A/4801A	4802	34000	2716	$4\text{ k} \times 8$	37000	$32\text{ k} \times 8$	2764	2764	$32\text{ k} \times 8$	37000	$4\text{ k} \times 8$	2716	34000	4802	4118A/4801A
				NC	NC	A_{14}	NC	V_{CC}	V_{CC}	V_{CC}	V_{CC}				
				NC	A_{12}	A_{12}	A_{12}	NC	NC	NC	WE				
A_7	A_7	A_7	A_7	A_7	A_7	A_7	A_7	NC	A_{13}	NC	NC	V_{CC}	V_{CC}	V_{CC}	V_{CC}
A_6	A_6	A_6	A_6	A_6	A_6	A_6	A_6	A_6	A_6	A_6	A_6	A_6	A_6	A_6	A_6
A_5	A_5	A_5	A_5	A_5	A_5	A_5	A_5	A_5	A_5	A_5	A_5	A_5	A_5	A_5	A_5
A_4	A_4	A_4	A_4	A_4	A_4	A_4	A_4	A_4	A_4	A_4	A_4	V_{PP}	NC	WE	WE
A_3	A_3	A_3	A_3	A_3	A_3	A_3	A_3	OE/ V_{PP}	OE	OE	OE	OE	OE	OE	OE
A_2	A_2	A_2	A_2	A_2	A_2	A_2	A_2	A_{10}	A/O	A_{10}	A/O	A_{10}	A_{10}	A_{10}	NC
A_1	A_1	A_1	A_1	A_1	A_1	A_1	A_1	CE	CE	CE	CE	CE	CE	CE	CE
A_0	A_0	A_0	A_0	A_0	A_0	A_0	A_0	D_7	D_7	D_7	D_7	D_7	D_7	D_7	D_7
D_0	D_0	D_0	D_0	D_0	D_0	D_0	D_0	D_6	D_6	D_6	D_6	D_6	D_6	D_6	D_6
D_1	D_1	D_1	D_1	D_1	D_1	D_1	D_1	D_5	D_5	D_5	D_5	D_5	D_5	D_5	D_5
D_2	D_2	D_2	D_2	D_2	D_2	D_2	D_2	D_4	D_4	D_4	D_4	D_4	D_4	D_4	D_4
V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	D_3	D_3	D_3	D_3	D_3	D_3	D_3	D_3

1. The Bytewyde family from Mostek covers not only RAM, ROM, and UV EPROMs, but also 24 and 28-pin DIPs and 32-pad LCCs to provide full pin compatibility.

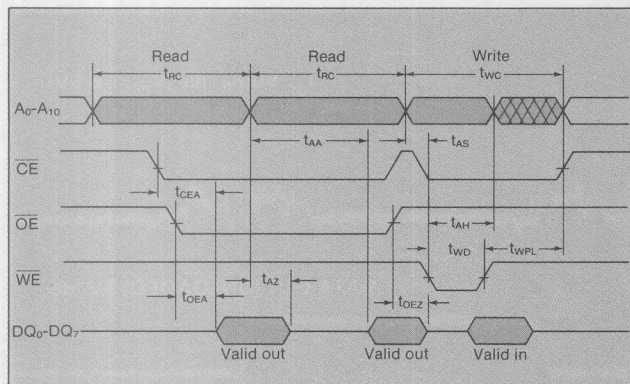
The SAT detectors are the “trick” to making the

Electronic Design • September 30, 1981 229

Memory Technology: Byte-wide memories



5. The timing differences between a read cycle followed by another read cycle and a read cycle followed by a write cycle amount to about a 10-ns increase in the write cycle, since the memory-output buffers need time to turn off.



6. Inside the MK-4801A, the timing generator starts when the sense-address-transition (SAT) circuitry on the address inputs detects the final transition on the address lines. This, and only this, starts the fully static read cycle.

RAMs appear static in the read mode. Actually, however, there are two different types of access times (Fig. 6). The t_{AA} value shown reflects the full rated speed of the memory—the fastest access is initiated when an address transition is detected, and is measured from the time the last address line is stable. The other two periods, t_{CEA} , and t_{OEA} , equal half of t_{AA} . (When the write-enable line is high, the only impact that the chip enable and output enable have is on the buffer, and in the read mode, that is all those two control lines do.)

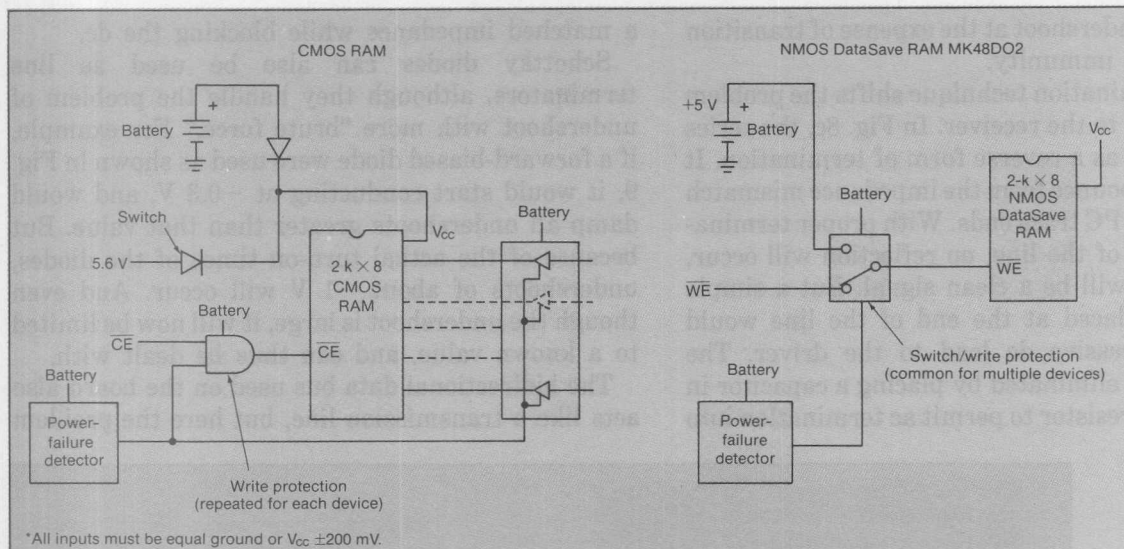
For data to appear at the output once the transitions are detected, the decoders select the proper row and columns, and the sense amplifiers detect the state of the cell and then feed the results to the output buffers. In both the MK-4801A and 4802, the data and data-bar lines are metal instead of polysilicon to keep the resistance low and thus keep the propagation delays short. If an address transition occurs before a complete access cycle occurs, the phase-1 cycle will not be completed and a new access will begin, with the memory outputs remaining in a high-impedance state.

The advantage of an address-activated read cycle is speed—as most system applications would show, time is required to decode some of the highest-order addresses into the chip-enable signal. If the chip access time begins from the address transition instead of from the edge of the chip-enable signal, then the chip decode time will no longer need to be minimized, thus allowing the use of slower logic while speeding up system operation.

Having the write cycle operate differently from the read cycle ensures the security of information stored in the array. System noise that could cause a read cycle to be aborted will not cause a loss of data, but during a write could cause incorrect data to be written into the memory. If, for example, a write cycle were to operate in the same manner as a read cycle, noise would be coupled into one of the address lines halfway through the phase-1 period, and the write cycle would be terminated, potentially leaving the eight cells in indeterminate states.

To prevent this from happening, a signal is generated inside the chip as soon as both the write-enable and chip-enable lines go low (become active). The signal latches the address-line inputs and marks the beginning of the phase-1 cycle. For an interval, t_{WD} , the row and column decoders select the proper cell, and during another interval, t_{DSW} , the data on the I/O lines settle into the input buffers.

When the write-enable line goes from low to high, the actual write starts. At this point, the phase-2 internal clock goes active and prevents any activity on the chip-enable or write-enable lines from interfering with the completion of the write cycle.



7. The low-power DataSave feature of the MK-48D02 drastically simplifies the support circuitry needed to power-down a memory system.

The 4801A and 4802 come in several versions with varying speeds: Write-cycle times are 80 or 100 ns, and ready-cycle times are 70 or 90 ns. The differences stem from system constraints on the bidirectional data bus.

Reducing power

Another version of the MK-4802, the MK-48D02, features an ultralow power-down mode called DataSave. This mode can be entered by holding the write-enable pin high (between 4 and 6 V), and letting V_{CC} ramp down to 0 V with a slew rate of 200 ns/V. Memory contents are maintained through the write-enable pin at a current drain of less than 50 μ A at 4 V, while all other memory inputs are in a don't-care condition. This DataSave feature is currently available on the 48D02 versions of the 2-k \times 8 RAMs in a full range of speeds.

Single-pin control of the memory, which both protects writes and saves the memory contents, gives the user a simple interface to the backup battery and control signals. This considerably simplifies the control needed by CMOS RAMs that use battery backup (Fig. 7). The electronically controlled power switch in both cases must be controlled by an early-warning system to notify the array of an impending power failure.

As system speeds increase, the design of the memory interface becomes much more than simply picking up a data book and selecting parts. Cycle times below 100 ns require that every available nanosecond be usable, and not eaten up by propagation delays and ringing. To keep this wasted time minimal, board design should account for high-frequency signal transmission.

When the propagation delays of the circuit in-

terconnections become significant with respect to the rise and fall times of the driver, the circuit behaves like a transmission line. If these effects are not considered, soft errors resulting from noise could occur. In systems that look like transmission lines, the load impedance should match the impedance of the transmission line for the maximum energy transfer.

Mismatches in the impedance will cause ringing, undershoots, and reflections. To gauge some of the effects of transmission lines, consider a design example using a four-layer PC board with internal power and ground planes and 20-mil line and spacing rules. Propagation delays can run about 4 ns per foot, and since a row of 16 devices is 12 in. long, delays are large compared with the desired 5-ns rise and fall times. As Fig. 8a shows, undershoots greater than -2 V can result at the end of an unterminated line.

The upper trace shows the signal measured at the Schottky driver outputs, while the lower trace shows the signal at the end of the unterminated line. Minimum voltage on any pin is specified at -1.5 V (for less than 50-ns duration). Since the measured undershoot exceeds this level, and many other manufacturers use levels closer to -0.5 V, proper termination becomes extremely critical.

Eliminate undershoot to protect the memory

There are many ways to minimize undershoot. One of the simplest is to put a resistor in series with the PC trace to match the impedance of the trace to the driver. Figure 8b shows the effect of a 43- Ω resistor. Not only is the undershoot considerably reduced, but the noise on the line drops without much waveform degradation. The value of the resistor can be empirically determined, but too large a value will

Memory Technology: Byte-wide memories

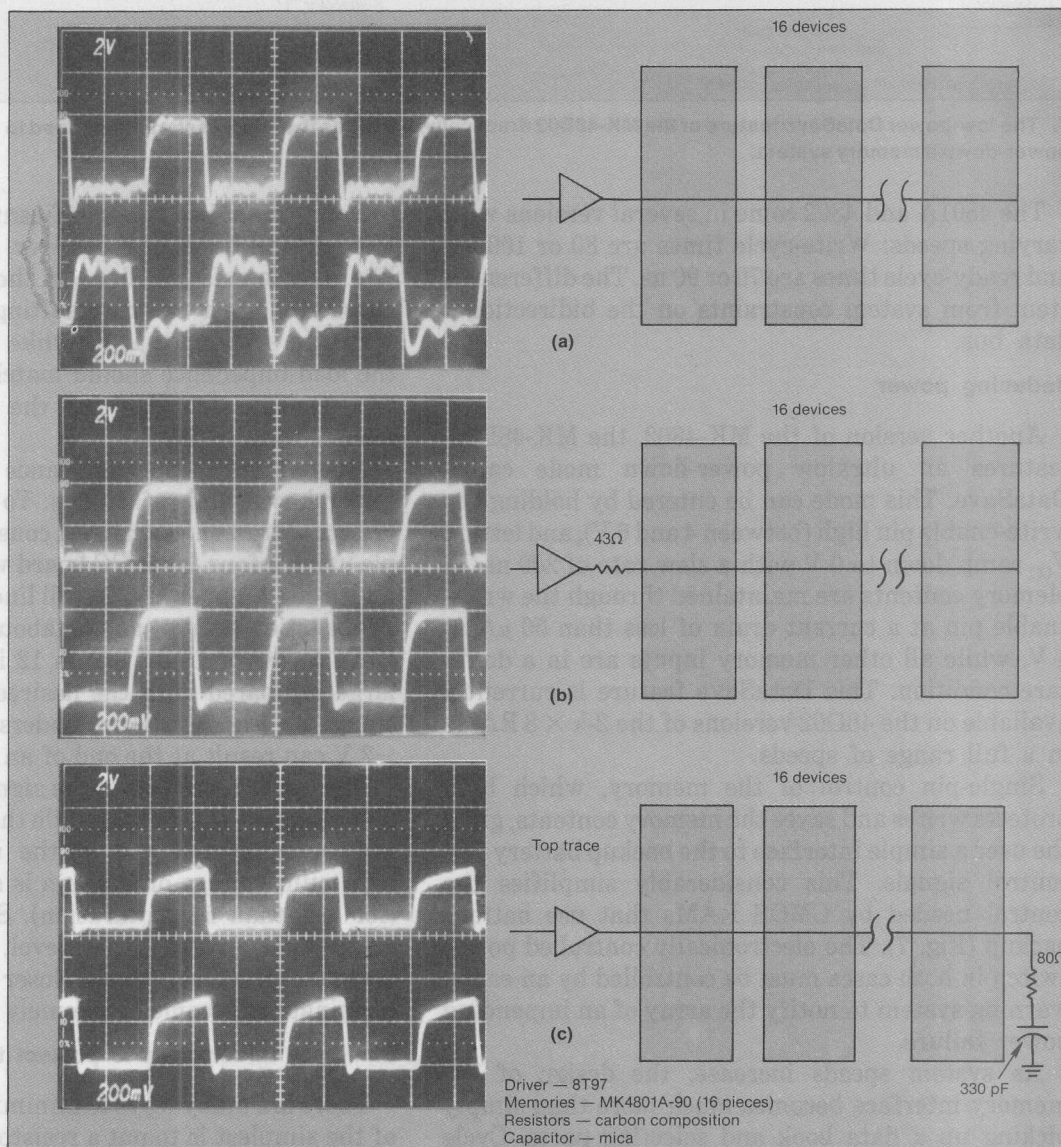
eliminate the undershoot at the expense of transition time and noise immunity.

Another termination technique shifts the problem from the driver to the receiver. In Fig. 8c, the series resistor is used as a reverse form of termination. It allows a single bounce from the impedance mismatch found when the PC trace ends. With proper termination at the end of the line, no reflection will occur, and the result will be a clean signal. But a simple 80- Ω resistor placed at the end of the line would present an excessive dc load to the driver. The problem can be eliminated by placing a capacitor in series with the resistor to permit ac termination into

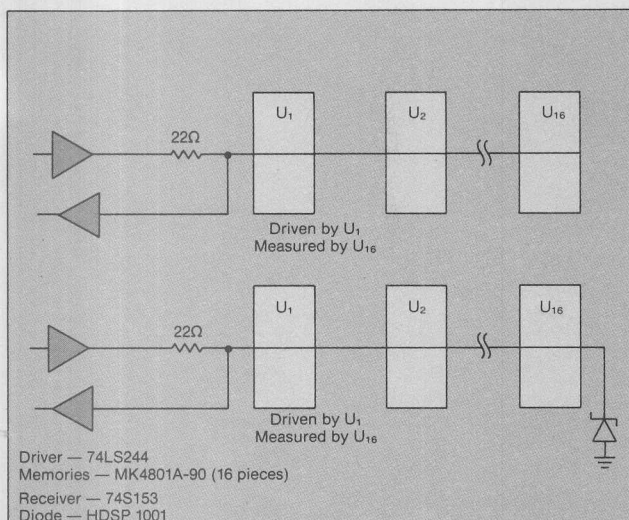
a matched impedance while blocking the dc.

Schottky diodes can also be used as line terminators, although they handle the problem of undershoot with more "brute force." For example, if a forward-biased diode were used as shown in Fig. 9, it would start conducting at -0.3 V, and would damp all undershoots greater than that value. But because of the actual turn-on times of the diodes, undershoots of about -1 V will occur. And even though the undershoot is large, it will now be limited to a known value, and can thus be dealt with.

The bidirectional data bus used on the board also acts like a transmission line, but here the problem



8. Compare the results of transmission-line measurements on memory-board traces: Whereas an unterminated version (a) shows a considerable amount of undershoot, a series-resistor termination technique (b) virtually eliminates the undershoot. A combination R-C series network (c) minimizes the dc-current loading, but the capacitance degrades the signal's rise time.



9. A single series resistor (a) can drive the bidirectional bus but when the bus goes into the high-impedance state, the resistor doesn't help much. The problem can be solved by adding a Schottky diode to terminate the line and limit the swing of any undershoot (b).

is not only that a single driver drives a number of memory inputs, but that each memory drives the line during a read cycle. Here, too, a single series resistor located at the driver will handle the undershoot problem.

The Schottky solution

However, when the driver is in the high-impedance state, the series resistor will not have a significant impact as a line terminator, and one of the memory devices must serve as a line driver. Trouble is, MOS memories are not known as powerful drivers, and cannot compete for speed or low impedance with a Schottky device. The two circuits in Fig. 9, along with the resulting waveforms, show the difference a Schottky diode added after the last memory device makes. Series resistors at each memory chip would occupy excessive board area, and resistor-capacitor termination would load down the MOS drivers excessively.

For future designs, then, two simple rules should be remembered:

1. Provide a series resistor in the address and control lines and, if the series resistor is not enough, provide an R-C shunt at the end of the trace.
2. Put a series resistor at the data driver, but not between the data line and receiver when one of the memories drives the line, and provide for a Schottky diode at the end of the line to supply termination. □

How useful?

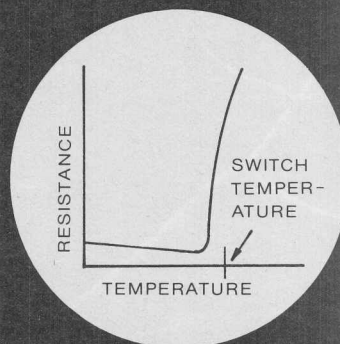
Immediate design application
Within the next year
Not applicable

Circle

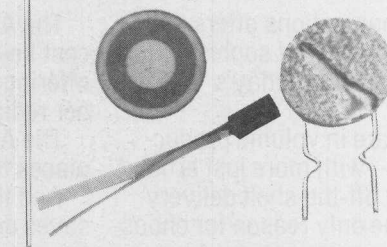
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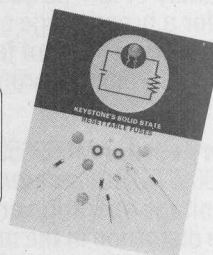
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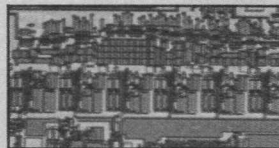
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Nonvolatile RAMs arranged as 256×4 and 64×4 bits facilitate the design of microprocessor-based systems requiring permanent storage of such parameters as calibration data for instruments.

4-bit-wide nonvolatile RAMs open up new applications

With the appearance of nonvolatile RAMs in 4-bit-wide configurations, designers can now enjoy the benefit of these unusual memories while cutting the chip count. These parts are unique in that they contain two memories in one device, a RAM and an EEPROM (see "How Nonvolatile RAMs Work").

The RAM functions as a fully static memory. The EEPROM, on the other hand, can be accessed only through the RAM. The storage operation transfers the entire contents of the RAM to the EEPROM with a single TTL pulse of 100 ns or greater. The recall operation transfers the contents back to the RAM with a 450-ns TTL pulse. At the end of either operation, both memories will contain the same data. The block diagram of Xicor's nonvolatile RAM family is shown in Fig. 1.

The first nonvolatile RAM was organized as 1024×1 bit. Although this configuration is extremely useful, eight chips are needed to construct a byte-wide memory. Some applications, however, require less than 1 kbyte of memory, and for them the designer had to buy the additional capacity even though he did not need it.

Since then, two more parts have come out, a 64×4 and a 256×4 device. The main advantage of the smaller part is in the storage of data that change infrequently—for instance, toggle-switch settings in terminals or calibration data in instruments. The larger-capacity memory is more applicable to those uses

where data generated during on-line operation must be retained when power is removed.

To illustrate how these new $\times 4$ memories can be incorporated into a design, it is helpful to look first at the interface signals of the memory and how they interact with a host computer.

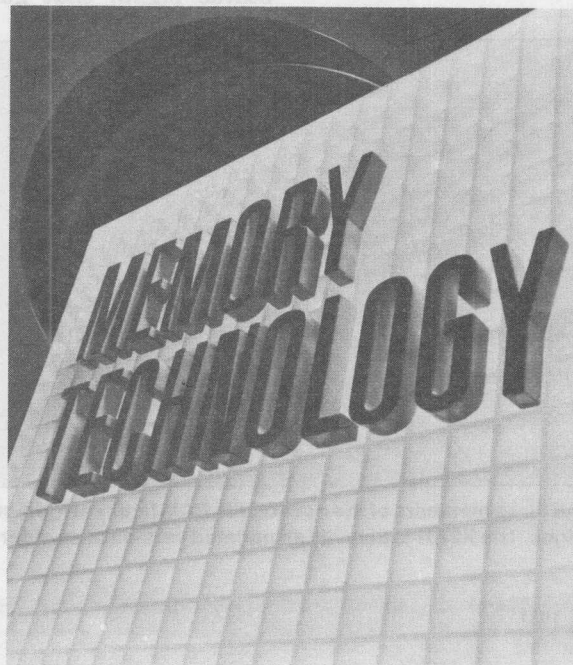
Figure 2 shows the pin configuration of the three chips. The 254×4 memory, the X2212, comes in an 18-pin DIP. The X2210, organized as 64×4 bits, is pin-compatible with the X2212, with two unused pins for the higher-order addresses. The earlier part, the X2201, has been given a new command structure, and the new version is also being introduced with the new parts.

The new command structure makes the nonvolatile RAM considerably easier to use. Three changes have been made: Only one pulse is required for a storage operation; a \overline{CS} signal is no longer required for either storage or recall; and storage is blocked with a recall-low—that is, the recall line is low prior to the occurrence of the storage pulse.

The use of a single storage pulse allows the microprocessor to issue a storage command and then perform other tasks without any further involvement in the storage operation. Removing \overline{CS} as a requirement for storage and recall simplifies the logic to generate the \overline{CS} signal. Finally, storage with a recall-low signal is a more positive way to ensure against an inadvertent storage, since it is difficult to guarantee a high from a TTL gate while the power supply is rising.

To demonstrate the easier-to-use interface of the

George Landers,
Applications Manager
Xicor, Inc.
851 Buckeye Ct.
Milpitas, CA 95035

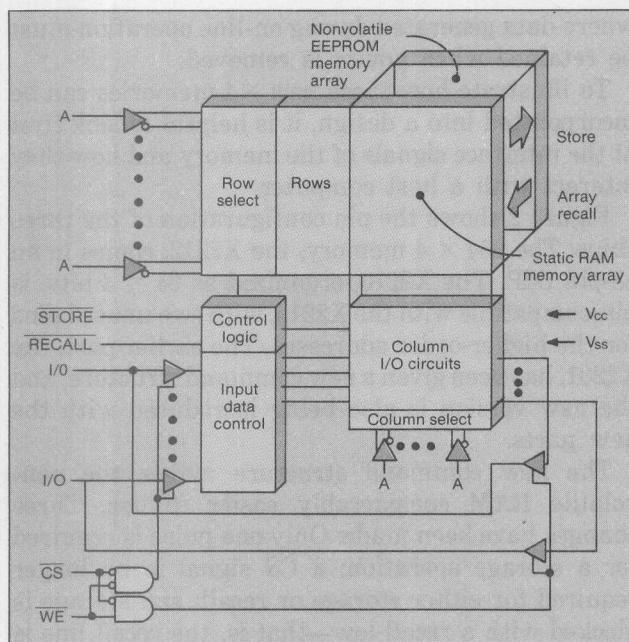


Memory Technology: $\times 4$ nonvolatile RAMs

new command structure, consider the X2210 used with an Apple computer. The Apple II was selected because its address space is fully decoded for I/O functions and it has convenient card slots using these decoder outputs. In fact, three separate decoder lines run to each card slot. One is common for all card slots and is 2048 bytes located at hexadecimal address \$C800 through \$CFFF; the other two are exclusive for an individual card slot. For slot 6 these are a 16-byte block starting at hex address C0E0 and a 256-byte block starting at \$C600.

Adding nonvolatile RAMs to a computer

When the Apple II is turned on, it looks for a disk controller card by examining the first 8 bytes of the



1. The secret behind a nonvolatile RAM is an on-chip EEPROM that can hold the entire contents of the RAM.

256-byte block for each card slot. When the correct 8 bytes are found, the computer jumps control to the program located in the 256-byte block.

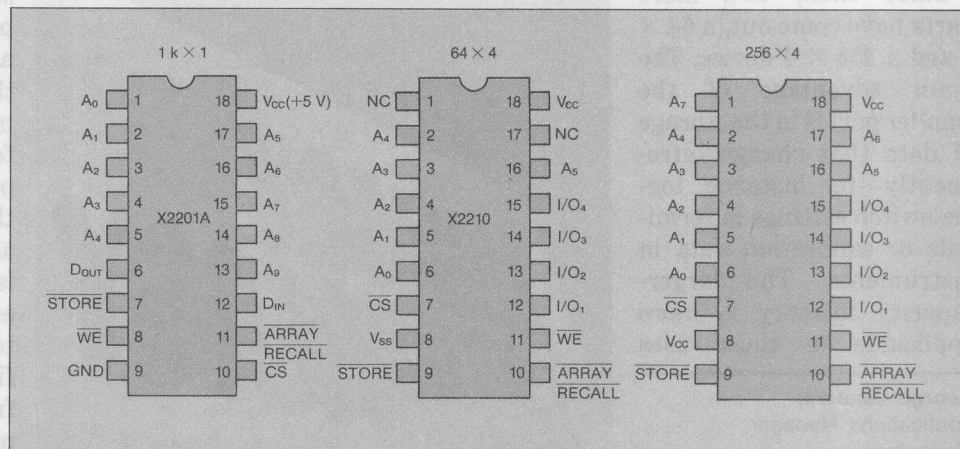
By locating the CS signal for the RAM at \$C600 and loading the correct first 8 bytes, the Apple II can be fooled at power-on into turning control over to a program in the nonvolatile RAM. The recall line is tied to the reset of the Apple, and the storage line (labeled Store) to the 16-byte exclusive select at \$C0E0. Figure 3 shows that no components other than the two X2210s are needed for the interface.

Figure 4 is a machine-language program that draws a box on the screen, with the byte at \$C61B determining the location of the upper left-hand corner and byte \$C613 the location of the lower right-hand corner. When the Apple is turned on and the program is placed in slot 6, the box will automatically be displayed on the screen. The corners can be positioned by writing \$C613 or \$C61B and then reading \$C0E0. The latter operation initiates storage, so that the size of the box will be different when the computer is turned on again.

The preceding descriptions assume that the power supply of the system is clean in its power-up and power-down sequences. In most systems, that may not be the case and should not be assumed. The nonvolatile RAM inhibits any operations whenever the power supply is below 3 V, but some form of storage protection should be provided above 3 V.

Storing data permanently

There are two methods of storage protection, and at least one or preferably both should be designed into the system. The two basic actions are to ensure that the voltage on the storage pin follows the power-supply voltage or to hold the recall pin low while the power-supply voltage is moving up or down. The latter can be accomplished with a power-supply status signal that goes low whenever the power



2. All three members of the nonvolatile RAM family are pin-compatible, easing many new designs. The X2201 is actually an updated version of an older part.

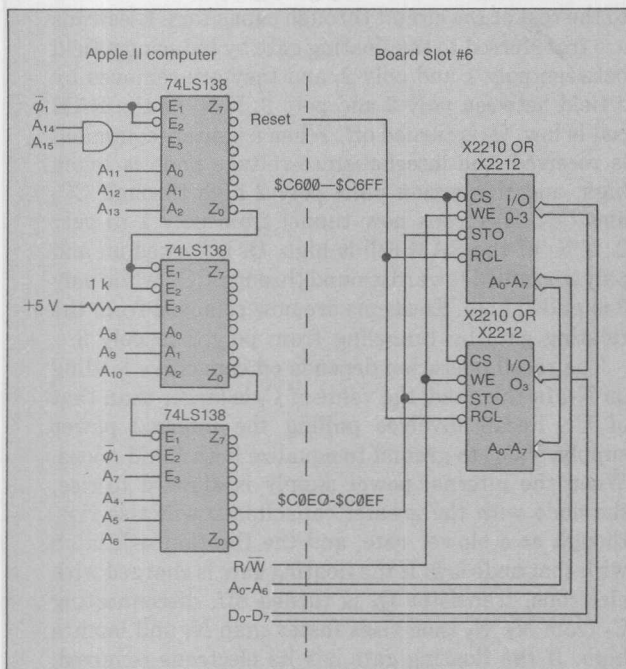
supply is out of tolerance. Tying this signal to the input of the open-collector NAND gate in Fig. 5 ensures that the voltage level on the storage pin trades the supply and that the recall pin is held low. An open-collector gate is used, since the output transistor cannot receive base current as long as any input is held low.

Some of the schemes employed to provide the power-supply status signal involve zener diodes and a sense circuit to monitor either the regulated or the unregulated dc. Alternatively, optoelectronic ac fault detectors can monitor the ac line. The circuit shown in Fig. 6 is a simple monitor of the regulated dc. Whenever the power supply drops below 4.5 V, transistor Q_1 loses base current and turns off, turning Q_2 on. The capacitor provides some delay before releasing the power-supply status.

Example shows how

Figure 7 shows an example of a design using storage protection techniques. The storage pin is held high whenever one of the inputs to the NAND gate is low. For a storage command to be received, several conditions must exist: the power supply must be above 4.5 V, the system reset must be high, the system recall must not be selected, the system write must be low, and the system storage line must be selected. Any other condition and the open-collector NAND gate output will not turn on.

The R/W line is included as a gate input, since



3. To operate the nonvolatile RAM on the I/O bus of an Apple II computer, the CPU reset line is connected to the memory's recall line and the address decoding signal for hex addresses C600 and C6FF selects the two memories.

during initiation, the microprocessor can generate a write command until it is fully under control. The recall line is pulled low whenever the power supply is below 4.5 V, the system reset is low, or the system recall is selected.

In this case, the memory card is designed to fit in slot 7 of the Apple II, with a disk controller card in slot 6. The decoder half selected by $\$C0F0-\$C0FF$ is used to decode the storage and recall command. The system store line is selected when hex addresses $\$C0F0$ through $\$C0F3$ are written or read. Because of the ORing of the system write command, the nonvolatile RAM receives only a storage command for a write cycle. The system recall is selected for hex addresses $\$C0F4$ through $\$C0F7$ and can be either a read or a write cycle.

Fooling the Apple

Again, if the first 8 bytes of the nonvolatile RAM located at hex address $\$C700$ are correct, the Apple II will think that the card is a disk controller and give up control to the program it contains. A 1280-byte machine-language program could be written that does some tasks on power-up. This program can be changed at will by loading a new program from disk and issuing a storage command to place it in

*C600-C63F							
C600-	A2	20	A6	00	A2	03	8C
C608-	20	58	FC	20	40	F8	A9
C610-	85	30	A9	27	85	2C	85
C618-	85	00	A9	00	85	01	A4
C620-	20	19	F8	A4	01	A5	00
C628-	19	F8	A4	01	A5	01	20
C630-	F8	A4	00	A5	01	20	28
C638-	A0	00	A1	00	20	28	F8

4. Shown here is a machine-language program that demonstrates how the nonvolatile RAM works with an Apple II computer. The program simulates the code for a disk controller card and then draws a box on the screen.

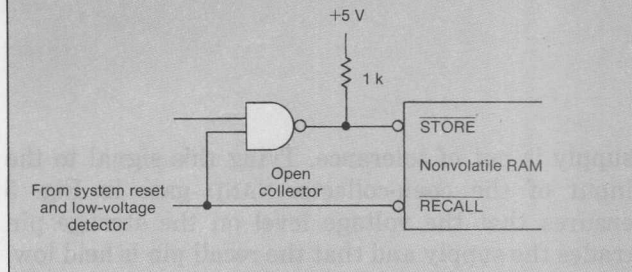
Memory Technology: $\times 4$ nonvolatile RAMs

the EEPROM. Now, the computer performs a different task when it is turned on regardless of what disk is in the disk drive.

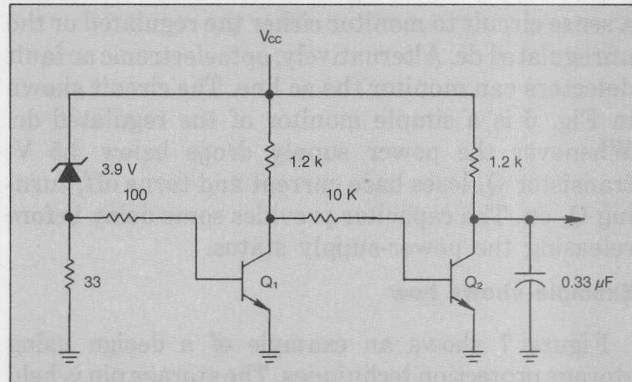
One novel use of nonvolatile RAMs has been to replace DIP switches as holders of configuration data or calibration constants. Here, opting for the memory reduces costs, improves reliability and density, and allows the designer to add system features. Another advantage is that the system board can be sealed against RFI, yet permit access to the switches (bits in the memory).

One memory equals 16 switches

As few as 16 switches (two packs of 8) can be replaced with a single X2210 at a lower overall—that is, assembly as well as component—cost. For a total of \$5, the user now gets 256 switches. Direct savings also result from the elimination of hardware access. In the past, many systems provided access doors cut into the cabinet so that the user could change the settings on the switches. With the nonvolatile RAM, the “switches” can be accessed from a keyboard, and no doors, hinges, or clips are required.



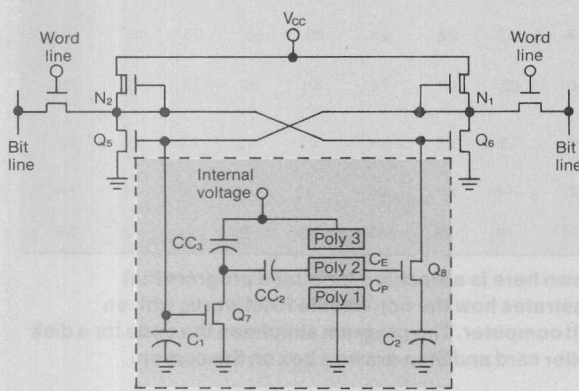
5. The open-collector NAND gate ensures that the storage pin is high whenever the power-supply status is low regardless of the power-supply voltage.



6. Forming a simple monitor of regulated dc, this circuit provides a low signal whenever the supply is below 4.5 V.

How nonvolatile RAMs work

The nonvolatile RAM consists of a RAM and an EEPROM on the same chip. The RAM operates as a fully static memory such as the popular 2102A or the 2114. The EEPROM stores or removes its data by the



absence or presence of electrons on a floating gate. Except for the method of introducing and removing electrons—which does not require high-voltage or ultraviolet light sources—its operation is similar to that of UV EPROMs.

For its nonvolatile RAM, Xicor uses Fowler-Nordheim tunneling, a technique in which tunneling is enhanced through the use of textured surfaces that increase the local field strength. This approach ob-

viates the use of very thin oxides to generate the necessary field strengths.

The figure shows the circuit diagram of each cell in the memory. The floating gate (poly 2) is connected to the rest of the circuit through capacitors. Electrons are transferred to the floating gate by inducing a field between poly 1 and poly 2, and they are removed by a field between poly 2 and poly 3. If N_1 of the RAM cell is low, Q_7 is turned off. When a storage command is received, the internal-store-voltage node is taken high, and this action pulls poly 2 high through CC_2 and CC_3 . Electrons now tunnel from poly 1 to poly 2. If N_1 of the RAM cell is high, Q_7 is turned on and poly 2 is pulled toward ground through CC_2 , while poly 3 is pulled high. Electrons are now removed from the floating gate by tunneling from poly 2 to poly 3.

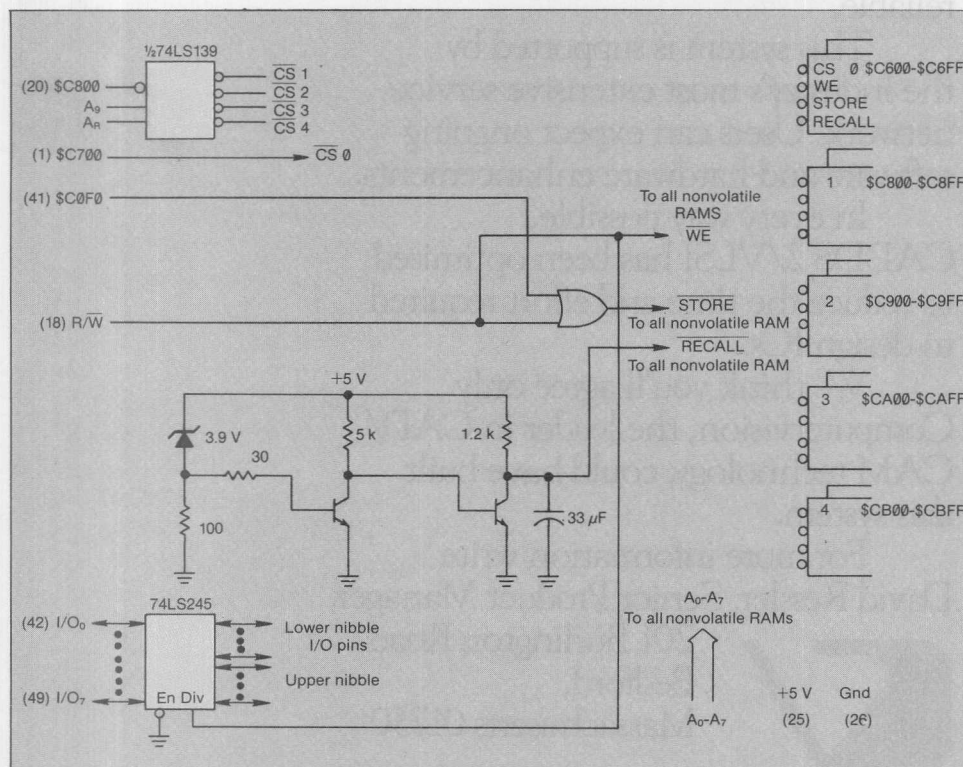
The recall operation depends on capacitive loading on N_2 . In this case, the value of C_2 is larger than that of C_1 . Recall involves pulling the internal power supply, V_{CCA} , to ground to equalize both RAM nodes. When the internal power supply is allowed to rise, the node with the greater capacitance will also rise, though at a slower rate, and the flip-flop will latch with that node low. If the floating gate is charged with electrons, transistor Q_8 is turned off, disconnecting C_2 from N_2 . N_2 then rises faster than N_1 and latches high. If the floating gate has its electrons removed, Q_8 is turned on and C_2 is connected to N_2 , causing N_2 to rise slowly and latch low.

As mentioned, using nonvolatile RAMs, the system designer can add features to a system that would have been impossible with DIP switches. A system can now be reconfigured remotely by telephone link or from the keyboard with software prompting messages. If a system does not require many switches, the leftover part of the memory can be used to store nonvolatile operating data. Finally, the RAM can be used independently after the system has been configured at power-on.

When replacing DIP switches, data are seldom changed and the nonvolatile RAM functions as a read-mostly memory. Similarly, some systems designers are turning to nonvolatile RAMs to store changeable programs or firmware that can be downloaded over a remote line.

In these cases, the required procedure is simple. The best results occur when the status of the power supply is sensed ahead of the regulated dc signal—that is, either at the incoming ac or at the unregulated dc. When the sensed voltage is missing or low for a selected time, an interrupt is issued that sends a single TTL pulse to the storage pin of the nonvolatile RAM. The only requirement for the device is that the 5-V power supply remain within specification for at least 10 ms. During that time, the memory is off the bus and the microprocessor can take care of whatever orderly shutdown procedure is required by the system. □

How useful?	Circle
Immediate design application	562
Within the next year	563
Not applicable	564



7. The circuit above connects nonvolatile RAMs to an Apple II bus and protects stored data on power-up and power-down.

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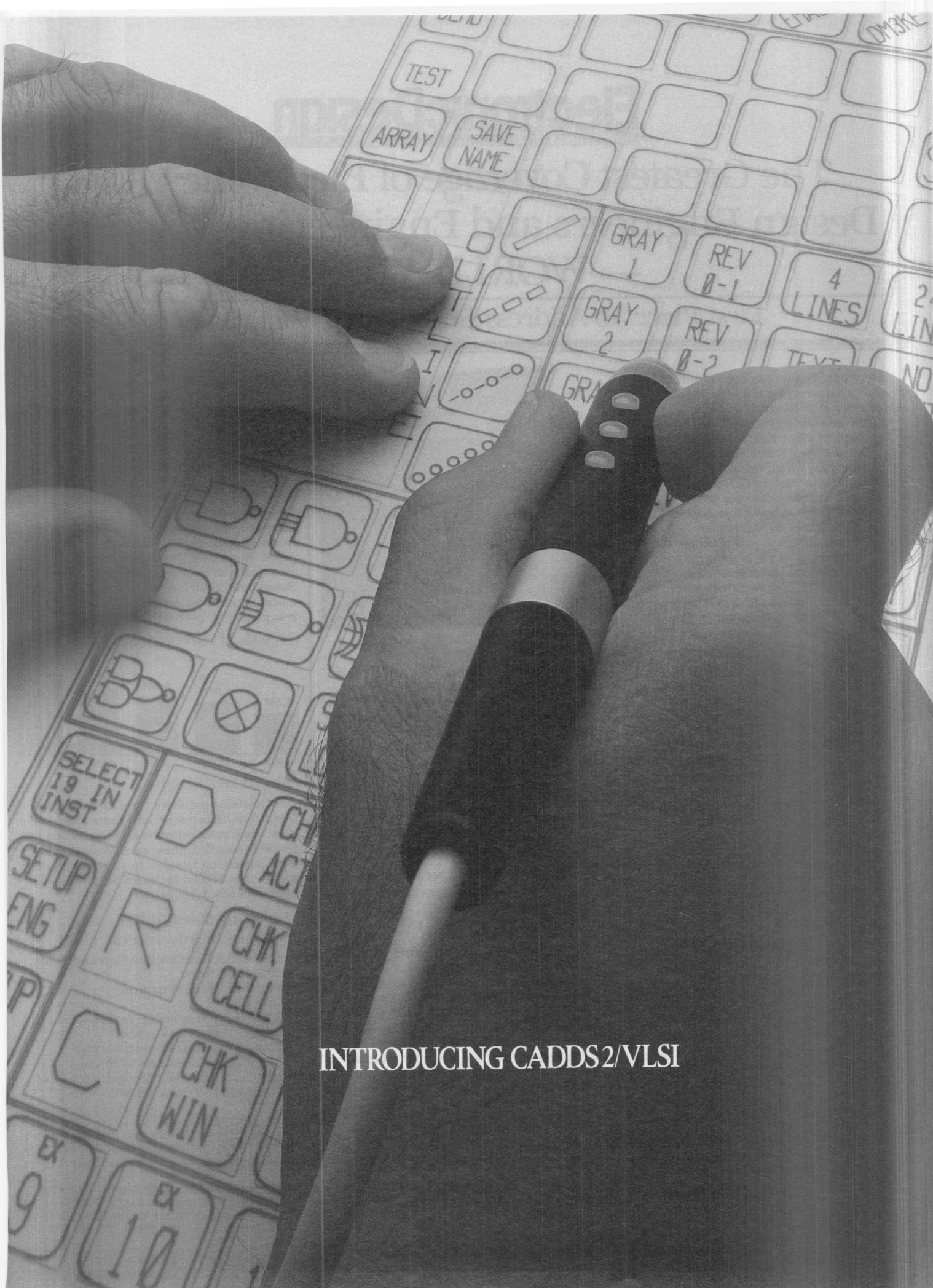
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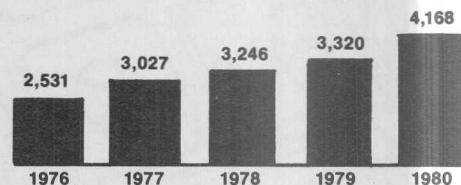
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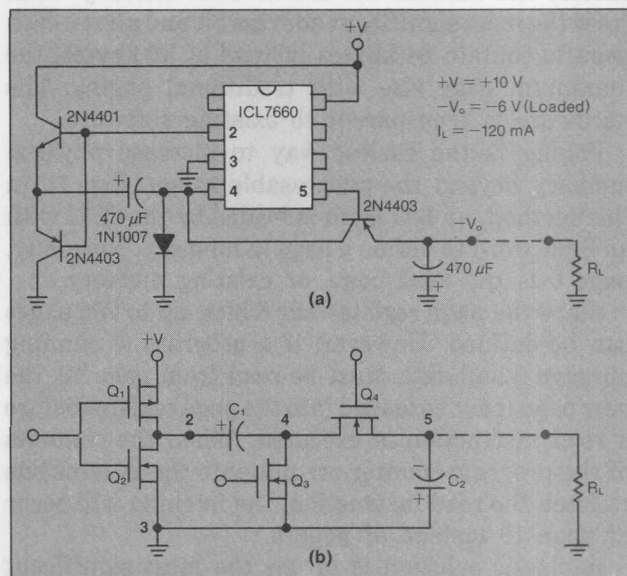
External components increase voltage-converter load current

Diverting charging current from internal transistors and capacitors to external components boosts the maximum load-handling capacity of the ICL 7660 negative-voltage converter more than ten times. The circuit shown in Fig. (a) easily provides 150 mA at approximately -5 to -6 V for an input of $+10$ V. The ICL7660's "barefoot" capability is only about 15 mA. Higher-value capacitors and better switching transistors will further improve the performance of this circuit.

A look inside the circuitry of the ICL7660 (Fig. B) shows that capacitor C_1 charges to the input voltage when transistors Q_1 and Q_3 are turned on and Q_2 and Q_4 are open. When Q_2 and Q_4 are turned on, part of the charge on C_1 is transferred to C_2 , developing a negative potential across C_2 . Subsequent cycles of charging C_1 and discharging the capacitor into C_2 bring the voltage across C_2 up to the input voltage level.

Under load and during the charge cycle of C_1 , C_2 discharges part of its stored charge into R_L . The loss of voltage across C_2 is minimized by keeping the C_1 charge/discharge cycle time shorter than the discharge time of C_2 . The switching frequency of the ICL7660 is approximately 10 kHz.

As Fig. (a) further illustrates, the bulk of the charging current to C_1 and C_2 , and ultimately to the load, is diverted through bipolar transistors, such as



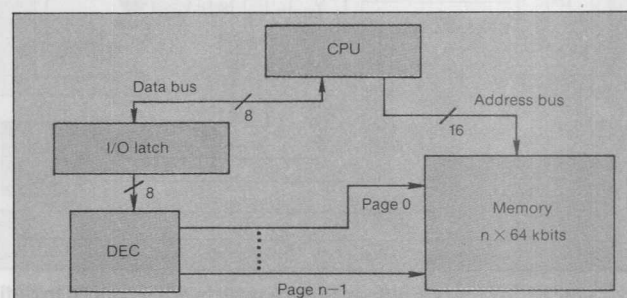
Adding a few external components (a) helps extend the current-handling capacity of the ICL7660 negative-voltage converter (b) to 150 mA or more by diverting current from the internal transistors to external bipolar devices.

the 2N4401 and 2N4403. The diode is added to absorb surge currents, especially when the circuit is first energized.

Syed M. Ahmed, Video Engineer, Videcom Engineering, P. O. Box 308, Mattawan, MI 49071.

Hardware modification expands Z80 memory address space to 16 Mbytes

The addressable memory space of a Z80-based microcomputer can be expanded to 16 Mbytes, far beyond the 64-kbyte limits imposed by the processor's 16-bit address size, by a relatively simple hardware modification. This increase in dynamic memory, made practical by the ever lower cost of memory chips, is particularly useful for dedicated microcomputers manipulating large quantities of data in such applications as speech analysis and synthesis and the measurement of noisy signals by long-term averaging.



1. Traditional paging technique to increase physical memory addressable by a CPU are limited to 32 kbytes.

IdeasForDesign

The modification improves upon traditional paging techniques, since it does not require the most significant address bit to specify whether local or main memory is being addressed. Instead, the circuit recognizes two instructions, each of which (and no others) can address the entire main memory. That frees the most significant address bit and allows each page to contain 64 kbytes instead of 32 kbytes, the maximum page size with traditional paging. The hardware is transparent to existing software.

Paging is the easiest way to increase physical memory beyond the addressable range (Fig. 1). In this method, an I/O latch is loaded by the CPU with an 8-bit word to define a page in memory. Normally, page 0 is the local page, or existing memory.

Since the page register has 8 bits, up to 256 pages can be defined. However, if a program is running on page 0 and data must be read from page 10, the new page must be loaded into the page register before a read instruction is executed. When the contents of the program counter are put onto the address bus to fetch the read instruction, the fetching will occur at page 10 instead of page 0.

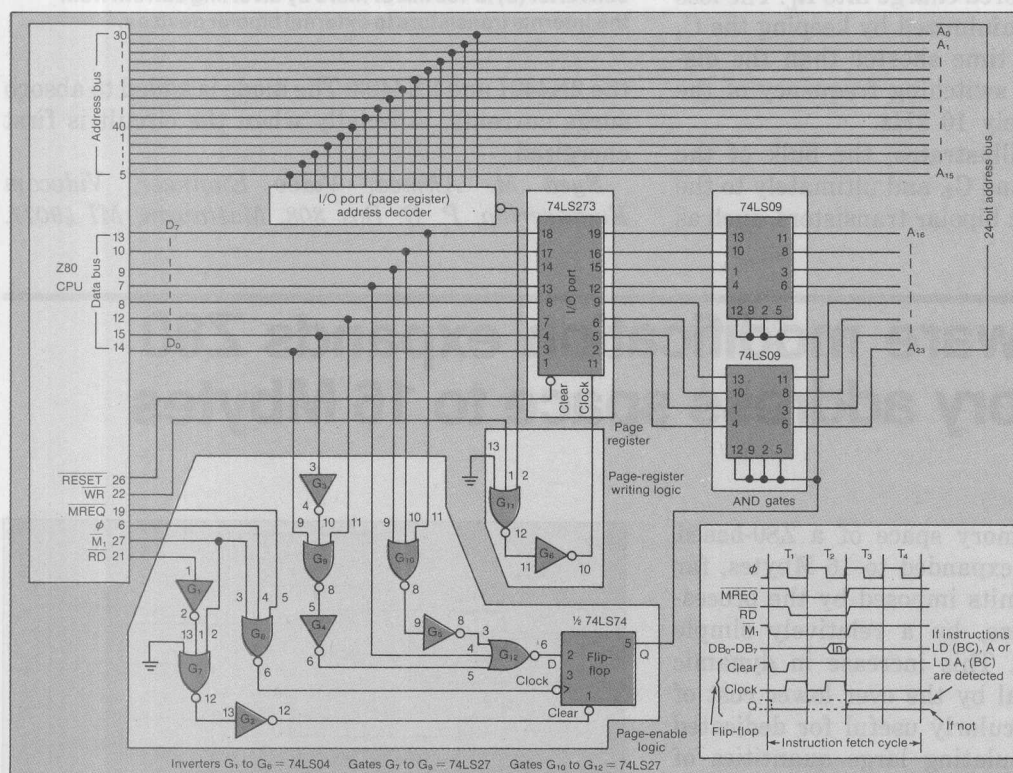
A classic solution is to use the most significant address bit to select either local or main memory. That, however, reduces the main memory size to 32

kbytes, which is not acceptable in most cases. However, as shown in Fig. 2a, instructions on the data bus can be detected during fetching time. Only these instructions can be allowed to access other pages beyond the local.

The timing diagram (Fig. 2b) shows that when the clock, ϕ ; the instruction fetch signal, M_1 ; and the memory request, $MREQ$, are low, the flip-flop will be set if the binary number 00000010 or 00001010 is on the data bus. Since an instruction is being fetched, these numbers correspond to two instruction codes: LD A, (BC) and LD (BC), A.

After the instructions are fetched, the contents of the page register are added to the Z80's 16-bit address bus and cause the instruction to be executed at the page defined by the page register. At the beginning of the next fetching cycle, the flip-flop will be cleared and the next instruction will be fetched from page 0. As this approach frees the most significant address bit, each page, including the local page, will have 64 kbytes. The program memory will still be confined to 64 kbytes (at page 0), but the data memory can use all 256 pages.

Henrique S. Malvar, Assistant Professor, Departamento de Engenharia Eletrica, Universidade de Brasilia, 70910 Brasilia, DF, Brazil.



2. Since the most significant address bit is not required to define local or main memory, this hardware modification will permit the addressing of up to 64 kbytes by the Z80's 16-bit address (a). Only two instructions are required to address the entire main memory, as shown in the timing diagram (b).

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CIRCLE 72

IdeasForDesign

Power-line phase detector automatically switches loads to correct lines

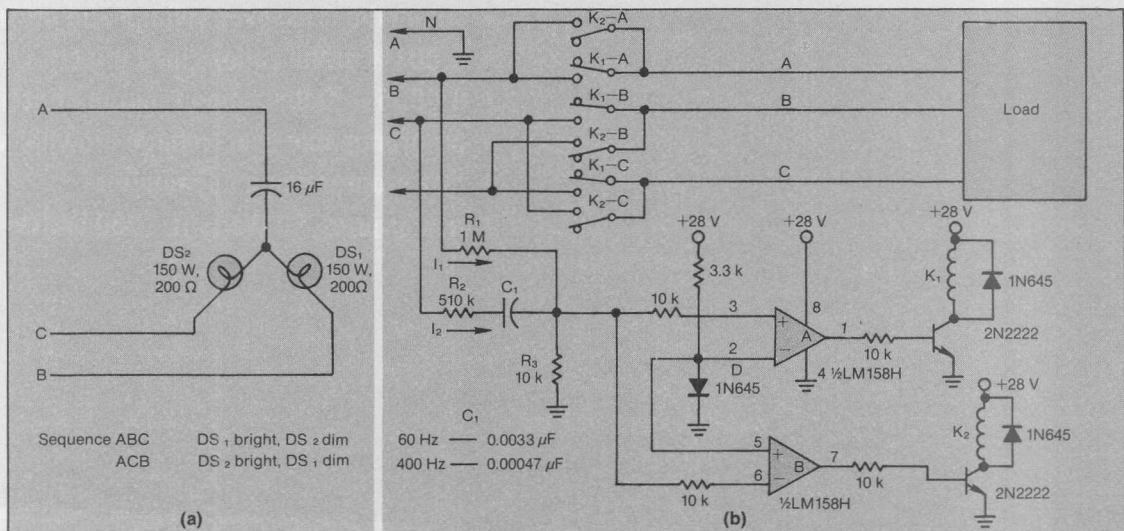
Damage to control and power systems, caused by incorrect hookup to a three-phase system, can be prevented by using this simple automatic phase detector and sequencer. Although the power-line phase sequence can be easily determined with just two light bulbs and a capacitor (a), circuit (b) prevents operator errors by detecting the phase and then automatically making the correct connection.

The industry-standard phase sequence is ABC, with B and C each lagging their predecessors by 120°. In the circuit, a 1-M Ω input resistor, R_1 , connected to line A, provides a current (I_1) of 0.115 mA (assuming a 115-V rms line-to-neutral system). Resistor R_2 and C_1 form an impedance of 1 M Ω , resulting in a current, I_2 , of 0.115 mA. This current, by virtue

of C_1 , leads the line B voltage by 60°. If phase B lags phase A by 120° (sequence ABC), I_2 will lag I_1 by 60°. Added vectorially, I_1 and I_2 produce 0.2 mA. This current develops 2 V across R_3 , which in turn fires comparator A and relay K_1 to apply the correct ABC sequence to the load.

If phase B leads phase A by 120° (sequence ACB), currents I_1 and I_2 will be 180° out of phase. The currents will cancel and there will be no voltage across R_3 . Comparator B will fire and energize relay K_2 . The correct ABC sequence will again be applied to the load. Diode D supplies a 0.6-V reference for the two comparators.

Stan Rubin, Senior Engineer, Ragen Data Systems, 3 Oval Dr., Central Islip, NY 11722.



A phase-detector circuit automatically connects a load to its proper lines. The voltage developed across R_3 determines which comparator and relay will fire to connect the proper phase sequence to the load. The currents I_1 and I_2 , which add vectorially to produce the voltage, are determined by the line's phase sequence. Since the neutral line is connected at all times, all hot lines must be switched simultaneously.

Winner for September 3, 1981

"PLL synchronizes switchers to end intermodulation noise"

Paul M. Baggenstoss, Design Engineer,
Raytheon Co., Submarine Signal Div., P.O. Box 360,
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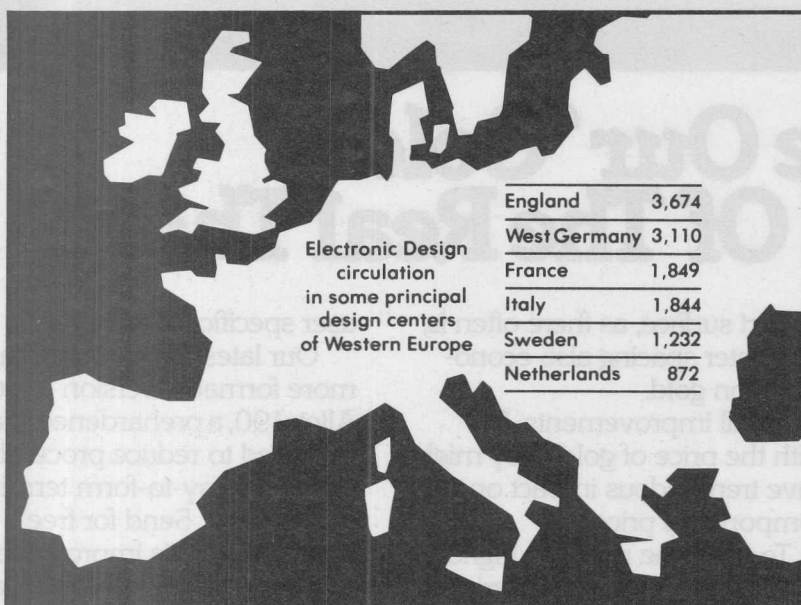
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Products

Built entirely out of CMOS components, this development system for the 1802 family speeds things up with a color display.

Low-cost development system uses color for speed

Low power, low price tag—and a color display for fast and easy program development: All characterize the CDP18S695 development system. Developed by RCA for the 1802 family of microprocessors and costing just \$1499, the all-CMOS development system consists of a 10-in. color monitor, a full alphanumeric keyboard, two cassette-tape recorders, a card cage, and four microboards. The four include a CPU card, a combined memory and tape controller board, a video-display board, and a PROM programmer board.

Color offers several advantages over monochrome displays: It permits faster and easier screen editing, because inputs and responses can be different colors; cursors and prompts can be different; and colors can be used to show the programming mode.

What's more, since the entire system uses CMOS technology, the power needs are so low that the entire power supply for the boards consists of a plug-in wall transformer.

Software that comes with the system includes ROM-based floating-point Basic, some system utilities, and an 1802 assembler-editor. Included on cassette is the control software for the PROM programmer and an interpreter



for RCA's VIS CRT-control chip set.

Thus, the system can be used to develop software not only for 1802-based microprocessor systems, but also for systems that will use the video display chip set. The development system serves as a hardware test bed that makes custom display-control software easy to develop.

The VIS chip set offers a flexible color CRT controller, which has a programmable character font, an audio output, and a video-overlay capability. Also fabricated in CMOS, the VIS chips offer the lowest power dissipation of any of the available chip sets on the market.

In addition to the firmware in ROM or on cassette, RCA offers

a time-share users' group, which operates over the CompuServe Infocservices Network based in Columbus, OH. When a user buys the CDP18S695 (or the smaller 18S693 and 694, the disk-based 008, or one of the VP-3300-series terminals), it comes with some documentation and a coupon good for one hour of nonprime-time connection to the CompuServe system. The user need only load the desired communications software and connect a modem to the development system.

Exhibited for the first time at Wescon/81, the color development system is now available from stock.

RCA, Rt. 202, Somerville, NJ 08876. Ed Folger (201) 685-7363.

CIRCLE 306

Dave Bursky, Senior Editor

A μ C board, memory boards, and remote I/O boards add up to a multifaceted system for process control and instrumentation.

Boards mate industrial control with 68000 capability

Industrial process-control and instrumentation applications now have easy access to the high-performance 16-bit 68000 microprocessor. The link is a series of board-level products revolving around a 68000-based microcomputer board (ELECTRONIC DESIGN, Sept. 17, 1981, p. 32).

Besides the VM02 board, there are the VM90 combination memory, I/O, and time-of-day clock module; the VM11 dynamic-RAM board; the RAD1 remote intelligent a-d converter module; the R101 remote digital I/O board; and the RSC1 remote serial converter module.

The microcomputer board's

local bus ties-on the three remote cards, for the system's real-time interfaces. Other peripherals—say, extra memory, I/O, counter-timers—connect to the microcomputer board via a VERSAbus.

The VM02 board offers standard 68000 performance features: 56 instruction types; memory-mapped I/O; 14 addressing modes; 16 32-bit data, address, and stack registers, five data types including bit, byte, word, long-word, and BCD; 256 multilevel vectored interrupts; and interlock instructions to handle multiprocessor operation.

To expand system memory beyond 256 kbytes, the designer can add one or more of the 512-kbyte VM11 dynamic-RAM

boards. Packed full of 64-k RAM chips, the memory also contains error detection and correction in the form of a modified Hamming Code, to detect all multibit errors and correct any single-bit faults. The VM80 board provides up to 128 kbytes and 256 k of extra ROM/PROM/EPROM; three 24-bit programmable timer/counters; two multiprotocol RS-232C serial-I/O ports, and six parallel I/O ports.

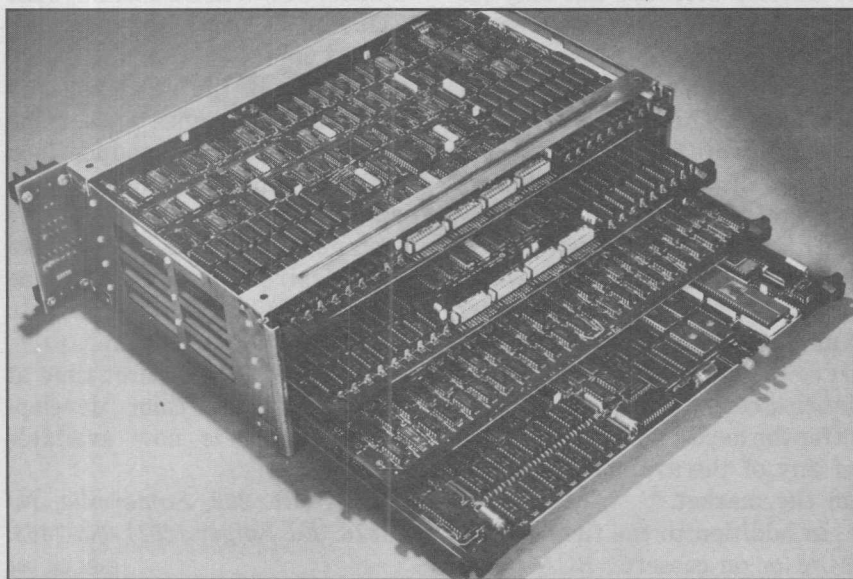
To connect to real-time process control, the RAD1 a-d-conversion module provides 32 single-ended or 16 differential a-d channels. Converter features include 0 to 10-V and ± 10 -V conversion ranges with 0.05% full-scale accuracy, 12-bit conversion at 25- μ s conversion time, ± 100 -V input and ± 32 -V channel-to-channel voltage protection, and 80-dB rejection for both common-mode and channel-to-channel crosstalk.

The other remote I/O board, the RI01, has its own 6809 8-bit microcomputer for interface to the main system microcomputer. The board accepts any mix of up to 16 Crydom Series 6, Opto-22, or other compatible solid-state relay input and output modules.

In single quantities, the cards range from \$180 to \$6000.

Motorola, 2200 W. Broadway Rd., Mesa, AZ 85202. Bill Crawford (602) 962-2156.

CIRCLE 311



Jonah McLeod, Instruments Editor

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For more information, call or write Fairchild about the 93422A and the 93L422A. Fairchild Bipolar Division, Drawer #7283, Mountain View, CA 94042. Telephone: (415) 962-3951. TWX: 910-379-6435.

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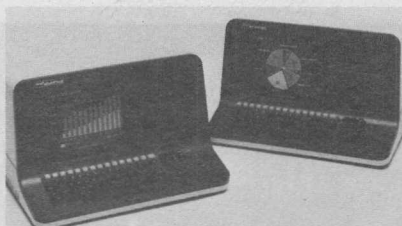
RAMs that really make tracks.

Desktop computer puts graphics within reach

A compact stand-alone desktop computer from North Star called the Advantage produces pie charts, bar diagrams, and three-dimensional graphic images on its 12-in. bit-mapped display—all for under \$4000.

The unit is built around a 4-MHz Z80 and 64 kbytes of RAM. An additional 20 kbytes of RAM supports the bit-mapping features. Along with the main CPU, the Advantage contains a 2-kbyte bootstrap PROM and an auxiliary 8035 microprocessor to control two 5¼-in. floppy-disk drives and an 87-key Selectric-style keyboard that reside within the system enclosure.

The 12-in. display shows up to 1920 characters in a 24-line, 80-column format. Graphics up to 240 × 640 pixels in size, with a resolution of 1 bit/pixel, are dis-



played on the CRT's P31 green-phosphor screen.

Nine symbol or control keys, 49 standard typewriter keys, a 14-key numeric/cursor control pad, and 15 programmable function keys incorporated on the system's keyboard are protected against n-key rollover—entry error caused by near-simultaneous depression of several keys.

Six slots in the unit's chassis accommodate plug-in cards to provide both a parallel interface for external printers or hard-disk drives and an RS-232 serial in-

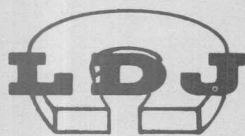
terface. An optional proprietary board performs floating-point arithmetic with 14-digit results.

Graphics CP/M, a compatible superset of CP/M, allows users to take full advantage of extensive graphics and also run all CP/M-compatible software. Graphics include four distinct geometric functions to draw points, lines, and numerous two-dimensional figures.

An extensive series of application software modules, including a managing operating system called ASP, written in the C language performs general ledger and accounting and inventory functions, word processing, and mailing-list preparation.

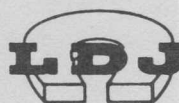
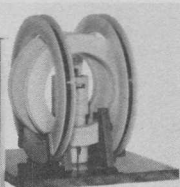
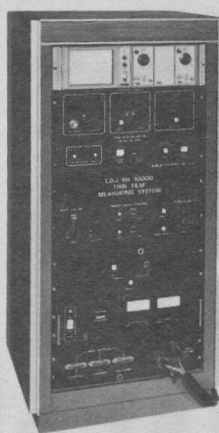
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CIRCLE 305



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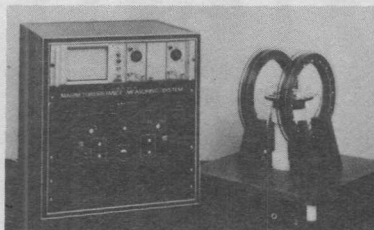
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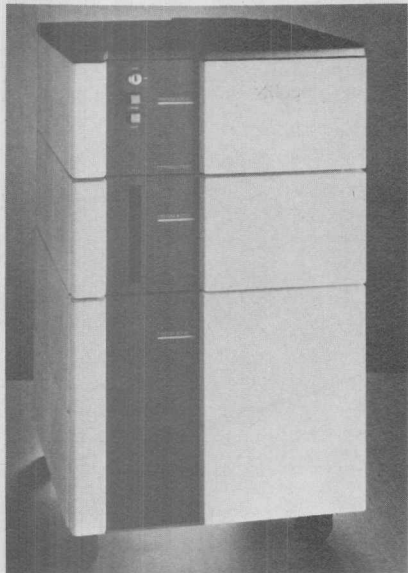


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16-bit computer based on UNIX serves business



A multiuser 16-bit computer system based on ZEUS, an enhanced version of the UNIX operating system, the System 8000, comes prepared for the general business environment. Operating-system enhancements include a visual editor utility suited for word-processing and other text-oriented applications such as general accounting, electronic mail, and MIS reporting. In addition, the system handles random records in large files (up to 1 Gbyte). The enhancements do not affect the UNIX kernel; therefore, UNIX programs developed on other systems can be transported. A CPU card based on a 6-MHz segmented Z8001A processor features three on-board memory management units that support segmented or non-segmented processes. The system supports up to 1.5 Mbytes of error-correcting memory, implemented in 256-kbyte memory array cards. Up to four 24-Mbyte, 8-in. Winchester disk drives and 17-Mbyte cartridge tape backup units are handled by two controller boards. The standard system configuration includes eight serial synchronous/asynchronous communication ports.

support eight serial lines each are optional. The basic system, the Model 20, includes the CPU board, two drive controllers, 256 kbytes of ECC memory, one 24-Mbyte Winchester disk drive, one 17-Mbyte cartridge tape drive, eight serial I/O ports, and all ZEUS software.

Zilog, 10340 Bubb Rd., Cupertino, CA 95014. (408) 446-4666. \$29,950.

CIRCLE 315

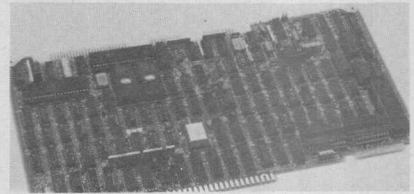
Manager monitors 768-channel network

The Alpha Star network manager, a floppy-disk-based micro-computer, permits users to monitor and control from a single site a statistically multiplexed data communications network consisting of up to 768 channels transmitting over as many as 32 independent data links. The manager operates through the supervisory port of up to 16 Timeplex Series II multiplexers to permit any one of the units to act as the control station. The manager automatically and continuously checks all data links and creates and stores a statistical data base on system operations. A report generated from the data base is automatically printed out every 24 hours, or at any time by operator command. The report indicates what links, if any, are degrading and at what rate. The report also shows the level of system activity for each data link. The manager comes in two configurations: ASM-1, which includes a controller, video terminal, printer, and desk console; and ASM-2, which consists of a rack-mountable control unit and a terminal.

Timeplex, Inc., 1 Communications Plaza, Rochelle Park, NJ 07662. (201) 368-1113. \$14,500 (ASM-1), \$13,700 (ASM-2); 13 wks.

CIRCLE 316

Multibus board controls hard and floppy disks



A single controller board that fits Multibus backplanes, the FWD8001, supports two Shugart SA1000 or Quantum 2000 8-in. Winchester disk drives plus two Shugart 800/850 floppy-disk drives to interface over 70 Mbytes of storage. The controller operates with single-head and double-head floppy-disk drives that use IBM 3740 single-density or IBM 2/2D double-density formats. In addition, the board supports the Intel 202 double-density format to permit program and data exchange with the Intel development systems.

Scientific Micro Systems, Inc., 777 E. Middlefield Rd., Mountain View, CA 94043. (415) 964-5700. \$1400 (100 qty); 7 to 9 wks.

CIRCLE 317

STD bus CPU card incorporates M6809

A CPU card compatible with the STD bus, the 7911/CP9, incorporates Motorola's M6809 microprocessor and 1 kbyte of RAM, which is expandable to 4 kbytes of on-board program support in 1-k increments. Interface with external RAM via the bus expands the primary system memory to 64 kbytes. Sockets on the card accept 2716 or 2732 EPROMs. A secondary memory mapping feature allows bank selection under software control for enabling additional associated memory and I/O cards.

Matrix Corp., 1639 Green St., Raleigh, NC 27603. (919) 833-2837. From \$240 (100 qty); stock to 2 wks.

CIRCLE 318

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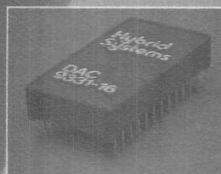
Our completely sealed package features a unique combination of materials that prevent any mismatch in thermal coefficient due to temperature extremes. Surface cracks, loose pins, and many other weaknesses typical of ordinary packages are eliminated. All components are arranged in an open cavity, away from messy epoxy, thereby knocking out mechanical strain, chemical degradation, and moisture problems.

The result is data conversion products so reliable, they've moved up to a class of their own. In this new class, the powerful winning combination of price/performance is in the hands of no one else but Hybrid Systems. The Contender.

We mean it when we say we're the Contender. We know we're going to have to work even harder to get you into our corner. But once you see what we can do, you'll make going with Hybrid Systems a unanimous decision.

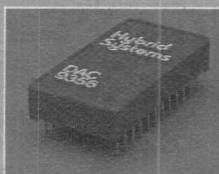
Call us today at (617) 667-8700, or write Hybrid Systems Corporation, 22 Linnell Circle, Suburban Industrial Park, Billerica, MA 01821.

The Contender Weighs In With Five Knockout Products



DAC 9331-16

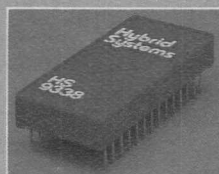
The first D/A converters with 16-bit resolution and linearity using monolithic I/C technology. Puts everyone else with 2"x4" modules down and out for the count.



DAC 9356

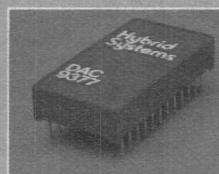
DAC 80 compatible. Lowest cost, complete, low-power, 12-bit D/A converter available.

The one to have in your corner when building systems that employ several DACs.



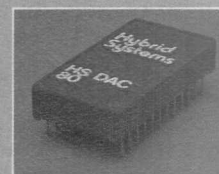
HS 9338

Complete, microprocessor-compatible, memory-mapped, 12-bit, double-buffered D/A converter. An all-around winner.



DAC 9377

Complete, buffered, voltage output D/A converter with 16-bit resolution and linearity. Flattens the competition's best price.



HS DAC 80

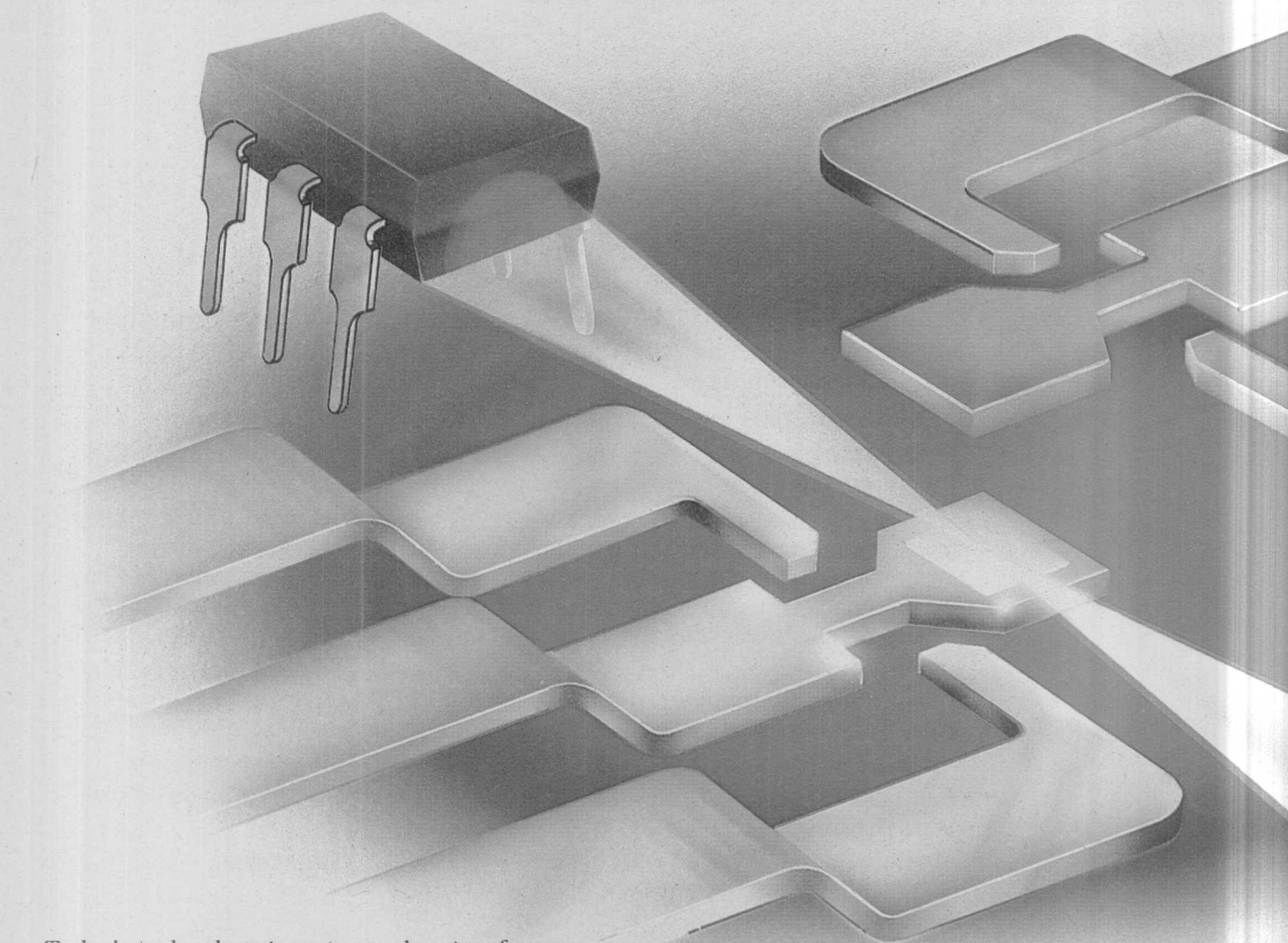
Low cost general purpose 12-bit D/A converter packaged in a 24-pin DIP. This one-two combination of price and performance has the "heavyweights" on the ropes.

Hybrid Systems

CORPORATION

Technological leadership.

Motorola presents the It's the beginning of the end



Today's technology in optocouplers is a far cry from the early days of simple, discrete, emitter-to-detector light transfer in a plastic box.

For many years Motorola's been the industry innovator and leading-edge source for advanced coupler technology, premium isolation protection, superior current transfer ratios and unique, complex functions with significant design advantages.

Now we eliminate the biggest coupler bugaboo of all, one that's consistently troubled designers seeking true, long-term performance and reliability — IRED degradation — and offer you couplers with phenomenal long-term performance and reliability.

Light-years of performance.

Crystal-stress, assembly damage, impurities and improperly designed metallization can alter the light-emitting mechanism leading to inefficiency and too-early, and observable, degradation.

And, if the IRED slips to less than 50% of initial current-transfer ratio, sometimes within a few hundred hours, the circuit's in trouble.

Motorola technology solves all this through exclusive use of Liquid Phase Epitaxial processing allowing stress-free, GaAs crystal growth...errorless, automatic die and wire attach...continuous process audit to monitor LED life characteristics...assembly-integrated die passivation...and non-mobile aluminum contacts to ensure junction integrity.

The detector's top-quality too, with stable, reliable devices resulting from conservative real estate design, nitride passivation, metal relief plates over critical areas and automatic assembly.

The effectiveness of what we've done is summed up like this: after 1.5 million device hours of documented, accelerated, long-term stress testing only 10% of the IREDs had degraded anywhere near marginal capability. And even these could still acceptably perform their functional purpose.

The package makes it perfect.

Motorola provides an all-transfer-molded, 6-pin DIP unit uniformly constructed with epoxy. No

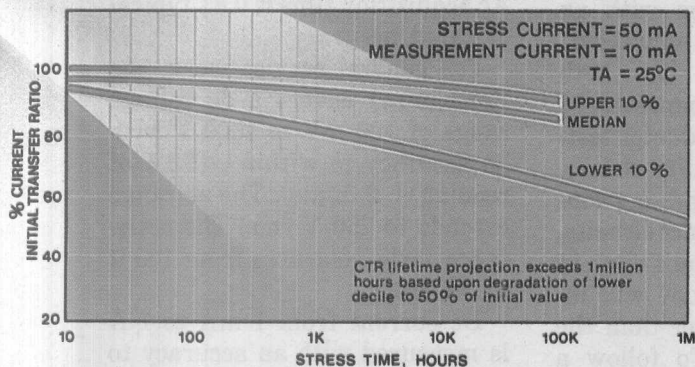
million-hour optocoupler. for IRED fadeout.

WHAT WE TESTED —

Group	IRED Sample Size	Number of Hours
A	108	168, 500, 1K, 2K, 3K
B	200	500, 2K
C	26	168, 500, 1K
D	53	168
E	49	168, 500, 1K
F	50	168, 500, 1K
G	322	500, 1K
H	38	168, 500, 1K, 2K
I	86	168, 500, 1K
J	100	168, 500, 1K
	1032	*

*1,441,904 Total Device Hours

WHAT THE RESULTS WERE —



glass or plastic slides, no air gaps, no tradeoffs. Our innermold encompasses almost 60% of the coupler body, providing as much as 10 times the interface distance of competitive designs, and results in mechanically and electrically stable construction with excellent integrity and stability. It's the best-designed coupler package you can get.

Minimum spec'd isolation voltage is 7.5 kV peak — on every Motorola unit. They're UL-recognized at 5 kV. File No. E54915.

Applications unlimited.

Motorola has more optocouplers specifically designed for AC line control than anyone else. SCR and Triac output types. Standard and zero-crossing, 250 and 400 V. Standard and sensitive-gate. Plus 4N's, H11's and TIL's. And, our production capacity's doubled within the past year to meet the explosive growth facing the optical coupler industry.

COUPLER	OUTPUT	TRIGGER CURRENT mA-Max	BLOCKING VOLTAGE V-Pk-Min
MOC3002	SCR	30	250
MOC3003	SCR	20	250
MOC3007	SCR	40	200
H11C1	SCR	20	200
H11C2	SCR	20	200
H11C3	SCR	30	200
MOC3009	Triac Driver	30	250
MOC3010	Triac Driver	15	250
MOC3011	Triac Driver	10	250
MOC3020	Triac Driver	30	400
MOC3021	Triac Driver	15	400
MOC3030	Triac Zero Cross Driver	30	250
MOC3031	Triac Zero Cross Driver	15	250
MOC3040	Triac Zero Cross Driver	30	400
MOC3041	Triac Zero Cross Driver	15	400

They're all available from one of the industry's largest distributor network, in quantity, at competitive prices.

Contact your local source or write Motorola Semiconductor Products, Inc., P.O. Box 20912, Phoenix, AZ 85036 for complete data, a free copy of our new Optocoupler Reliability Report or the new Motorola Optoelectronic Data Book for just \$3.25.

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CIRCLE 80

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Beeping DMM snares fast pulses for logic testing

With the addition of logic testing facilities and a fast peak-hold function, the Roadrunner II handheld digital multimeter from Weston Instruments becomes the only piece of test equipment needed for a wide variety of field service work on microcomputer systems, peripherals, and business machines. One of a new breed of "audio-response" testers, the Roadrunner II gives its user six functions in 29 ranges. Measurements are displayed on 3-1/2 digit, 0.5-in. LCD readout.

The instrument catches logic pulses as fast as 100 μ s and is TTL-level compatible, making it the right tool for testing the majority of present-day digital IC circuits. Pulse-stretching and peak-hold capabilities, for voltage and current changes as fast as 50 ms, make it possible to detect very brief nonrepetitive deviations. As with its analog testing functions, the Roadrunner II alerts its user to threshold crossings with an audible and a visual indication.

Threshold levels for both audible and visual response can be set at 2 V for semiconductor testing, at 2 Ω for continuity checks, and at 20 Ω for determining continuity in high-resistance circuits. With its mode-selection switch in the "A" position, a tone will indicate an input greater than the selected threshold. To follow a value which drops below a threshold, the mode switch is placed in the "V" position. Both annunciators, on simultaneously, indicate a voltage passing through the threshold. Voltage or resistance below a threshold appears as a "V" annunciator.

Harold Winard, Associate Editor



The peak-hold function, used for measuring transient signals, offers accuracies to within $\pm(3\%$ of reading + 15 digits). Acquisition time for a square pulse is typically 30 ms, 50 ms maximum. Ac acquisition time is 0.8 s typical of rated accuracy.

For general service work, the Roadrunner covers a dc voltage range of 100 mV to 1000 V with an accuracy to within $\pm(0.1\%$ of reading + 2 digits). The ac range extends to 750 V rms. The resistance scale measures from 100 Ω to 10 M Ω .

Dc current from 1 mA to 1 A is measured with an accuracy to $\pm(0.5\% + 1 \text{ digit})$. Ac current accuracy is to within 1.5%, ± 3 digits from 1 mA to 1 A.

The Roadrunner II costs approximately \$240 and is available from stock.

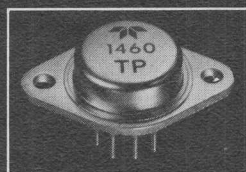
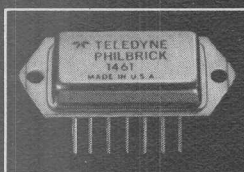
Weston Instruments, 614 Frel-inghuysen Ave., Newark, NJ 07114. (201) 242-2600.

CIRCLE 308

WHO WAKES THE ONLY VMOS POWER OP AMPS?

 **TELEDYNE PHILBRICK**

Call them high speed op amps with more muscle than previously available or power op amps with more speed than previously thought possible, but Teledyne Philbrick's 1460 and 1461 are still the first and only op amps with VMOS FET output stages. SOA restrictions and secondary breakdown problems are no longer a concern. The 1461 has a FET input, a guaranteed $\pm 30V$, $\pm 600mA$ output, an incredible $1200V/\mu sec$ slew rate, and an astonishing $1GHz$ GBW product ($15MHz$ operating bandwidth). The 1460 has a guaranteed $\pm 30V$, $\pm 150mA$ output, a $300V/\mu sec$ slew rate, and a $1GHz$ GBW product. Teledyne Philbrick is a leading manufacturer of precision, high speed and high power op amps for both military and commercial applications. We also manufacture extremely fast A/D-D/A converters, V/F-F/V converters and S/H amplifiers.



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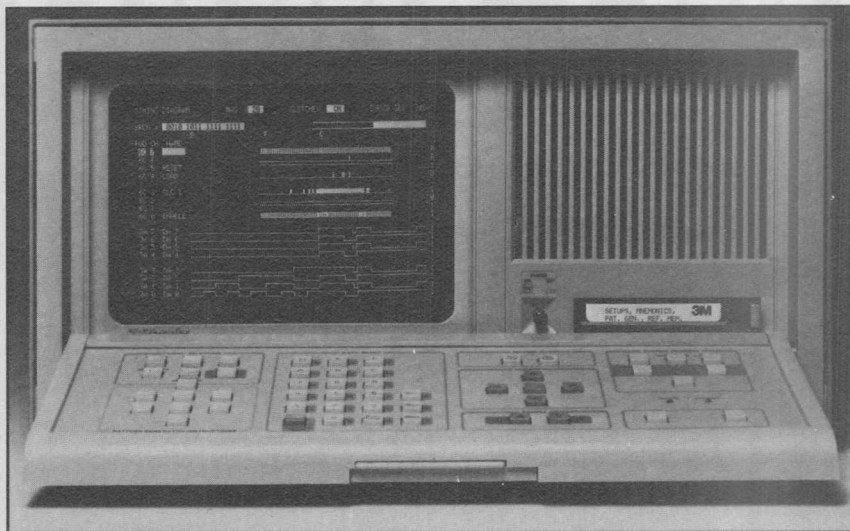
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INSTRUMENTS

Plug-in modules make logic analyzer flexible



By incorporating various plug-in cards, the Tektronix DAS 9100 digital circuit analyzer integrates pattern generation, logic analysis functions, mass storage, and communications interfaces in one instrument to debug logic systems before the prototype stage. Modules combined in the instrument's six-slot cage set the analyzer to monitor up to 104 logic channels, sample synchronous and asynchronous data channels at rates up to 330 MHz, and generate test pulse patterns on as many as 80 channels at up to 25 MHz.

Three data-acquisition modules serve different system development applications. One card lets the analyzer resolve 40-ns pulses on 32 separate channels at a 25-MHz sample rate, retains 512 bits/channel in memory, and provides two clock qualifiers. An eight-channel module provides 10-ns-pulse resolution for 100-MHz sampling, separate data acquisition and glitch memories, and one clock qualifier. A four-

channel module provides 3-ns resolution for 330-MHz operation, retains 2048 bits/channel in memory, and resolves pulses as short as 1.5 ns on two channels.

The pattern generator module for the DAS 9100 supplies pulse sequences to stimulate the memory and I/O ports of systems under development, or simulate microcode. A single card generates patterns on 16 channels at 25 MHz. The addition of one or two 32-channel expander modules extends the total to 48 or 80 channels of patterns with up to ten programmable strobes. An external clock or the internal program-selectable timebase controls pattern timing.

An optional RS-232 port and GPIB interface allows remote control of the instrument and transfer of channel data to another DAS 9100. The DAS 9100 mainframe with integral 9-in. CRT is priced at \$4950; modules start at \$3500.

Tektronix, Inc., P.O. Box 500, Beaverton, OR 97077. (503) 644-0161.

Ed Connolly, New Products Editor

CIRCLE 309

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high-speed, high-impedance probes; a nonvolatile, 1000-word, reference memory and the ability to search for strings up to 16 words long.

Monitor feature keeps logic analyzer logical

All too often with test instruments, the price of increased capability is increased operating complexity, which can nullify the performance improvements—or worse. That is not true, however, with Dolch's latest logic analyzer—the LAM4850A. On the contrary, the 48-channel, 50-MHz instrument adds features that actually make it easier to use than its predecessor.

It incorporates a so-called monitor function that lists status information and comments in an easy-to-understand format that the operator can call up any time by depressing the MONITOR key on

the instrument. When the key is pressed, the analyzer displays an interpretation of the menu shown on the unit's screen. It explains variables to be set up on the instrument and interprets any error messages the operator receives during operation. Moreover, it alerts the operator to incorrect connections made to the system under test.

For the operator's convenience, up to six test setups can be stored for months in nonvolatile CMOS memory in the analyzer.

Another convenience that has been added is a new type of fast general-purpose probe. It offers an input impedance of 1 M Ω in parallel with 10 pF, allowing

glitches of 5 ns or greater to be captured easily. In addition, a virtual grounding system inside the analyzer eliminates ground loops and noise pickup.

Also improved is the instrument's triggering capability. One new mode offers 12 levels of triggering with interaction for selective tracing, including Boolean combinations. Three trigger words, each 48 bits wide, can be logically combined on every sequential step.

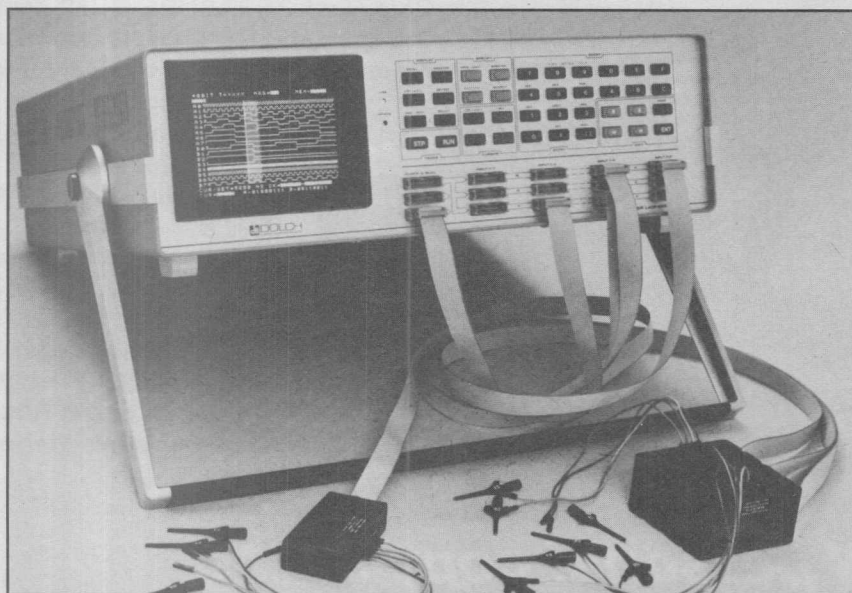
Yet another new feature is the instrument's ability to search for strings up to 16 words long. Thus a single event, as well as complex sequential program conditions, can be identified. With the analyzer's full-size reference memory (1000 \times 48 bits), stored data can be compared with newly recorded data and any differences can be highlighted.

In the auto-comparison mode, the memory continually compares newly recorded data with that in reference memory and signals when any mismatch occurs. Such comparisons are especially useful in finding intermittent problems in a design.

Priced at \$11,750 for a single unit, the LAM4850A is available 30 days after order.

Dolch Logic Instruments, 230 Devon Dr., San Jose, CA 95112. Jesse King (408) 998-4633.

CIRCLE 302



Jonah McLeod, Instruments Editor

Wafer inspector finds 0.3- μ m contaminates

A cassette-fed wafer-surface inspection system, the C1628, detects, sizes, and locates particulates as small as 0.3 microns on 2 to 5-in. semiconductor wafers, then displays or prints the complete results within 5 to 7 seconds. A cassette-to-cassette wafer transport system eliminates manual handling and the related danger of accidental contamination during inspection and sorting. The wafer inspection system finds point, scratch, haze and other defects in addition to contaminates. An RS-232 interface connects the system to a host computer to communicate X-Y coordinates, relative defect size, and histograms for subsequent compilation.

Hamamatsu Systems, Inc., 332 Second Ave., Waltham, MA 02254. (617) 890-3440.

CIRCLE 321

True rms VA meter has peak-hold function

The hand-held 3½-digit Model VAM meter measures true rms ac voltage and current up to 1000 V and 2 A and provides a peak read and hold function. The instrument's peak-read and hold circuit acquires a peak dc signal within 10 ms or a peak ac signal within 100 ms and continues to display the value until reset. The meter provides four voltage ranges and four current ranges. Readings are accurate to within ½% on all ranges except the 2-A full-scale range, which has a tolerance of 2% \pm 1 digit. The meter provides a maximum resolution of 1 mV and 1 μ A.

Engineered Systems and Designs, 2011 Bayard Blvd., Wilmington, DE 19802. (302) 571-1195. \$225.

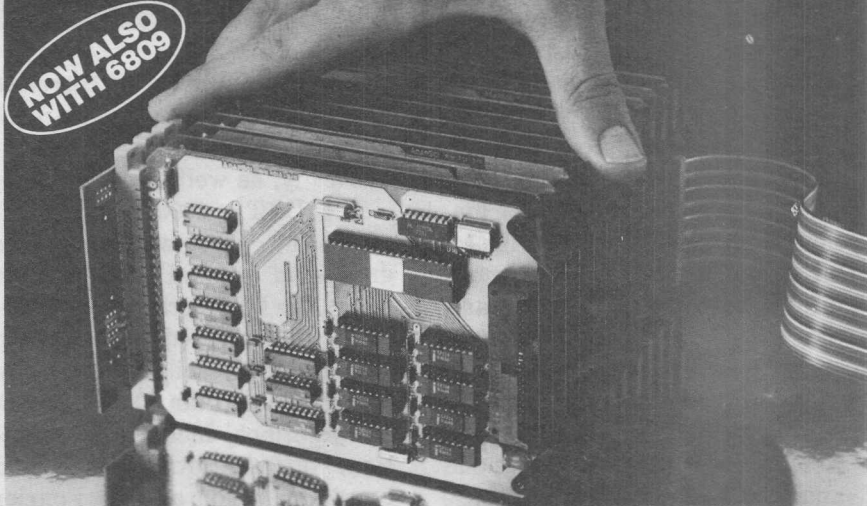
CIRCLE 322

ModulasOne puts a lot of micro-phistication in your hand. A compact 4½" x 6½" board set designed for sophisticated applications such as Data Monitoring, Data Capture and Display, Process Control and Television Reporting, ModulasOne offers a combination of high-quality hardware and turnkey

firmware support. Its high reliability is built around the 6800 microprocessor, and its rugged construction makes it ideal for operating in harsh environments. To find out more about ModulasOne write to Adaptive Science Corporation, 4700 San Pablo Ave., Emeryville, CA 94608. Phone 415-652-1805.

ModulasOne. The 8-bit microcomputer that's not for everybody.

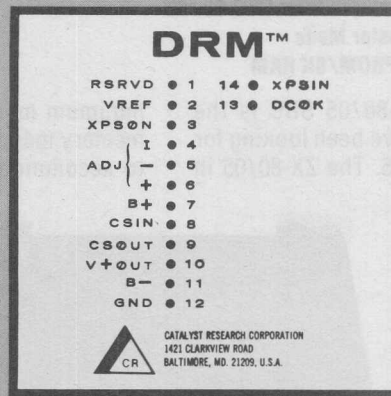
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CIRCLE 82

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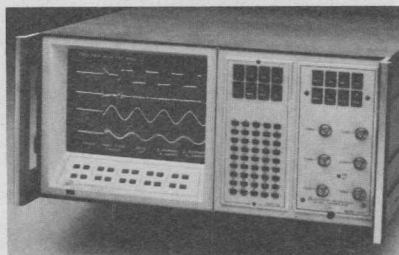
1421 Clarkview Rd., Baltimore, Md. 21209 U.S.A. TEL. 301/296-7000 TELEX #87-768

CIRCLE 83

Analog-signal analyzer goes beyond the scope

A portable instrument combining the features of a digital storage oscilloscope with a waveform analyzer, transient-signal analyzer, spectrum analyzer, and data-acquisition system includes a 16-bit microcomputer with 10-k data points of memory (expandable to 100 k); a CRT display; and a series of interchangeable plug-in data-acquisition, preamplifier and digitizer modules. The two announced front-end modules sample low-frequency information at 100 kilosamples/s with 14-bit resolution or high-frequency information at 100 megasamples/s with 7-bit resolution.

The instrument displays up to four traces simultaneously, which can be independently positioned; X-Y expanded or compressed; and analyzed using cross hairs, base line, cursor, and graticule. The



cursor may be used to correlate independently timed data. All measurements are displayed numerically, as well as graphically.

The DATA 6000 is programmable by the user from five groups of control keys located below the CRT screen. Key functions are displayed on the screen and can be easily changed to perform more than 300 front-panel operations, including integration, differentiation, auto and cross correlation, and fast Fourier transforms.

Waveform characteristics that can be displayed numerically include: period, frequency, rise time, fall time, delay, width, root mean square, area, energy, maximum, minimum, maximum slope, or threshold crossing in either direction. Live signals may be compared with signals from memory or disk. The inputs and outputs are compatible with both the IEEE-488 and RS-232 formats.

The price of the DATA 6000 without acquisition modules is \$4995. The low-frequency acquisition module costs \$1995, and the high-frequency module \$3995. They are available in 90 to 120 days.

Data Precision, Electronics Ave., Danvers, MA 01923. Ken Berquist (617) 246-1600.

CIRCLE 301

THE ZENDEX Model ZX-80/05 SINGLE BOARD COMPUTER

"ECONOMY, HIGH-PERFORMANCE 8085A-2 BOARD"

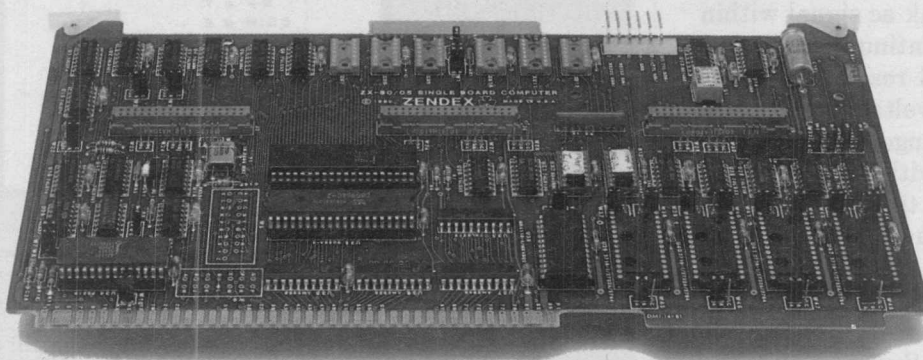
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The ZENDEX ZX-80/05 SBC is the replacement you've been looking for in Intel SBC-80/05. The ZX-80/05 in

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- Select standard or 5 MHz operating speed for CPU.
- Has three SBX-module positions
- 5V only operation

and program memory space you've needed. The ZX-80/05 can also be set to run double quick over the Intel.



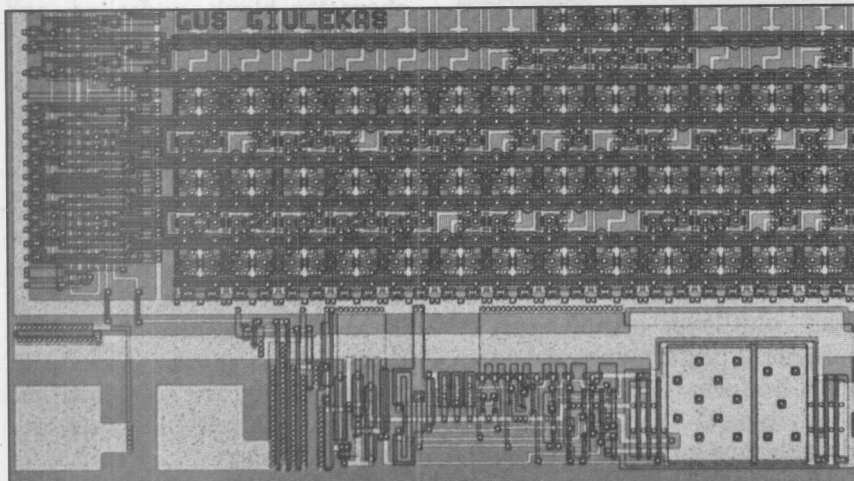
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Data-separator chip cuts controller chip count



A portion of the PLA, which controls the timing-correction circuitry of the floppy-disk data separator.

Cutting the discrete data-separation circuitry in floppy-disk systems back to a single chip, the FDDS from Standard Microsystems separates the single stream of pulses from a floppy-disk drive into clock and data inputs for a floppy-disk controller. The chip contains a clock divider, a long-term timing corrector, a short-term timing corrector, and reclocking circuitry.

Compatible with the 1791 and 1793 floppy-disk controller chips, among others, the FDDS (FDC 9216) eliminates several SSI and MSI devices normally needed to do the data separation. Able to operate from a 5-V supply, the circuit is TTL-compatible on all inputs and outputs.

An eight-pin mini-DIP houses the FDDS, with just six pins needed for signal handling. Three pins handle data and clock (one input data from the disk and the two separated data and clock outputs), and the other three pins are for a reference clock and two

clock-divider control pins.

Besides requiring a power-supply current of just 50 mA, the circuit can handle a maximum clock frequency of 8.3 MHz for the reference clock input. Rise and fall times on the clock signal can range from 50 to 2500 ns, and input capacitance on all inputs is only 10 pF. Two of the control pins let the user select the reference clock frequency to suit the type of drive the data will be coming from—single or dual density and 5¼ or 8-in. sizes can be handled by the same chip.

The circuit takes the reference clock (2 to 8 MHz) and divides it to provide the internal clock timing. The circuit detects the leading edges of the disk data pulses and adjusts the phase of the internal clock to provide the separated clock output.

The FDC 9216, in 100-quantity lots, costs \$6.85; delivery is from stock.

Standard Microsystems, 35 Marcus Blvd. Hauppauge, NY 11787. Brian Cayton (516) 273-3100.

CIRCLE 307

Dave Bursky, Semiconductors Editor

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68000 comes in JEDEC leadless chip carrier

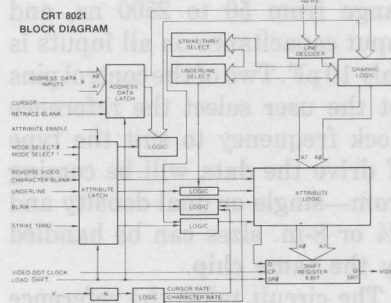


The MC68000Z8 now comes in a JEDEC type-C leadless chip carrier. The symmetry of the compact multilayer ceramic carrier makes the performance of devices more uniform than those in DIPs. The type-C package solders directly to a substrate or mounts in a socket. The chip carrier can also be adapted to leads.

Motorola Inc., MOS Integrated Circuits Div., 3501 Ed Bluestein Blvd., Austin, TX 78721. \$124 (100 qty).

CIRCLE 325

Chip provides graphics for CRT displays



The CRT 8021, an n-channel MOS/LSI IC, works in conjunction with a character-generator ROM to provide video attributes and graphics for a CRT display. The device processes and serializes parallel data from the character generator for direct connection to the video input of a CRT monitor. Attributes are added as desired to alphanumeric data, or data are converted into the desired graphic form. The chip provides two modes of graphics,

field and/or character attributes, a 20-MHz video shift register, blinking, reverse video, a cursor, and separate data and attribute latches. Attributes include reverse video, character blink, character blank, underline, and strike-through. The CRT 8021 provides an eight-part graphic entity which fills the character block. It helps form seven-dot-wide, nine or eleven-dot-high characters in 9×12 or 10×12 character blocks. Another version, the CRT 8021-003, provides a six part graphic entity for five-by-seven dot or five-by-nine-dot characters in character blocks of up to seven by ten dots. Both the devices come in 28-pin plastic and ceramic DIPs.

Standard Microsystems Corp., 35 Marcus Blvd., Hauppauge, NY 11787. (516) 273-3100. \$8 (100 qty); Stock.

CIRCLE 326

EEPROM gives flexibility to nonvolatile storage

The ER5716 EEPROM, which is organized as 2048×8 , gives the advantage of bulk erasability and in-circuit reprogramming to applications that require a 16-k memory for nonvolatile storage but also require occasional data changes, such as microprocessor program storage. The device permits block erasure with a 25-V pulse applied for 1 s. The memory reprograms at a rate of 1 byte/ms. In the read mode, the memory operates from a 5-V supply and provides a 300-ns access time. The EEPROM is interchangeable with the 2716 EPROM and is pin-for-pin compatible with the Hitachi HN48016.

General Instrument Corp., Microelectronics Div., 600 W. John St., Hicksville, NY 11802. (516) 733-3120.

CIRCLE 327

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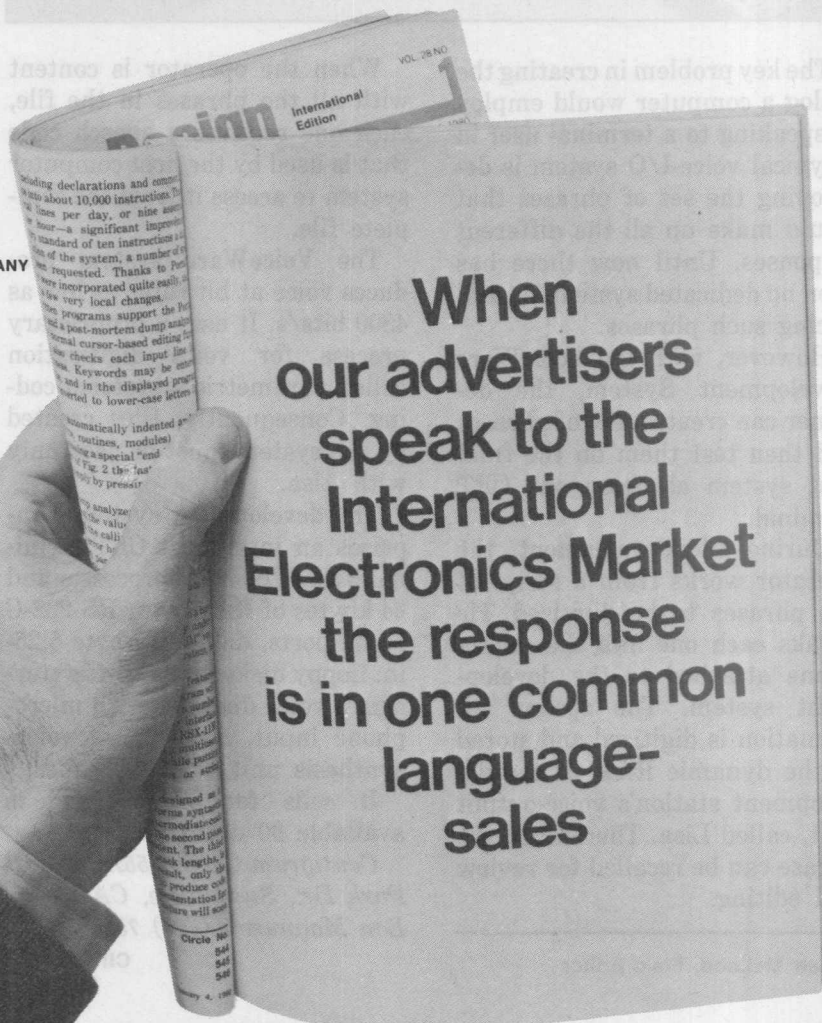
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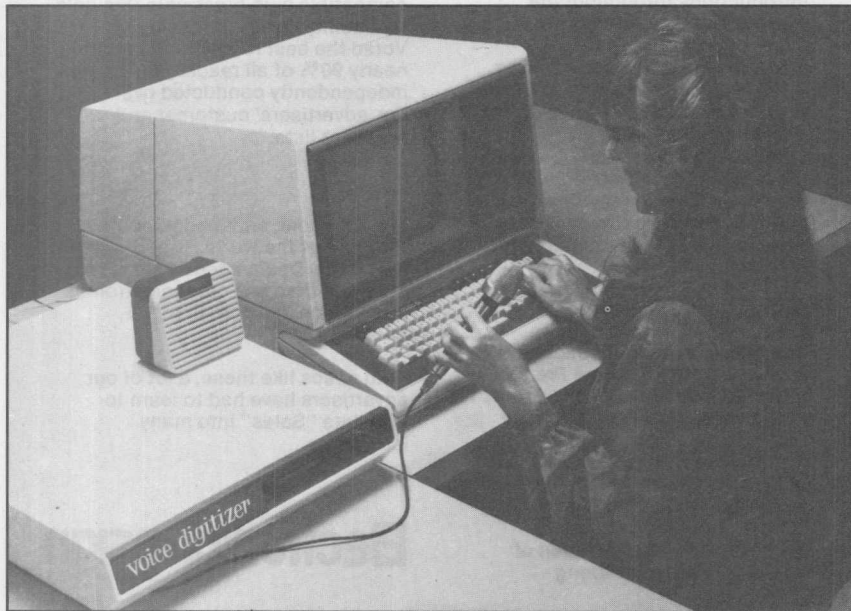
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Haruki Hirayama
EMS Inc.
Room 801, Shinjuku Komuro-Heim
1-22, Shinjuku 4-chome, Shinjuku-ku
Tokyo 160, Japan



Voice coach develops computers' lines



The key problem in creating the dialog a computer would employ in speaking to a terminal user in a typical voice-I/O system is developing the set of phrases that would make up all the different responses. Until now there has been no dedicated system for producing such phrases.

However, with the VoiceWare Development System, the designer can create a file of phrases and then test them on the final host system all from one CRT terminal.

During file development, the operator works from a script of the phrases to be digitized. He speaks each one into the microphone attached to the development system. The spoken information is digitized and stored in the dynamic RAM of the development station's voice-output unit, called Lisa. Thereafter, the phrase can be recalled for review and editing.

When the operator is content with all the phrases in the file, each one receives a speech code that is used by the host computer system to access it from the complete file.

The VoiceWare system produces voice at bit rates as low as 4800 bits/s. It uses a proprietary process for voice digitization called parametric waveform coding. Consequently, files created by the system must be used only with Lisa.

The development system comprises an intelligent CRT terminal with a Z80 microprocessor and 64 kbytes of RAM, four RS-232-C serial ports, dual 500-kbyte 5.25-in. floppy disks for voice-file storage, a voice digitizer with microphone input, and a Lisa voice-synthesis unit with a speaker.

It sells for \$25,000 and is available 90 days after order.

Centigram Corp., 155A Moffett Park Dr., Sunnyvale, CA 94086. Len Magnuson (408) 734-3222.

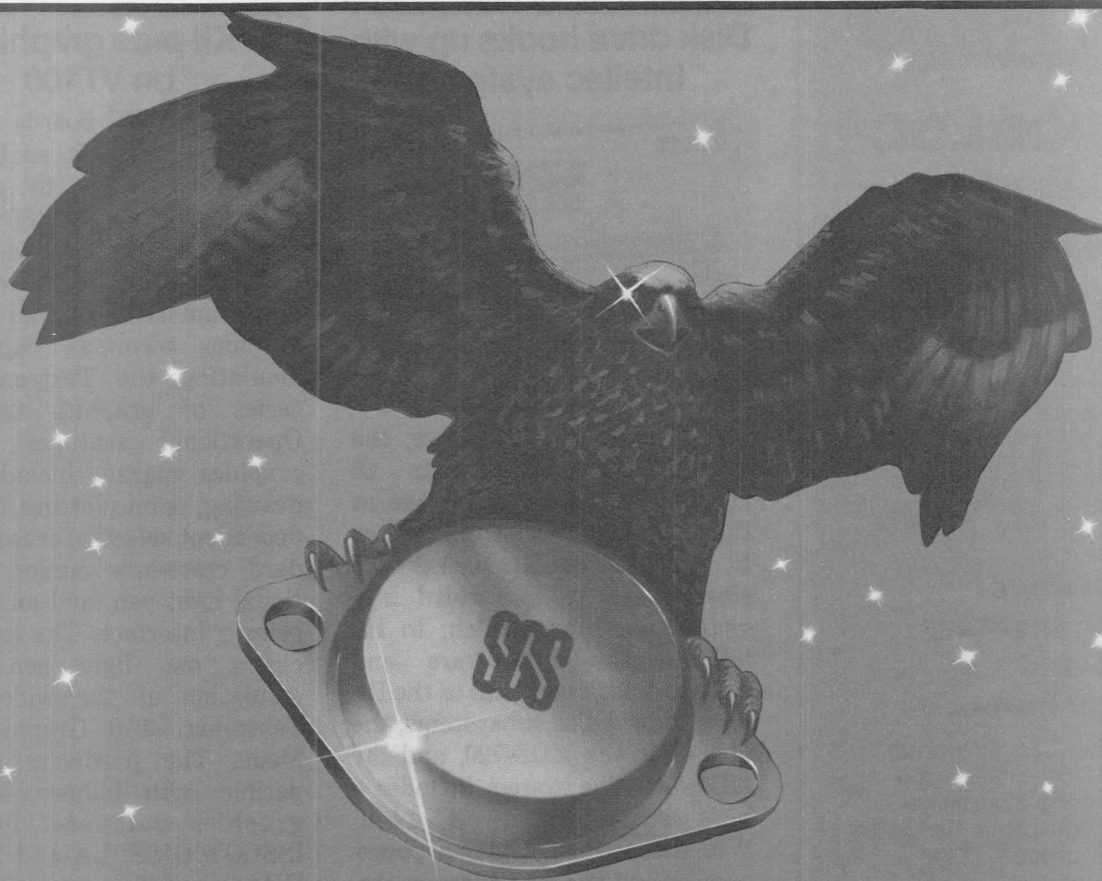
Jonah McLeod, Field Editor

CIRCLE 304

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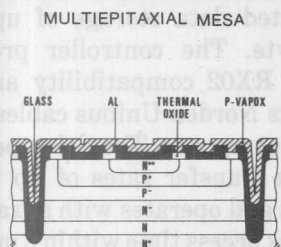


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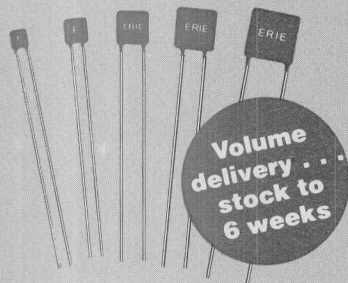
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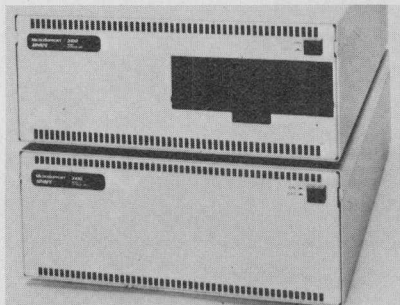
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CIRCLE 91

PERIPHERALS

Disk drive hooks up with Intellec systems



A Winchester disk drive, the MicroSupport 3100, puts 20 Mbytes of formatted storage at the disposal of Intellec 800, Series II, and Series III users. The storage system is divided into virtual partitions which, to Intellec system hardware and software, look identical to the Intel standard disk subsystems, the MDS-710, the MDS-720, and the MDS-740. The system includes a bit-slicer controller, a 14-in. Winchester disk drive, a power supply, and the host adapter. Optional systems support up to four hard-disk and two floppy-disk drives.

*Advant Corp., 696 Trimble Rd.,
San Jose, CA 95131. (408)
946-9300. \$8995; 4 to 6 wks.*

CIRCLE 328

Hard-disk drive stores 104 Mbytes for V77-800

A fixed-disk drive, the Model F3770, stores up to 70 or 104 Mbytes in Sperry Univac V77-500/700/800 minicomputer systems. Up to two drives interface with each system, using a single controller. The sealed, environmentally-controlled storage module includes a stack of 14-in. rack-mounted disks. Two read/write moving heads access both surfaces of each disk, allowing data transfer at a rate of 1.2 Mbyte/s.

*Sperry Univac, P.O. Box 500,
Blue Bell, PA 19424. (215)
542-4213. \$13,000.*

CIRCLE 329

Kit puts graphics on VT100

The three PC boards included in the VT640S kit enable DEC VT100 terminals to generate graphics with 640 \times 480-pixel resolution. Once installed, the kit lets the VT100 perform both as an alphanumeric terminal and as a graphics terminal, capable of emulating the Tektronix 4010 series of graphics terminals. Operational features of the graphics upgrade include vector drawing, point plotting, mode-independent selective erase, a standard cross-hair cursor, an optional light pen, and an optional printer interface. The cross-hair cursor and light pen permit emulation of the widely used Tektronix 4010 Graphic Input Mode. The hardware is compatible with industry-standard graphics software, including ISSCO's DISSPLA and TELLAGRAF, and Tektronix' PLOT 10.

*Digital Engineering, Inc., 630
Bercut Dr., Sacramento, CA
95814. (916) 447-7600. \$1230; 13
wks.*

CIRCLE 330

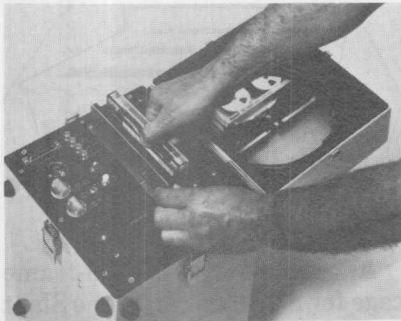
Military floppy-disk drive holds 1 Mbyte

A militarized floppy-disk drive for use with Norden PDP-11M and DEC PDP-11 computers, the DD400/DC400, provides a formatted data storage of up to 1 Mbyte. The controller provides full RX02 compatibility and accepts Norden Unibus cables from the computer. The drive permits data transfer rates of up to 500 kHz and operates with a track-to-track access time within 6 ms. The system comes qualified to MIL-E-16400 and includes MIL-M-38510/MIL-STD-883 B micrologic.

*Miltope Corp., 9 Fairchild Ave.,
Plainview, NY 11803. (516)
349-9500.*

CIRCLE 331

4.3-Mbyte cartridge drive meets MIL shock specs



A militarized cartridge-tape drive with an integral power supply and microprocessor-based formatter/interface unit, the Model 2765, meets the requirements of MIL-T-21200 and MIL-T-810C for shock and vibration. The drive stores up to 4.3 Mbytes and performs automatic error checking and automatic retry. A built-in heater allows the Model 2765 to operate at temperatures as low as -10°C . A sealed, hinged cover prevents dirt from entering the unit. The drive serves applications at airfields for commercial and military flight line operations, and airborne and land-based geophysical applications.

Qantex Division, North Atlantic Ind., Inc., 60 Plant Ave., Hauppauge, NY 11787. (516) 582-6060. \$10,365; 10 to 12 wks.

CIRCLE 332

Magnetic tape reduces PCM recording errors

A magnetic recording tape for instrumentation, the type 721, has a coercivity of 650 Oe. The tape reduces error rates in high-bit-density PCM recording and offers a signal-to-noise improvement of up to 6 dB over other gamma-ferric tapes. Controlled abrasion characteristics extend recorder-head life and reduce maintenance.

Amper Corp., 401 Broadway, Redwood City, CA 94063. (415) 367-4151

CIRCLE 333

Bar-code printer also puts text on labels

The 8425 bar-code printer interfaces with host minicomputers or terminals over an RS-232 interface to produce code 39 format codes on roll-fed labels or tags. In addition, the unit produces up to either five or ten lines of human-readable characters on each coded label. The printer employs a continuously rotating engraved print drum, electromagnetically actuated print hammers, and a dry carbon ribbon. The unit can be configured as a stand-alone printer by connecting a "dumb" terminal. The printer prompts operators with data fields, quantities, and increment/decrement instructions. A 32-character bar-code message with up to 350 characters of descriptive text can be printed on a 2.5×4 -in. tag.

Interface Mechanisms, Inc., P.O. Box N, Lynwood, WA 98036. (206) 743-7036.

CIRCLE 334

20-Mbyte streaming tape drives backup hard disks

A $\frac{1}{4}$ -in. streaming cartridge tape drive for use in Winchester-disk backup applications, the Quarterback, comes in two versions that operate at 30 or 90 in./s. The drives offer formatted data storage of either 10 or 20 Mbytes per cartridge. The units' intelligent controller relieves the host computer of overhead functions such as tape formatting, error detection and correction, file mark positioning, and tape positioning. The 90-in./s version transfers 20 Mbytes of formatted data onto a single cartridge in just over four minutes.

Cipher Data Products, Inc., 10225 Willow Creek Rd., San Diego, CA 92138. (714) 578-9100. \$1550.

CIRCLE 335

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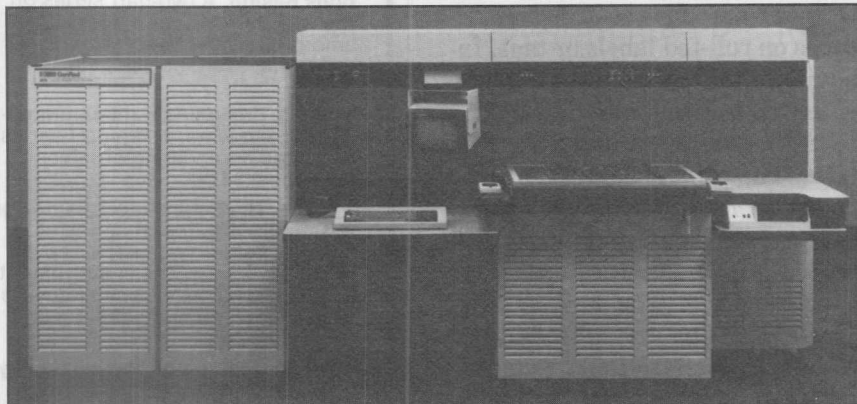
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IN-CIRCUIT TESTER WORKS WITH 3584 multiplexed pins



Normally, in-circuit test systems that can test up to 3500 pins cost a pretty penny and are large to boot—each pin requires its own driver and sensor electronics. The Model 2272 (see photo) from GenRad substantially changes that by offering 3584 hybrid pins and by multiplexing the pins so that one set of pin electronics drives more than one pin. (The Model 2271 does the same for 960 pins.)

Both the 2271 and 2272 offer true hybrid test capability at every pin. Each pin can be programmed to handle all major logic families, which makes mixed logic-family testing possible. In addition, each pin has a 270-kHz clock speed.

Besides improving the pin count at a reasonable cost per pin, the systems come with improved software capability. Release 7, part of the Automatic Test Generation (ATG) software package, offers a diagnostic procedure called BusBust, which identifies faults on bus-structured boards beyond a failing node to a defective component.

BusBust wiggles every component tied to the bus. If any one device is pulling the bus down, the

software automatically begins isolating the problem. In fact, the ATG software does all the test generation necessary to isolate the problem to the failing node. Furthermore, it can find multiple faults and works on all major logic families. All this is done without intervention.

Another software enhancement, this one provided in the analog-component library, enables a programmer to create component-description files for complex analog, multiple component, and custom devices. Having these high-level part descriptions reduces circuit description entry, improves ATG circuit analysis capability, and provides more accurate diagnostics.

The library itself has been expanded with Release 7, which adds device models for the 68000, Z8000, and 8086 microprocessors, support chips for the 8086, and new ECL-family components.

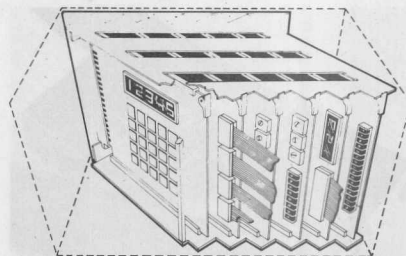
Systems with usable configurations are priced at \$151,000 for the 2271 and at \$180,000 for the 2272. Delivery for both units begins in the fourth quarter of 1981.

GenRad, 170 Tracer Lane, Waltham, MA 02254. Raymond McNulty (617) 890-4900.

Jonah McLeod, Instruments Editor

CIRCLE 310

board edges accessible



A space-saving open-frame cage for STD-bus cards, the Slant Rack, holds boards at an angle to permit easy access to their edges. The cage exposes terminal blocks, pots, and other components at the edge of boards to permit fast connections and adjustments. The end board position leaves a card completely exposed—a good spot for a control panel. The 10-in.-wide cage spaces cards 3/4-in. apart and fits in a 7-in.-deep enclosure with room to spare.

Circuits and Systems, Inc., 2 Main St., Hollis, NH 03049. (603) 465-7063. \$295.

CIRCLE 336

Automated system tests and sorts wafers

An automated system for characterizing and sorting substrates, the WaferCheck 7000, performs capacitance testing of wafer flatness and thickness with an accuracy to within 0.5 μm , tests resistivity over a range of 0.001 to 199.9 Ω/cm , sorts n-type and p-type substrates, and provides a null decision category for indeterminant dopant types. Along with flatness, thickness, resistivity, and type, the WaferCheck includes a visual inspection subsystem for categorizing such surface defects as fingerprints, pitting, scratches, particulates, and stains.

ADE Corp., 77 Rowe St., Newton, MA 02166. (617) 969-0600.

CIRCLE 337

The industry's most complete computer systems package—

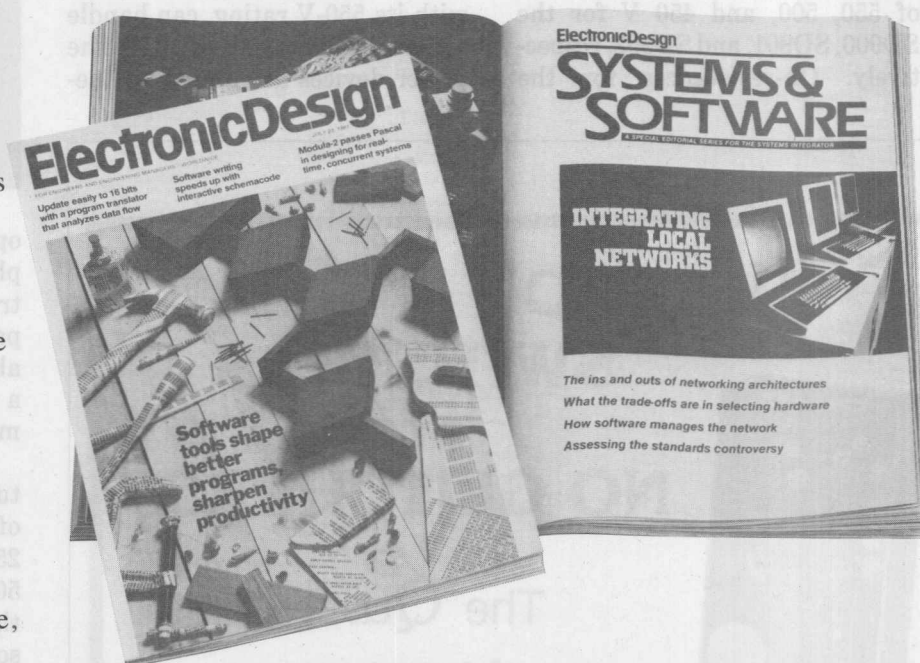
With more and more products reaching VLSI levels, design engineers and managers have an increasing need to understand the end-use implications of systems designs. At the same time systems integrators are discovering they must know more about chip and board-level design trends. New technologies at these levels are greatly impacting the performance and capabilities of integrated systems.

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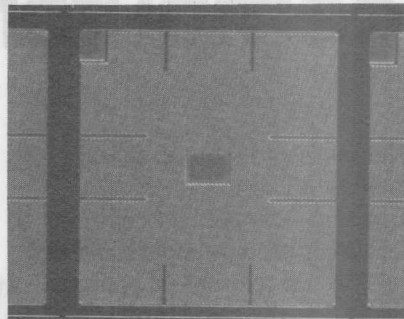
First place to address engineering management

DMOS power FETs handle 450 to 550 V at up to 7A

Offering continuous current ratings of 5, 6, and 7 A, the SD900 series of DMOS power FETs will also feature drain-source voltages of 550, 500, and 450 V for the SD900, SD901, and SD902, respectively. On-resistances for the

n-channel devices are 2, 1.5, and 1 Ω , respectively.

Designed to meet European voltage requirements, the SD900, with its 550-V rating, can handle a peak drain current of 12 A. The power devices are aimed at line-



operated switching power supplies, amplifiers, and motor controls. Housed in TO-3 metal packages, the units can handle about 80 W (continuous) and have a linear derating factor of 640 mW/°C.

All three power devices have a turn-on time of 40 ns and a turn-off time of 160 ns with a V_{DS} of 25 V, an I_D of 2 A, and an R_G of 50 Ω . At a frequency of 1 MHz, the transistors have a common-source input capacitance of 1500 pF, a reverse transfer capacitance of 40 pF, and an output capacitance of 200 pF. Also, all units have a common-source forward transconductance of 1.8 S (at $f = 1$ kHz, $V_{DS} = 25$ V, and $I_D = 2$ A).

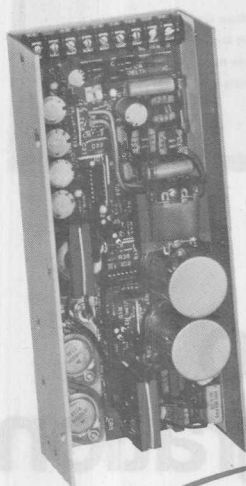
Other versions of the SD900 family planned for the future include a 20-A unit with a 100-V rating. The device will have an on-resistance of just 0.15 Ω . Another, longer-term project is to develop a higher-power TO-220 plastic package. The problem with currently available TO-220 packages is that the lead frames are too small for the chip, which is about 200 mils on a side.

Prices for the devices in 100-unit lots are \$16.15, \$15.00, and \$13.40, for the 900, 901, and 902, respectively. Delivery is from distributors' stock.

Semi Proceses Inc., 1885 Norman Ave., Santa Clara, CA 95050. Tom Cauge (408) 988-4004.

CIRCLE 303

DELTRON SWITCHERS are NO GLITCHERS



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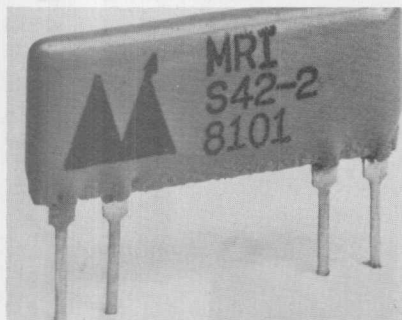
Deltron inc.

Wissahickon Avenue • North Wales, PA 19454
Tel: 215/699-9261 Twx: 510/661-8061

AC 34

CIRCLE 92

Miniature SSR handles 0.75 A and 250 V rms



The S42-series solid-state ac relays rated at 0.75 A and 250 V rms come in an SIP that measures $0.75 \times 0.325 \times 0.125$ in. The relays provide 2500 V rms of input/output isolation and carry a 600-V peak transient rating as an option. Incorporating parallel photo SCRs as output switching devices, the relays feature zero-voltage turn-on, with a maximum ± 5 -V zero switch window. Model S42 takes a 3.5 to 8-V dc input, with a maximum of 8 mA required to operate the relay at a 5-V input. Model S42-3 operates with 8 to 17-V dc inputs and requires a maximum of 8 mA at 10 V.

Microelectronic Relays International, Inc., 2566 Via Tejon, Palos Verdes, CA 90274. (213) 373-0721. \$7.50 (1000 qty); stock to 6 wks.

CIRCLE 338

2-A latching relays measure 10.4 mm high

Polarized latching relays in the BZB series handle 50 W at 2 A and switch a maximum of 60 V dc, but measure 10.4 mm high and weigh 18.2 g. The relays come in 4PDT and DPDT versions equipped with gold-overlay, silver-palladium stationary contacts and silver-palladium movable contacts.

ITT Components, 3201 S. Standard St., Santa Ana, CA 92707. (714) 964-8391. \$7.75 (4PDT) (1000 qty); 8 to 10 wks.

CIRCLE 339

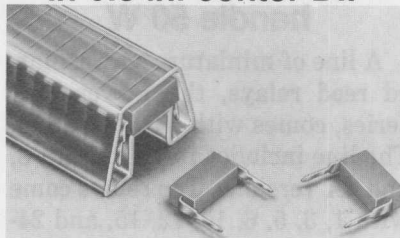
LEDs and detectors serve remote controls

A series of GaAs IR LEDs in T 1- $\frac{3}{4}$ dark plastic packages operate in remote control applications with a series of PIN photodetectors that come in a plastic package similar to the TO-92. The emitter series, designated LD-271, includes three versions with 7, 10, and 16-mW/sr radiant-intensity ratings at 100 mA, with a half-angle of 25° . The photodiodes, designated SFH-205 (sensitive on rounded side) and SFH (sensitive on flat side) come in black encapsulated packages. Another version, the SFH-206K, has a colorless plastic package. Spectral sensitivity for the SFH-205 and SFH-206 is greater than $30 \mu\text{A} \cdot \text{cm}^2/\text{mW}$ at 5 Vr. Spectral sensitivity for the SFH-206K is greater than 5 nA/lx.

Litronix, Inc., 19000 Homestead Rd., Cupertino, CA 95014. (408) 256-7910.

CIRCLE 340

Ceramic caps come in 0.3-in.-center DIP



Mono-Pak ceramic capacitors come with two in-line pins set on a 0.3-in. spacing for mounting compatibility with ICs and other DIP components. The capacitors stand 0.165 in. high above a board when installed. Capacitance values range from 10 pF to .39 μF . The units are magazine packed for automatic insertion.

Centralab, Inc., 5855 N. Glen Park Rd., Milwaukee, WI 53201. (414) 228-7380. \$0.09 (50,000 qty).

CIRCLE 341

Circuit breakers conform to VDE 0730 spacing

A line of magnetic circuit breakers that conform to the spacing requirements of VDE 0730, Snapaks, includes double-pole push-pull and push-to-reset, and single or double-pole rocker versions. An auxiliary switch is available as an integral part of a series pole in single or multipole assemblies. Isolated electrically from the protector's circuit, this switch works in unison with the power contacts and provides indication, at a remote location, of the protector's on-off status. The compact units come with choices of handle actuation, colors, illumination, terminals, and hardware.

Airpax/North American Philips Controls Corp., Cambridge Div., Woods Rd., Cambridge, MD 21613. (301) 228-4600.

CIRCLE 342

Snap-in LED indicators come in bicolor versions

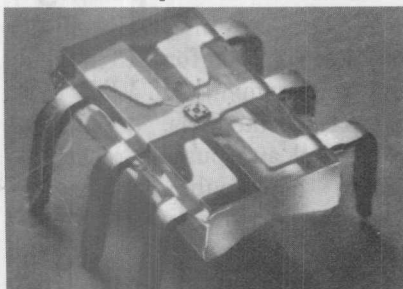


A line of snap-in LED panel indicators, the 558 and the 559 series, includes red, green, and yellow versions, in addition to a model that combines a red and a green-emitting chip in a single package. The 558 indicators fit in 0.156-in. holes on 0.2-in. centers and the 559 series fits in 0.25-in. holes on 0.3-in. centers. Black housings increase color contrast.

Dialight, 203 Harrison Pl., Brooklyn, NY 11237. (212) 497-7600.

CIRCLE 343

Four-sector photodiode develops 0.11 nA/lx

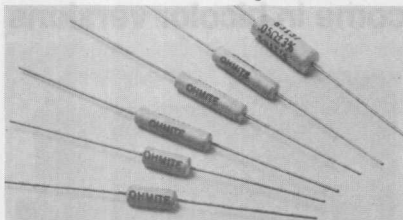


The SFH-204 photodetector has four separate active sections whose contacts are spaced 12 μm apart for precise positioning in such applications as edge control, path scanning, and angle scanning. The device operates with a sensitivity of 0.11 nA/lx. The detector comes encased in a transparent package with 6 leads.

Litronix, Inc., 19000 Homestead Rd., Cupertino, CA 95014. (408) 257-7910. \$7.85 (100 qty); Stock.

CIRCLE 344

Sub-ohm wire-wound resistors keep L low



A series of wire-wound vitreous enamel resistors with values from 0.005 to 1 Ω , the Lo-Mite 99L series, typically shows an inductance value of 0.1 μH . The resistors come in 3, 5, and 10 W sizes, with a standard tolerance of 5%. Tempcos range from ± 300 ppm/ $^{\circ}\text{C}$ for 0.01- Ω resistors to ± 60 ppm/ $^{\circ}\text{C}$ for 1- Ω resistors. The 3-W versions measure 0.562×0.234 in. The axial-lead resistors are compatible with automatic insertion equipment.

Ohmite Manufacturing Co., 3601 Howard St., Skokie, IL 60076. (312) 675-2600.

CIRCLE 345

LEDs with oscillator chip blink

Two red LED indicators, designated the CQX21 and the CQX22, contain two chips in their standard T-1 $\frac{3}{4}$ diffused packages: a conventional GaAsP LED and an oscillator chip connected in series. Thus, the LEDs' on/off state can be controlled by the internal oscillator chip, which switches the LED via an internal MOS switch at a predetermined rate (typically 3 Hz). The CQX22 has two supply leads and a control lead to permit selection of the blink mode, continuous on, or off. The 5-V devices provide a typical luminous intensity of 1.6 mcd at a peak wavelength of 660 nm. The indicators operate with a half-intensity angle of 80°. On-state consumption measures 35 mA with a 5-V supply.

AEG-Telefunken Semiconductors, Rt. 22—Orr Dr., Somerville, NJ 08876. (201) 722-9800. \$0.58 (CQX21), \$0.63 (CQX22) (1000 qty).

CIRCLE 346

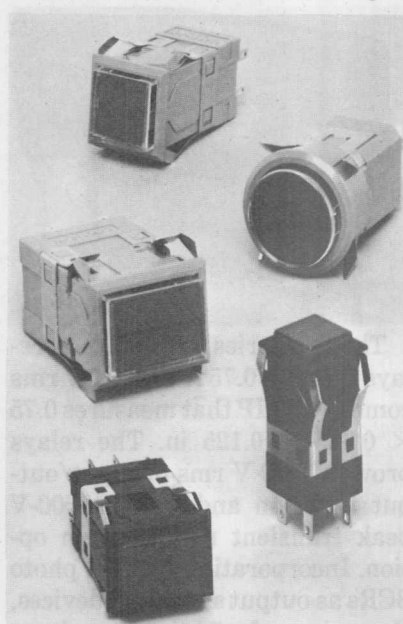
Miniature reed relays handle 50 W

A line of miniature encapsulated reed relays, the Power Max series, comes with a 50-W rating. The line includes form 1A, 2A, 3, and 4A versions. The relays come with 1, 3, 5, 6, 10, 12, 15, and 24-V coils and have 0.1-in. terminal spacing. The injection-molded components meet UL 94V-0 and withstand cleaning solvents, acids, fluxes, and salt spray. Options include magnetic shielding and special construction for operation in high-temperature environments.

Electronic Applications Co., 4918 Santa Anita Ave., El Monte, CA 91734. (213) 442-3212. Under \$0.95 (OEM qty); stock to 4 wks.

CIRCLE 347

Illuminated pushbutton switches offer variety



A line of momentary and alternate-action illuminated pushbutton switches, the A3 series, offers a broad selection of models with either LEDs or incandescent lamps, and silver or gold contacts. The units come with switch guards and protective covers for harsh environments. Versions come with solder terminals or terminals for PC board mounting.

Omron Electronics, Inc., Control Components Div., 650 Woodfield, Schaumburg, IL 60195. (312) 843-7900.

CIRCLE 348

20-k trimmer drops tempco to 5 ppm/ $^{\circ}\text{C}$

A $\frac{3}{4}$ -in. trimming potentiometer with a range of 10 to 20 k, the Model 1285, works from -55 to $+125^{\circ}\text{C}$ with a tempco of ± 5 ppm/ $^{\circ}\text{C}$. The trimmer has a $\pm 5\%$ tolerance. At 100 MHz, rise-time measures 10 ns.

Vishay Resistive Systems Group, 63 Lincon Hwy., Malvern, PA 19355. (215) 644-1300.

CIRCLE 349

OEM AMERICA MEETS AT THE INVITATIONAL COMPUTER CONFERENCES



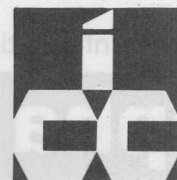
Every type of computer and peripheral — mini/micros, disk drives, tape drives, printers, interfaces, CRTs — will be on display at the Invitational Computer Conferences, the only one-day regional seminar/displays directed exclusively to the needs of the quantity buyer. During the 1980/1981 series, over 7,000 OEMs attended the conferences to receive a concentrated, close-up view of the newest computer and peripheral equipment presented by forty of the world's top manufacturers, as well as to attend a program of technical seminars covering the latest state-of-the-art technology.

Last year some of the biggest names in the computer industry exhibited their products at the

Invitational Computer Conferences. Shouldn't you be there this year with:

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Date	Location
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Oct. 27, 1981	Valley Forge, PA
Oct. 29, 1981	Washington, D.C.
Nov. 17, 1981	Palo Alto, CA
Jan. 14, 1982	Orange County, CA
Feb. 10, 1982	Ft. Lauderdale, FLA
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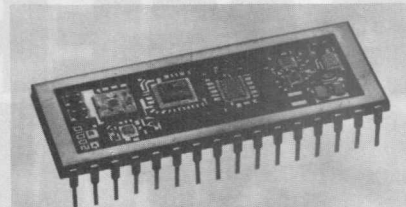
alpha data

20750 MARILLA STREET, CHATSWORTH, CALIFORNIA 91311
(213) 882-6500

CIRCLE 94

ANALOG CIRCUITS

10-bit ADC converts within 1.8 μ s at 550 kHz

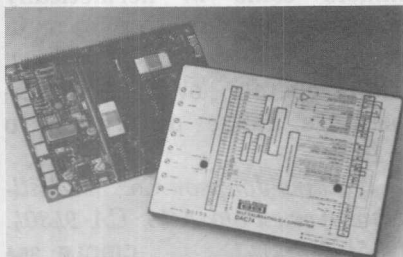


One version of the AD579 10-bit a-d converter performs a full-accuracy conversion within 1.8 μ s at maximum. Applications for the converter include data acquisition systems with throughput requirements of up to 550 kHz. The device may be short-cycled to provide faster conversions at lower resolutions. Key specifications include a maximum linearity error of $\pm\frac{1}{2}$ LSB, a gain temperature coefficient of ± 30 ppm/ $^{\circ}$ C maximum, and a power requirement of 775 mW. A number of features make the AD579 easy to use, including a choice of parallel or serial output, short cycle capability, an adjustable internal clock, and input ranges of ± 5 V, ± 10 V, 0 to +10 V, and 0 to +20 V. The internal reference can also be applied externally to supply up to ± 1 mA. Four grades of the AD579 are available. JN and KN grades are specified over the 0 to +70 $^{\circ}$ C temperature range and are packaged in a 32-pin side-brazed ceramic DIP with a polymer seal. BD grades are specified over the -25 $^{\circ}$ C to +85 $^{\circ}$ C range and TD grades are specified over the -55 $^{\circ}$ C to +125 $^{\circ}$ C range; BD and TD versions are packaged in the 32-pin side-brazed ceramic DIP with a hermetic seal. Power requirements are ± 15 V at +8 mA and -35 mA maximum and +5 V at 110 mA maximum. Optional "Z" models are available for operation from ± 12 -V supplies.

Analog Devices Semiconductor, 804 Woburn St., Wilmington, MA 01887. (617) 935-5565. \$178.75 (AD579TD) (100 qty).

CIRCLE 354

16-bit DAC incorporates μ P for self-calibration

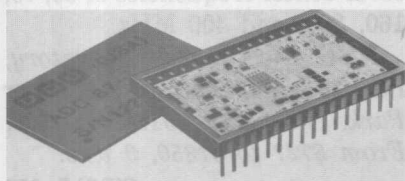


A true 16-bit a-d converter module, the DAC74, incorporates a microprocessor-based calibration circuit that prohibits non-linearity and gain error from exceeding $\pm 0.00075\%$, and keeps offset from exceeding $\pm 80 \mu\text{V}$, over a 30° temperature range from 15 to 45°C for one year. The calibration circuit reduces total error to ± 1 LSB over the same temperature range. A single TTL signal initiates the 2.5-s calibration cycle. The converter provides a unipolar or bipolar output.

Burr-Brown, P.O. Box 11400, Tucson, AZ 85734. (602) 746-1111. \$14.95; stock to 4 wks.

CIRCLE 355

12-bit ADCs serve as alternatives to ADC85/87



Two 12-bit, $10\text{-}\mu\text{s}$, a-d converters, the DDC ADC85 and the DDC ADC87, serve as pin-for-pin replacements of the industry-standard ADC85 and ADC87. The converters operate from ± 15 or $\pm 12\text{-V}$ supplies at 1.2 W power dissipation. The 12-bit a-d converters come in hermetic 32-pin DIPs.

ILC Data Device Corp., 105 Wilbur Pl., Bohemia, NY 11716. (516) 567-5600. From \$14.3; stock to 4 wks.

CIRCLE 356

Clock and resistors set chip filter's parameters

An external clock and three to four resistors are the only external components necessary to set the center frequency, gain, and Q of the MF10 monolithic filter. The filter sets the center frequencies of various second-order functions (up to 20 kHz) directly proportional to an external clock frequency, or directly proportional to both the clock frequency and external resistor ratios. As a result of the elimination of capacitors, the complexity of tuning the center frequency is substantially reduced. The stability of the filter frequency depends on the quality of the clock. A single clock drives an infinite number of the filters. The device performs a wide variety of functions, including allpass, highpass, bandpass, and notch. Up to fourth-order functions—and any of the classical filter configurations, such as Butterworth, Bessel, Cauer, and Chebyshev—can be easily arranged by cascading devices.

National Semiconductor, 2900 Semiconductor Dr., Santa Clara, CA 95051. (408) 737-5000. \$3.70 (100 qty).

CIRCLE 357

Signal processing chip calculates FFTs

A signal processing chip, the S2814A, uses a decimation-in-frequency technique to calculate 32-point fast Fourier transforms and inverse fast Fourier transforms in as little as 1.3 ms . Optional versions process larger transforms, extend dynamic range from 57 to 70 dB , and compute the power spectrum of the transformed signal.

American Microsystems, Inc., 3800 Homestead Rd., Santa Clara, CA 95051. (408) 246-0330. \$250 (100 qty).

CIRCLE 358

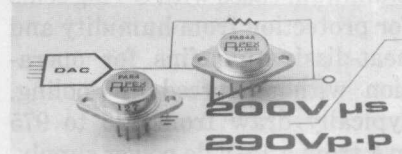
Op amp reduces input offset to $10 \mu\text{V}$

A series of operational amplifiers, the OP-07 line, reduces input offset to $10 \mu\text{V}$. Low-frequency noise up to 10 Hz measures $0.35 \mu\text{V}$ pk-pk. In addition, internal biasing reduces external bias and offset currents to $\pm 1\text{ nA}$ over the range of -55 to $+125^\circ$ (military versions). The series includes 5 grades for industrial and military environments.

Raytheon Semiconductor, 350 Ellis St., Mountain View, CA 94040. (415) 968-9211. From \$4.50 to 49.50 (100 qty).

CIRCLE 360

High-voltage op amps slew $200\text{ V}/\mu\text{s}$

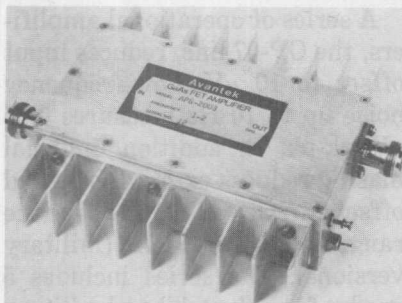


The PA84 and the PA84A hybrid op amps deliver outputs up to 290 V at load currents of $\pm 40\text{ mA}$ with a $200\text{-V}/\mu\text{s}$ slew rate. Internal over-temperature protection safeguards outputs. Internal current limiting enables the amplifiers to withstand a short circuit without causing secondary breakdown. Output transistors are biased for a continuous on condition to enhance linearity. The input circuit is also protected against differential input voltages as great as the power-supply potential. The PA84 reduces input-offset voltage drift to $10 \mu\text{V}/^\circ\text{C}$; the PA84 tightens the specification to $5 \mu\text{V}/^\circ\text{C}$. Both op amps accept power supply voltages from $\pm 150\text{ V}$ (or 300 V , total) to $\pm 15\text{ V}$ (30 V , total).

Apex Microtechnology Corp., 1130 E. Pennsylvania St., Tucson, AZ 85714. (602) 746-0849. \$66.50 (PA84), \$77.50 (PA84A) (100 qty).

CIRCLE 359

Amplifier for 1 to 2 GHz gives 30-dBm output



GaAs FET amplifiers in the APG-2000 series provide 10, 20, or 30-dB gain, as flat as ± 0.5 dB, over the range of 1 to 2 GHz for a minimum output power of 30 dBm at 1 dB gain compression. The amplifiers reduce operating noise to a maximum of 5 dB. The amplifiers, which come in aluminum cases with O-ring seals for protection from humidity and heat-dissipating fins for operation without forced-air cooling, typically draw from 875 to 975 mA from a 15-V dc power supply. An integral dc-dc converter provides each GaAs FET with both positive and negative bias voltages, permitting the device source terminals to be electrically grounded and reliably heat-sunk.

Avantek, Inc., 3175 Bowers Ave., Santa Clara, CA 95051. (408) 727-0700. From \$1000 to \$2000; 13 wks. **CIRCLE 361**

Two-wire pair transfers 24-bit input at 7 kbits/s

A two-wire transmitter and receiver pair, the STAR, converts a 24-channel parallel input from contact closures or TTL signals to serial format for transfer at a rate of 7 kbits/s. Expansion modules, available in 24-bit increments, increase the data word-length to 96 bits for two-wire transmission. Latched outputs are available as standard logic drivers or high-power open collectors rated at 50

V at 0.3 A to drive relays. The transmitter and receiver operate from 5-V supplies. Terminal blocks on both the transmitter and receiver modules accept 18 to 22-AWG wires.

Analite, Inc., 24 Newtown Plaza, Plainview, NY 11803. (516) 752-1818.

CIRCLE 362

GaAs FET amplifier gives 14-dB gain at 12 GHz

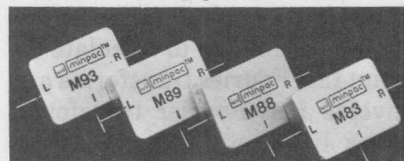


A hybrid GaAs FET amplifier, the A55I-82, covers from 7 to 12 GHz with a minimum gain of 14 dB, a 6-dB noise figure, and a typical 13-dBm output at 1 dB compression. The amplifier incorporates a regulator chip in-circuit. The package is compatible with stripline applications.

Aerotech Industries, 825 Stewart Dr., Sunnyvale, CA 94086. (408) 732-0880.

CIRCLE 363

Microwave mixers work in EW applications



Four broadband double-balanced mixers, the M83, M88, M89, and M93, cover 2 to 18 GHz over rf and LO ranges while affording the user an IF choice of either 0.03 to 4 GHz or 1 to 8 GHz. The mixers work in up-conversion and down-conversion applications and, along with their dc-coupled IF

ports, operate as phase detectors or biphase modulators. All four mixers come in hermetically sealed microstrip packages or in drop-in SMA-connector housings. They operate over the temperature range of -54°C to $+100^{\circ}\text{C}$.

Watkins-Johnson Co., 333 Hillview Ave., Palo Alto, CA 94304. (415) 493-4141. **CIRCLE 364**

Delay-line i-f limiter discriminators aid EW

A series of delay-line i-f limiter discriminators, the ICDX family, serves radar and EW applications that require measurement of the frequency of a pulsed carrier and applications in which FM information is carried within pulses. Leading and trailing-edge transients in limiter discriminators result from AM to PM conversion in limiter stages and small time-delay variations through the opposing detectors used to generate an "S" curve. The series reduces these transients by using a simulated delay line for demodulation and a constant-phase limiter/driver. Six models cover center frequencies of 60, 70, 160, 300, and 400 MHz.

RHG Electronics Laboratory, Inc., 161 E. Industry Court, Deer Park, NY 11729. (516) 242-1100. From \$727 to \$1350, 9 wks.

CIRCLE 365

PIN-switch driver takes TTL direction

A TTL-compatible driver for PIN microwave switches, the 207F, operates within 10 ns up to 20 MHz. The driver uses a 12-V supply and comes packaged in a 0.375×0.375 -in. flatpack.

New England Microwave Corp., 26 Hampshire Dr., Hudson, NH 03051. (603) 883-2900.

CIRCLE 366

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MATERIALS

Semiconductor insulator needs no grease

A thermally conductive, electrically isolating interface material for mounting semiconductor devices, Cho-Therm 1685, requires no grease, unlike mica or beryllium insulators. The material provides a thermal impedance of 0.25°C/W and has a breakdown-voltage rating in excess of 2500 V. The insulators are available cut to standard or non-standard power-semiconductor case configurations, with or without an adhesive coating on one side.

Chomerics, Laminates, Inc., 77 Dragon Ct., Woburn, MA 01888. (617) 935-4850.

CIRCLE 367

As dopant produces source-drain diffusions



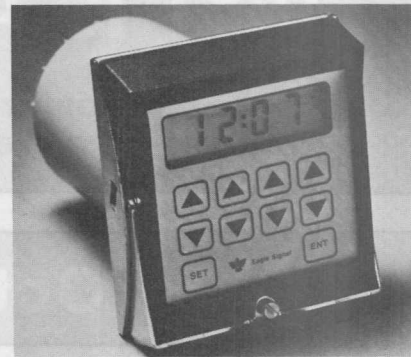
An arsenic-based spin-on dopant, Accuspin AS-310, works in the production of shallow-junction source-drain diffusions for MOS circuits or deep-diffused buried-collector layers. The dopant can be used from 1000 to 1050°C to provide sheet resistance values of 25 to 35 Ω /square at junction depths of 0.3 to 0.5 μ m. The liquid comes in 125-ml, 500-ml, and one liter plastic bottles.

Allied Chemical, Electronic Chemicals Group, P.O. Box 1139, Morris Township, NJ 07960. (201) 455-2000.

CIRCLE 368

SUBASSEMBLIES

μ P-based counter/timer withstands industrial use



A 4½-digit microprocessor-based timer/counter with a sealed front panel to protect against contaminants, the CX300, offers four time ranges from 0.01 s to 199 h, 59 min. The unit performs 19,999 counts at count speeds of 500/min. ac or dc, 5000/min. ac or dc, and 5000/s dc. The counter/timer incorporates an LCD and a battery-protected memory. The unit has two form-C instantaneous contacts rated at 10 A and two form-C delayed contacts rated at 10 A. Optional 5-A gold-diffused, silver contacts are addressable.

Eagle Signal Industrial Controls, 736 Federal St., Davenport, IA 52803. (319) 326-8120. \$175.

CIRCLE 369

Flat accelerometer gives 5 mV/g at 20 kHz

An accelerometer with an integral preamplifier, the Model 9001, measures vibration on small, light masses over a frequency range of 3 to 20,000 Hz with a sensitivity of 5 mV/g. The accelerometer, which stands 0.25-in. tall and weighs 0.75 grams, operates at accelerations up to 500 g without clipping and requires no charge amplifier. The unit withstands a 10,000-g shock.

Vibra-Metrics, Inc., 385 Putnam Ave., Hamden, CT 06517. (203) 288-6158.

CIRCLE 370

New Literature



Ceramic substrates

A six-page bulletin includes diagrams and tables that describe the electrical and physical properties of multilayer ceramic substrates. 3M.

CIRCLE 371

PC connectors

An eight-page bulletin describes a line of high-density, two-piece board connectors with up to 96 contacts in three rows. Panduit.

CIRCLE 372

Relays

A 125-page catalog describes a line of sealed relays for PC board installation, a series of mercury-wetted relays, and programmable time delay relays. Extensive application data assist selection. Midtex.

CIRCLE 373

Plugs and jacks

A four-page catalog details a line of battery snaps, plugs, and jacks. Drawings are included. Connector Corp.

CIRCLE 374

Connectors

A catalog describes a full line of high-reliability electronic interconnection and packaging components ranging from sockets and headers to mounting racks, backplanes and boards. Garry.

CIRCLE 375

Printers

A catalog describes two 20-column alphanumeric thermal printers, one with an RS-232 interface. Also included is information on a digital tape recorder and a bubble-memory storage module. Memodyne.

CIRCLE 376

Power conditioners

A 20-page catalog discusses sources of surges, transients, and noise, and features line monitor power conditioners to counter them. SGL Waber Electric.

CIRCLE 377

Impact printers

A six-page brochure describes a line of dot-matrix impact print mechanisms, including information on print speeds, characters per line, print area, printheads, sweep, and operating temperatures. Eaton.

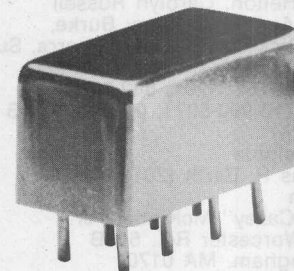
CIRCLE 378

Glass photomasks

A 12-page booklet describes image-plane plate-glass photomasks for imaging applications. The booklet outlines the advantages of image-plane photomasks over conventional emulsion-coated glass plates or film in the production of PC boards, flexible circuits, and other products that require fine line geometries. PPG Industries.

CIRCLE 379

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CONTROL	DC-0.05		
INSERTION LOSS, dB		TYP.	MAX.
one octave from band edge		1.4	2.0
total range		1.6	2.5
ISOLATION, dB		TYP.	MIN.
1-10 MHz IN-OUT		65	50
IN-CON		35	25
10-100 MHz IN-OUT		45	35
IN-CON		25	15
100-200 MHz IN-OUT		35	25
IN-CON		20	10
IMPEDANCE		50 ohms	

For complete specifications and performance curves refer to the 1980-1981 Microwaves Product Data Directory, the Goldbook or EEM.

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CIRCLE 95

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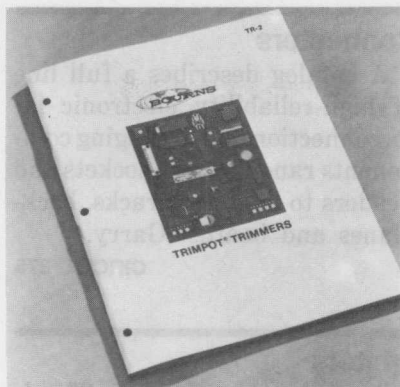
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NewLiterature



Trimmers

A 76-page catalog describes a line of wirewound and cermet trimmers and resistors. Ranges, sizes, shapes, and methods of mounting are included, and there are sections on military specifications, outline templates, and characteristics. Bourns.

CIRCLE 380

DIP sockets

A 44-page catalog contains specifications and ordering information on DIP and transistor sockets, cable sockets, plugs, jumpers, and strip connector products. Samtec.

CIRCLE 381

Software packages

A four-page brochure describes a library of image processing software, including disk paging, tape I/O, pixel move and convert routines, enhancement and expansion analysis, and interpretation capacities. DeAnza Systems.

CIRCLE 382

Millimeter-wave systems

Over 100 pages describe components and systems for millimeter-wave transmission and reception, including instrumentation. The edition highlights a computer-controlled millimeter-wave network analyzer. Hughes Aircraft.

CIRCLE 383

Small-signal transistors

A four-page data sheet reviews the LT4700 small-signal, low-noise microwave transistors. Charts include typical noise figures and associated power gain vs frequency, noise measure vs frequency, and output power vs collector current. TRW.

CIRCLE 384

Pressure transducers

A catalog details a line of pressure transducers that come with or without integral amplifiers for aircraft use. Photos, drawings and specifications are included. Kulite Semiconductors.

CIRCLE 385

Thumbwheel switches

A six-page product guide contains photographs and diagrams of ten commercial and industrial thumbwheel digital switches. Digitran.

CIRCLE 386

Delay lines

A 20-page catalog reviews a line of BAW delay lines for radar signal processing. The booklet reviews delay-line principles. Thomson-CSF Components.

CIRCLE 387

Headers and sockets

A four-page brochure outlines a line of headers and sockets, with from 10 to 60 contacts, that meet MIL-C-83503 dimension specifications. Robinson-Nugent.

CIRCLE 388

X-Y recorders

A six-page bulletin describes the performance of a series of laboratory X-Y recorders. Gould.

CIRCLE 389

GM may drop its technical college

In a move to cut corporate overhead costs, General Motors Corp. is considering doing away with its wholly owned General Motors Institute (Flint, MI), which for 62 years has trained technicians, engineers, and managers for the automotive giant.

By all accounts, GMI has been a success. Of the total graduates of the five-year accredited college, 96% have gone to work for the company, and often—because GMI's recruitment has been highly selective—these engineers and managers have been the cream of the crop. In some cases, much of the company has ended up working for them: GM's president, F. James McDonald, and nine vice presidents have passed through the Institute's gates. But according to officials, GM is now seeking less costly and more effective ways of recruiting and training engineers and other technical professionals.

Engineers rank low in management potential

Two studies by AT&T, one started in 1956 and one started in 1977, come to the same conclusion: Engineers are least likely to have the characteristics that AT&T considers necessary for promotion into management.

The studies tracked the career progress of hundreds of AT&T employees with degrees in humanities, business, and engineering. Nearly 50% of the humanities/social science majors were considered to have potential for middle management, compared with 31% of the business majors. Only 26% of the engineers were rated favorably.

According to Robert E. Beck,

AT&T's assistant vice-president of human resources, in a paper describing the studies, "both the humanities/social science majors and the engineers have shown a consistent pattern of strengths and weaknesses that held over a 20-year period in the two longitudinal studies."

Beck adds that AT&T's first management-assessment center was able to identify with remarkable accuracy which study participants would eventually receive promotions. Assessment centers are now used company-wide to determine potential for advancement. Over 250,000 people have been assessed to date, and the method has spread to hundreds of other companies.

Immigration reform would ease alien hirings

As part of an ambitious package of immigration law reforms, the Reagan administration has proposed a "guest worker" provision that significantly streamlines the rules under which foreign nationals can be hired to fill technical jobs in the United States.

The plan would eliminate the current requirement that an employer must show case by case that a job offered to an alien cannot be filled by a U.S. citizen. Instead, the Department of Labor will publish an annual list of employment categories for which not enough U.S. citizens can be found and open those jobs to aliens, to be filled with a minimum of paperwork. The present alien employment process often takes a year or more and imposes thousands of dollars in bureaucratic costs. Since the U.S.'s engineering shortage is well publicized, many engineers fear that the Reagan plan would

open such employment to aliens.

However, those close to congressional immigration policy leaders indicate that the President's proposals will probably meet with resistance and amendments before they become law. They say that the guest worker provision in particular is strongly opposed by Sen. Alan Simpson (R-WY), chairman of the Senate Immigration and Refugee Policy Committee.

"We have a situation where an entire economy and social education policy could be overrun by the sheer numbers of nonresident people flooding into this country," says Mary Kay Wilson, press assistant to the senator. "We should tend to ourselves. If there are job openings, they should be filled—in whatever way—by American citizens."

Feerst launches write-in campaign

Irwin Feerst, IEEE's perennial reformer and gadfly, is taking a last-minute shot at the office of Region 1 IEEE Director. His latest newsletter urges that all eligible IEEE members write in his name for this job on the 1981 annual election ballot, which has already been sent out to the Institute membership. All ballots must be signed and returned to the Independent Election Corp. of America (Westbury, NY) by November 2, 1981.

There are no petition candidates for national offices this year, and all the Board of Directors nominees are running unopposed. In Region 1, three candidates nominated by the region are also seeking the Director position: Alex Gruenwald, Joel B. Snyder, and Bruce D. Wedlock.

Don Mennie, Jeffrey Rothfeder

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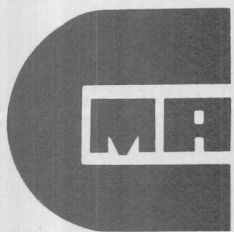
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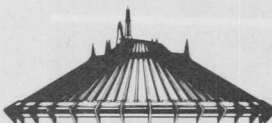
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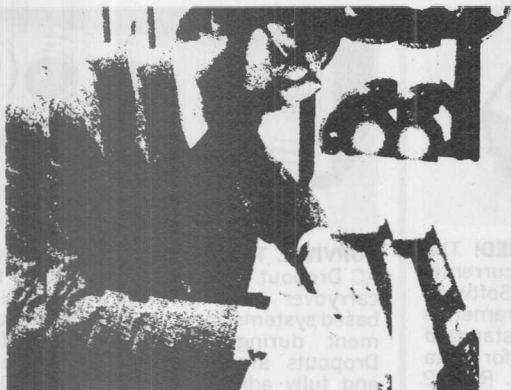
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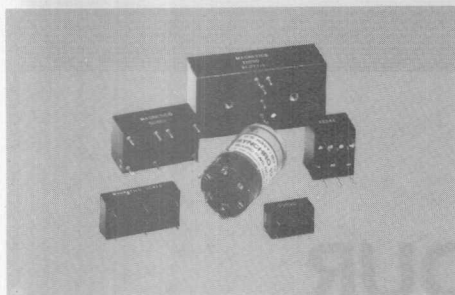
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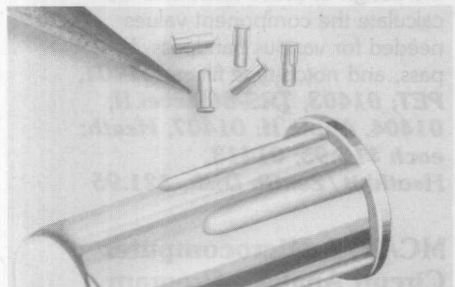
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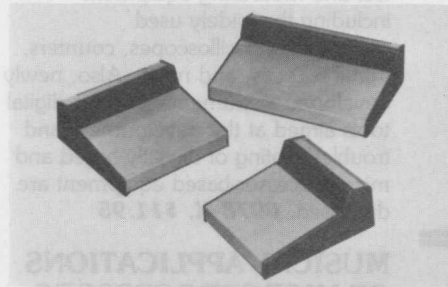
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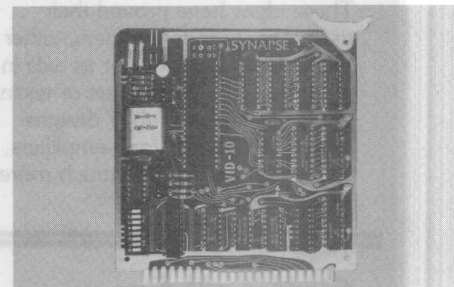
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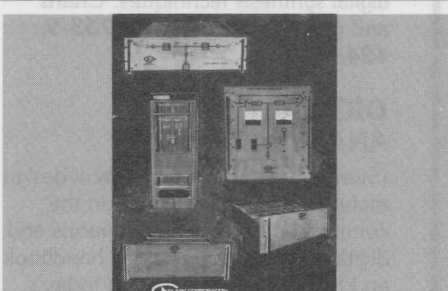
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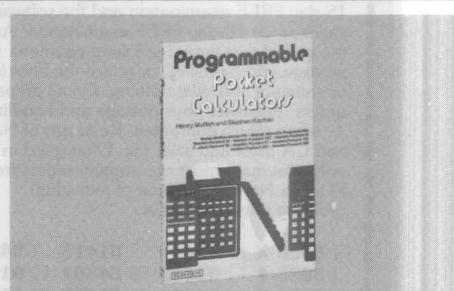
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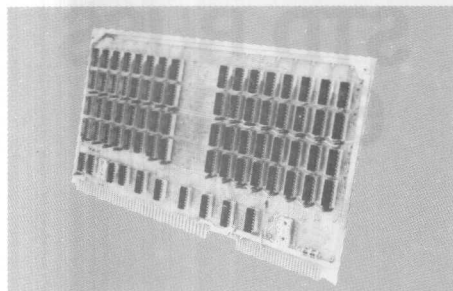
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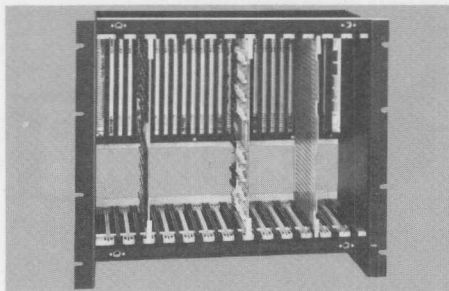
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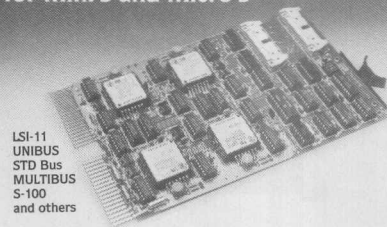
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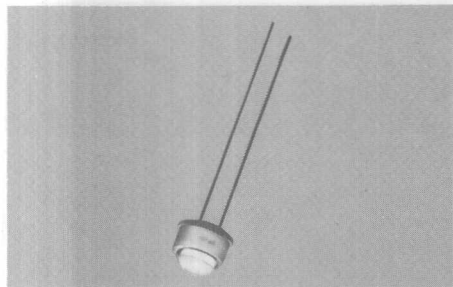
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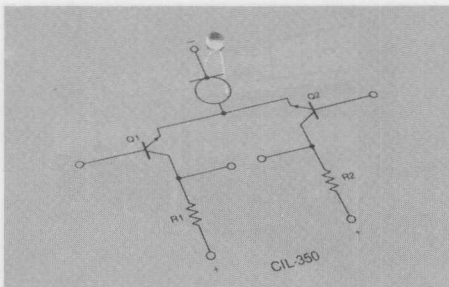
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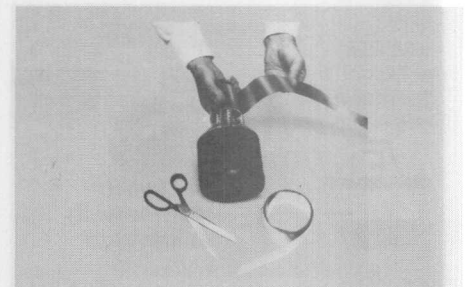
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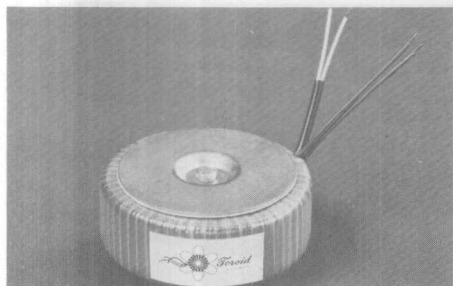
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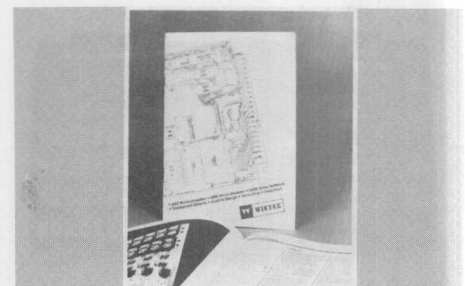
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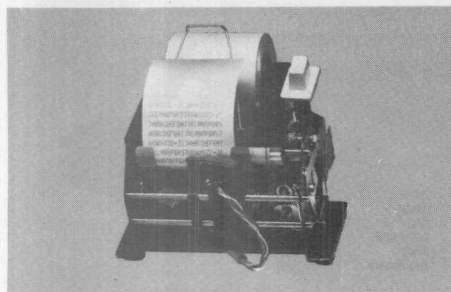
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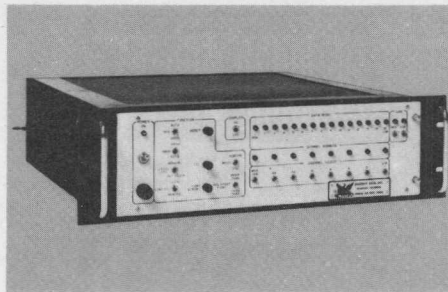
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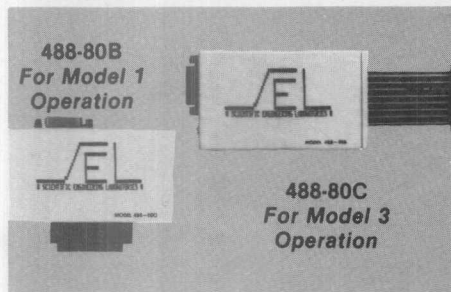
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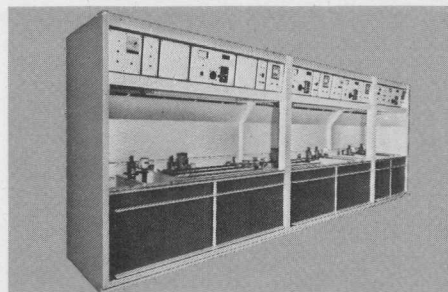
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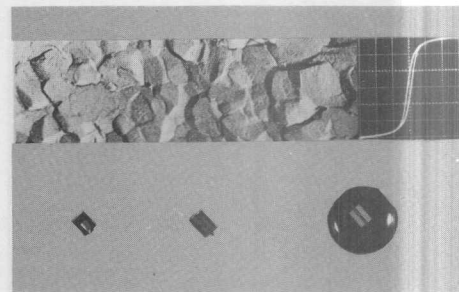
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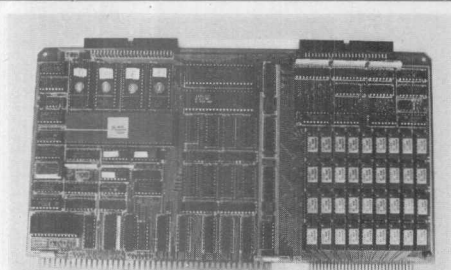
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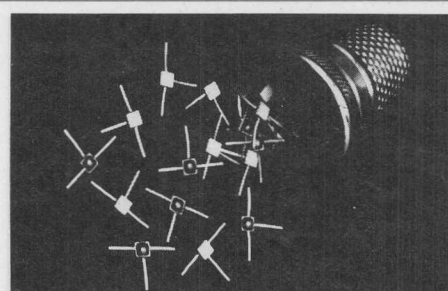
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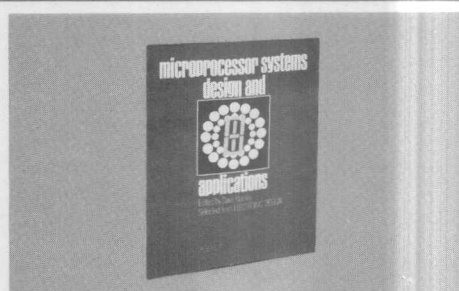
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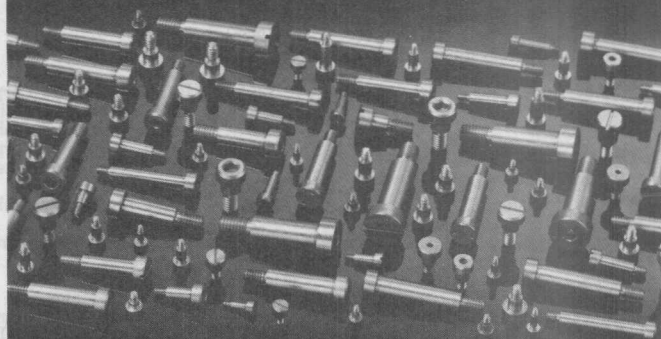
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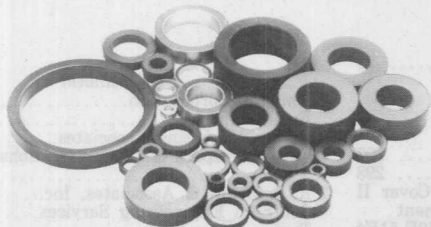
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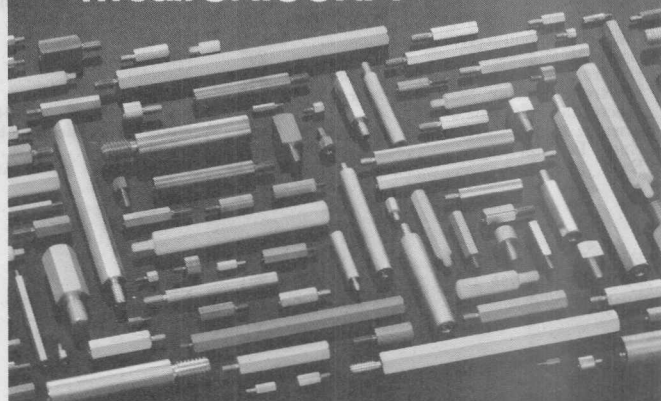
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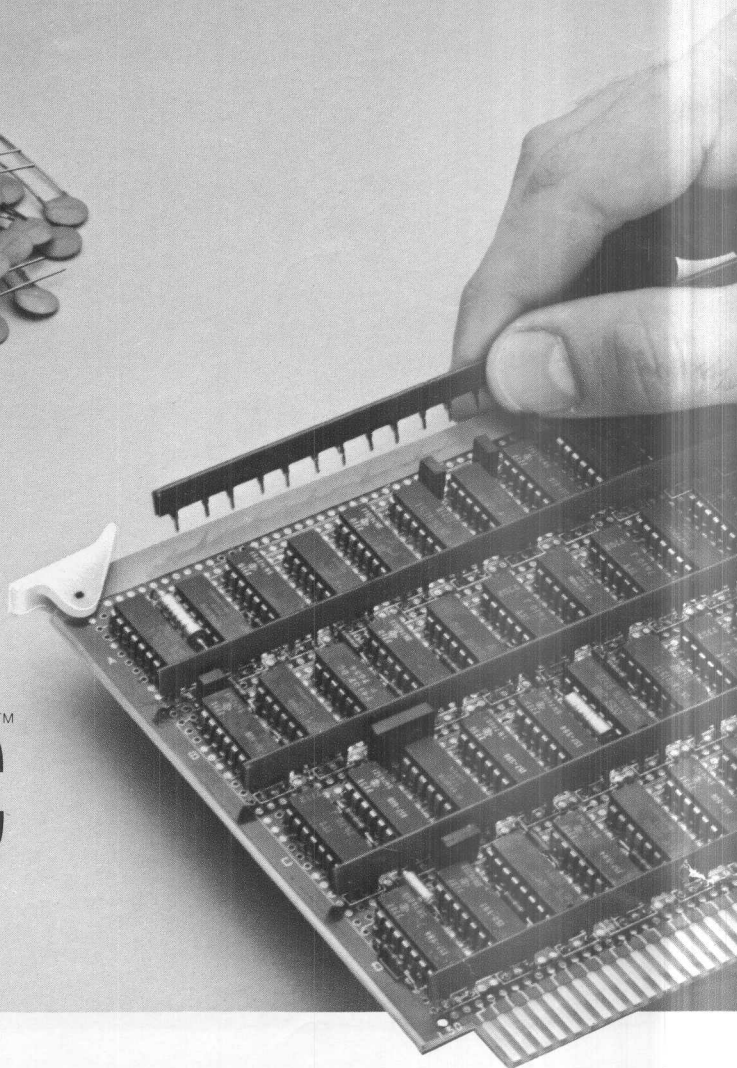
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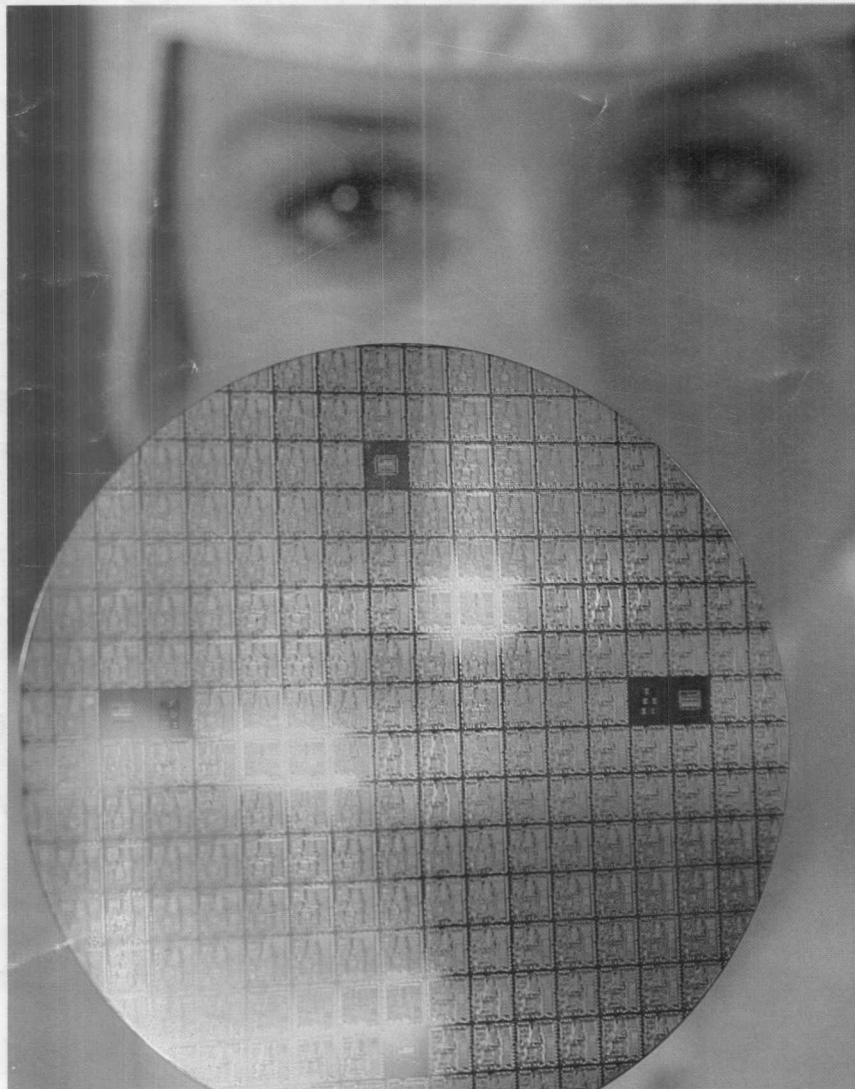
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